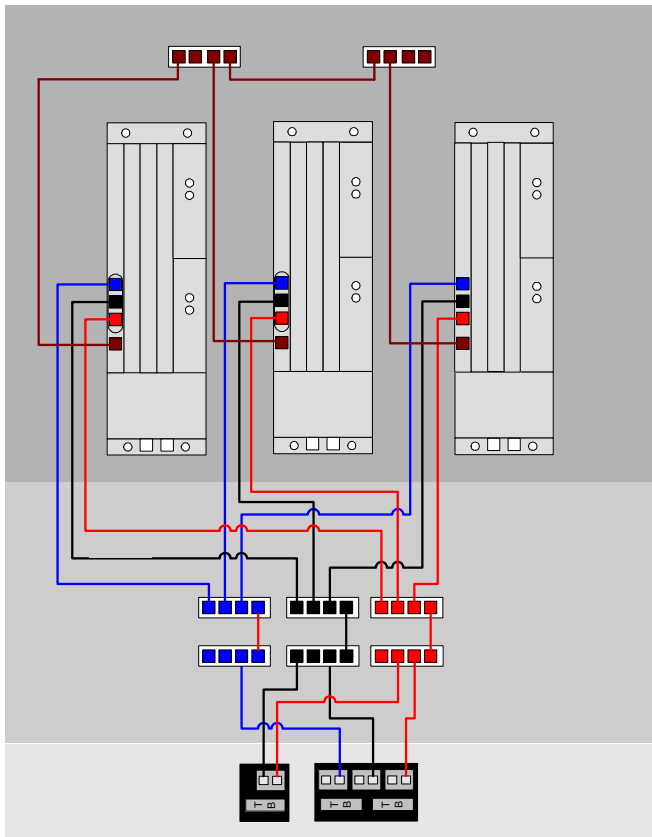


GE Energy

# Mark\* V1e Control System Guide, Volume II

GEH-6721G



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# ***Safety Symbol Legend***



***Warning***

Indicates a procedure, condition, or statement that, if not strictly observed, could result in personal injury or death.

---



***Caution***

Indicates a procedure, condition, or statement that, if not strictly observed, could result in damage to or destruction of equipment.

---



***Attention***

Indicates a procedure, condition, or statement that should be strictly followed in order to optimize these applications.

---

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***Note*** Indicates an essential or important procedure, condition, or statement.

---



This equipment contains a potential hazard of electric shock or burn. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

Isolation of test equipment from the equipment under test presents potential electrical hazards. If the test equipment cannot be grounded to the equipment under test, the test equipment's case must be shielded to prevent contact by personnel.

To minimize hazard of electrical shock or burn, approved grounding practices and procedures must be strictly followed.

---



To prevent personal injury or equipment damage caused by equipment malfunction, only adequately trained personnel should modify any programmable machine.

---

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## ***Notes***

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## Mark\* Vle Controller

The Mark\* Vle UCCx controllers are a family of CPCI, 6U high, single-board computers that run the application code. The controller mounts in a CompactPCI<sup>®</sup> (CPCI) enclosure, and communicates with the I/O packs through on board I/O network interfaces. The controller operating system (OS) is QNX<sup>®</sup> Neutrino<sup>®</sup>, a real-time, multitasking OS designed for high-speed, high-reliability industrial applications. Five communication ports provide links to I/O, operator, and engineering interfaces as follows:

- Ethernet connection for the Unit Data Highway (UDH) for communication with HMIs, and other control equipment
- Ethernet connection for the R, S, and T I/O network
- RS-232C connection for setup using the COM1 port

---

**Note** The I/O networks are private special purpose Ethernet that support only the I/O packs and the controllers.

---

### Operation

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**Note** Application software can be modified online without requiring a restart.

---

The controller is loaded with software specific to its application, which includes but is not limited to steam, gas, and land-marine aeroderivative (LM), or balance of plant (BOP) products. It can run rungs or blocks. The IEEE<sup>®</sup> 1588 protocol is used through the R, S, and T IONets to synchronize the clock of the I/O packs and controllers to within  $\pm 100$  micro seconds.

External data is transferred to and from the control system database in the controller over the R, S, and T IONets.

In a simplex system, this includes process inputs/outputs to the I/O packs.

In a dual system:

- Process inputs/outputs to the I/O packs
- Internal state values and initialization information from the designated controller
- Status and synchronization information from both controllers

In a triple modular redundant (TMR) system:

- Process inputs/outputs to the I/O packs
- Internal state values from for voting and status and synchronization information from all three controllers
- Initialization information from the designated controller

## Configuration

The controller must be configured with a TCP/IP address prior to connecting to the UDH Ethernet. This is achieved through the ToolboxST\* application and the COM1 serial port. See *GEH-6700, ToolboxST Guide for Mark VIe Control* for details.

## Installation

The controller module contains (at a minimum) a controller and a four-slot CPCI rack with either one or two power supplies. The primary controller must be placed in the left-most slot (slot 1). A second, third, and fourth controller can be placed in a single rack.

---

**Note** If the slot 1 controller is removed, the other controllers will stop operating.

---

The CMOS battery is disconnected using a processor board jumper during storage to extend the life of the battery. When installing the board, the battery jumper must be reinstalled. Refer to the specific UCCx module drawing for jumper location. The battery supplies power to the CMOS RAM settings and the internal date and real-time clock. There is no need to set CMOS settings since the settings are defaulted to the proper values through the BIOS. Only the real-time clock must be reset. The initial date and time can be set using a system NTP server or ToolboxST application.

If the board is the system board (slot 1 board) and other boards are in the rack, ejection of the system board will cause the other boards to stop operating. It is recommended that power be removed from the rack when replacing any board in the rack. Rack power can be removed by one of the following methods.

- In a single power supply unit, a switch is provided to disable the power supply outputs.
- In a dual power supply unit, both power supplies can be safely ejected to remove power.
- Unplug the bulk power input Mate-N-Lok<sup>®</sup> connector(s) on the bottom of the CPCI enclosure.
- Use a remote disconnect switch.

Unlike the Mark VI VME boards that provided only ejectors, the UCCx module has injectors/ejectors at the bottom and top of the module. Before sliding the board in the rack, the top ejector should be tilted up and the bottom ejector should be tilted down. When the connector on the backside of the board connects with the backplane connector, the injectors should be used to fully insert the board. This is done by pushing down on the top injector and pulling up on the bottom ejector. Remember to finish the installation by tightening the top and bottom injector/ejector screws. This provides mechanical security as well as a chassis ground connection.

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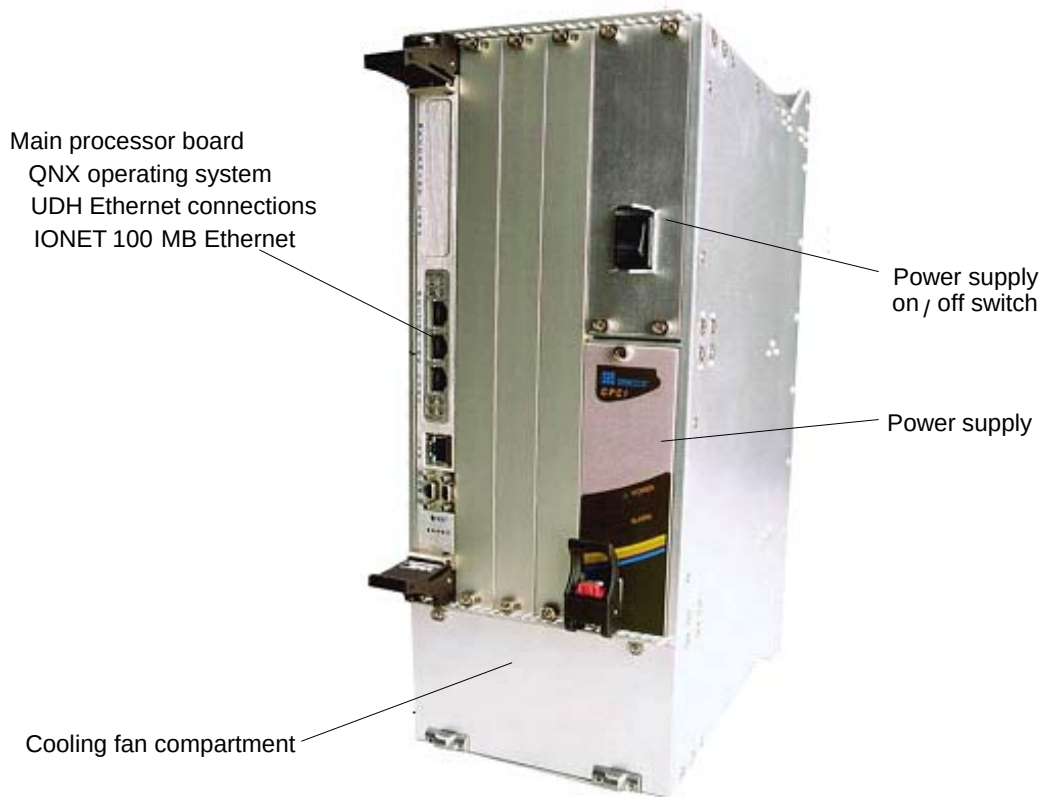
**Note** Failing to lock the injectors will prevent the controller from booting. When extracting the board, perform the insertion process in reverse. See the next section on configuration before connecting the Ethernet cables. If a previous application is loaded in the module, mis-operation may occur if the Ethernet addresses collide with other operating equipment.

---



## CPCI Component Replacement

The following sections provide replacement procedures for the CPCI control module.



*CPCI Controller*

### ➤ To replace the CPCI controller

- 1** Power down the CPCI rack. If the rack has a single power supply (version P1), turn off the power switch located on the panel above the power supply. The power can also be removed by disconnecting the bulk power plug from the bottom of the rack or by using a remote disconnect.
- 2** When two power supplies are used (version P2), loosen the top and bottom screw on each one. Press down the red tab in the black release lever on each power supply. Press down on the black release lever and pull out to disconnect both power supplies from the CPCI rack backplane. The power can also be removed by disconnecting the bulk power plugs from the bottom of the rack or by using a remote disconnect.
- 3** Loosen the screws at the top and bottom of the controller.
- 4** Press down on the top ejector tab and pull up on the bottom ejector tab to disconnect the controller from the backplane. Carefully pull the controller out of the CPCI rack.
- 5** Carefully slide the new controller module into the CPCI enclosure.
- 6** Press up on the top injector/ejector tab and push down on the bottom injector/ejector tab to seat the controller connectors with the receptacles on the backplane.
- 7** Tighten the screws at the top and bottom of the controller, securing it in the CPCI enclosure.

- 8 Power up the controller by turning on the power switch on CPCI enclosure with a single power supply or pushing in on both power supplies and securing them on a CPCI enclosure using dual supplies.
- 9 Configure controller with TCP/IP address prior to connecting the UDH Ethernet cable. This is done using the ToolboxST application and COM1 serial port.
- 10 Connect the UDH Ethernet cable to the LAN port. Connect the three IONet Ethernet cables to the appropriate receptacles.

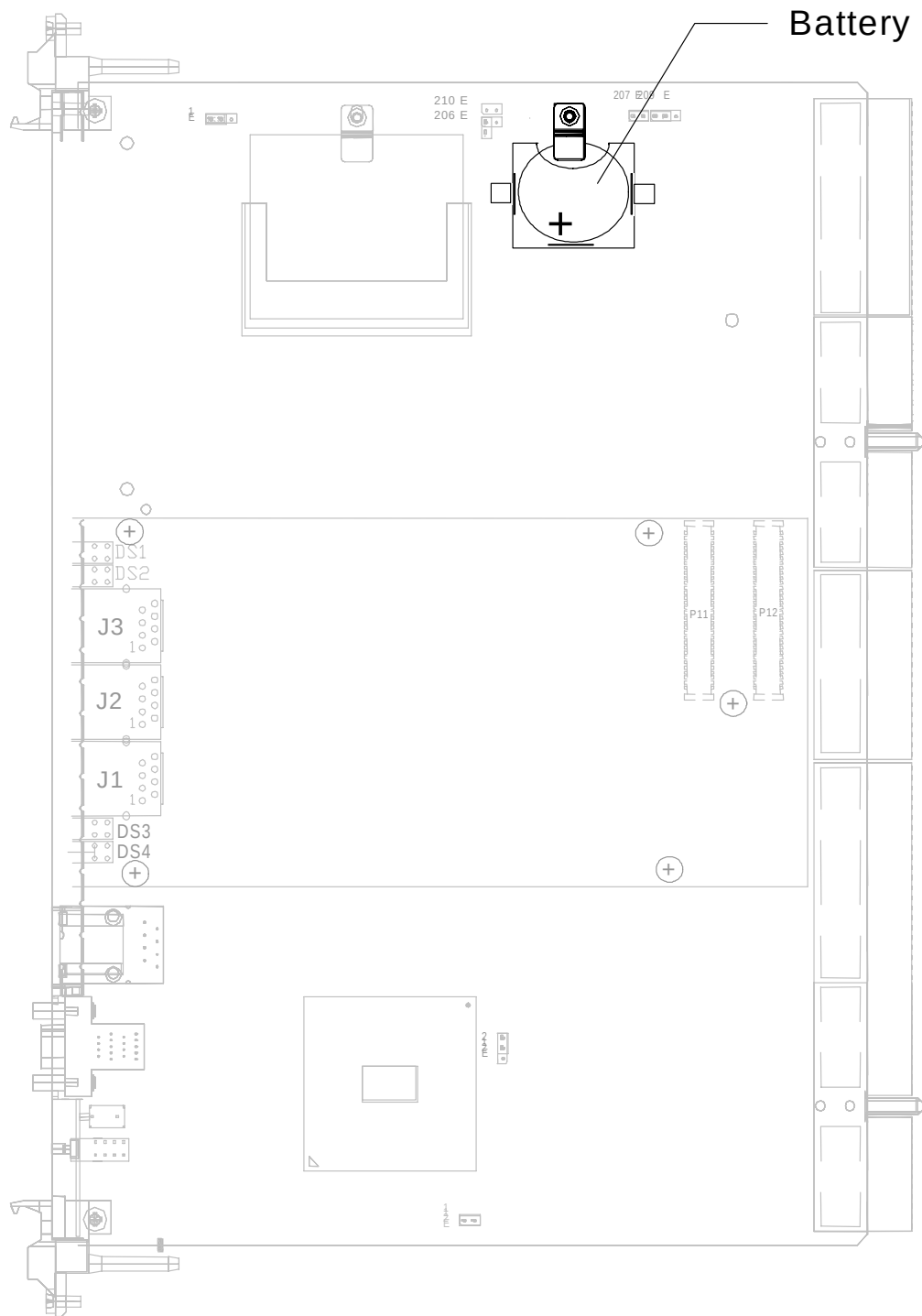
## ***Controller Battery***

The UCCx uses a lithium battery to supply power to the CMOS (which contains the BIOS settings for the CPU board) and the real-time clock when the controller is not on. Default CMOS settings are also stored in flash memory, so when the battery reaches end-of-life, only the real-time clock functions are lost.

The lithium battery for the UCCx has a service life of 10 years. The battery is disabled in stock and can be disabled when storing a controller. If the controller is stored with the battery disabled, its life expectancy is 10 years, minus the time the controller has been in service. If the controller is stored with the battery enabled, the life expectancy drops to seven years minus the time the controller has been in service. An expired battery can be replaced on the controller board.

### **➤ To replace the controller battery**

- 1 Power down the CPCI rack. If the rack has a single power supply (version P1), turn off the power switch located on the panel above the power supply.
- 2 Loosen the screws at the top and bottom of the controller.
- 3 Press down on the top ejector tab and pull up on the bottom ejector tab to disconnect the controller from the backplane. Carefully pull the controller out of the CPCI rack.
- 4 Locate the battery near the top, inboard side of the controller.
- 5 Loosen the screw on the tab holding the battery and move it out of the way.
- 6 Slide the expired battery out of its enclosure, making note that the positive (+) side faces away from the controller.
- 7 Insert the new battery. Reposition the holding tab and tighten the screw.
- 8 Slide the controller back into the CPCI rack and secure it in place.
- 9 Use the ToolboxST application to reset the real-time clock.



*UCCx Controller Battery*

## Cooling Fan

A cooling fan is located in a tray at the bottom of the CPCI rack. The cooling fan can fail, causing temperatures to rise to a level that will damage the controllers and power supplies. The cooling fan can be replaced without removing power to the rack.

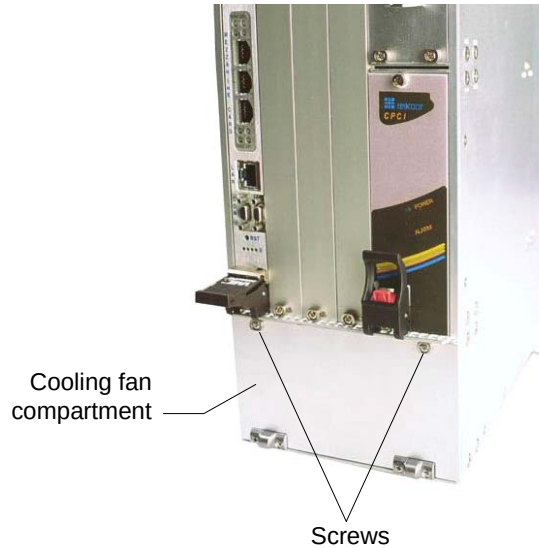
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**Note** The controller automatically monitors the CPU core temperature and can be configured to continue to run, or to reboot the controller into a low power failure state. See the help for the TEMP\_STATUS function block for details.

---

➤ **To replace the cooling fan**

- 1 Loosen the two screws at the top of the door located at the bottom of CPCI rack.
- 2 Open the door and slide the old cooling fan out of the rack. There are no cables to remove. The fan assembly plugs directly into the backplane.
- 3 Insert a new cooling fan into the guides in the compartment and push in firmly. If the fan is not completely in place, the compartment door will not close.
- 4 Close the door and tighten the two screws at the top.



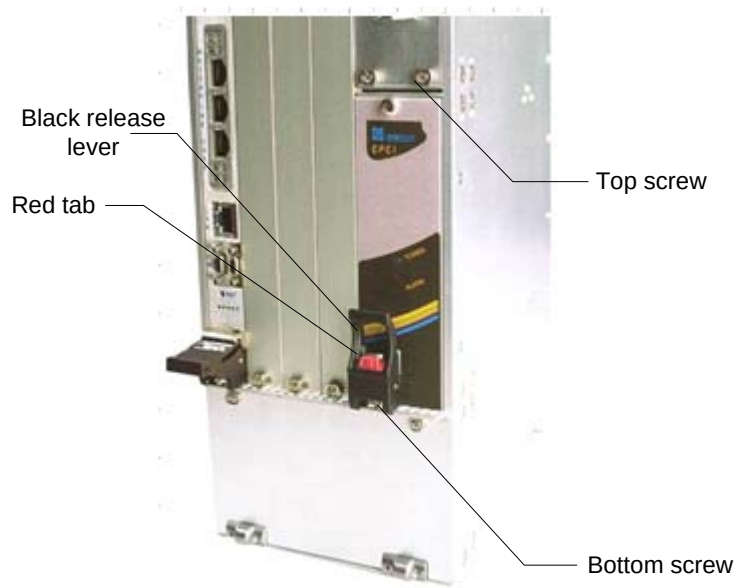
*Replacing CPCI Cooling Fan*

## **Power Supply(s)**

The CPCI rack can hold one or two power supplies. The power supplies plug directly into the backplane using a standard CPCI 47-pin connector. The power supply(s) are hot swap compliant and can be safely removed without powering down the CPCI rack.

➤ **To replace the CPCI power supply(s)**

- 1 Loosen the two screws holding the power supply in the rack. The bottom screw is located beneath the black ejection lever at the bottom of the power supply faceplate.
- 2 Press down on the red tab inside the black ejection lever to release it.
- 3 Push the black release lever down to unplug the power supply from the backplane.
- 4 Slide the power supply out of the CPCI rack.
- 5 Slide the new power supply(s) into the CPCI rack. Ensure the front of the power supply is flush with the other components in the enclosure.
- 6 Push the black ejection lever up. The red tab in the black ejection lever will snap up when the power supply is fully inserted.
- 7 Tighten the top and bottom screws.



*Replacing CPCI Power Supply*

## **EPMC**

The CPCI controllers support a single PCI Mezzanine Card (PMC) daughterboard called the IS200EPMC.

The IS200EPMC contains specific Mark VIe controller hardware functions as follows:

- Power supply monitoring
- Flash backed SRAM
- IONet Ethernets
- Ethernet physical layer packet snooping for precision time synchronization

The EPMC board plugs onto one of the PMC sites and communicates to the processor board through the PCI bus. The PCI interface on the EPMC is PCI Rev 2.2 compliant and supports both 3.3 V and 5 V signal levels.

## **UCCA Processor**

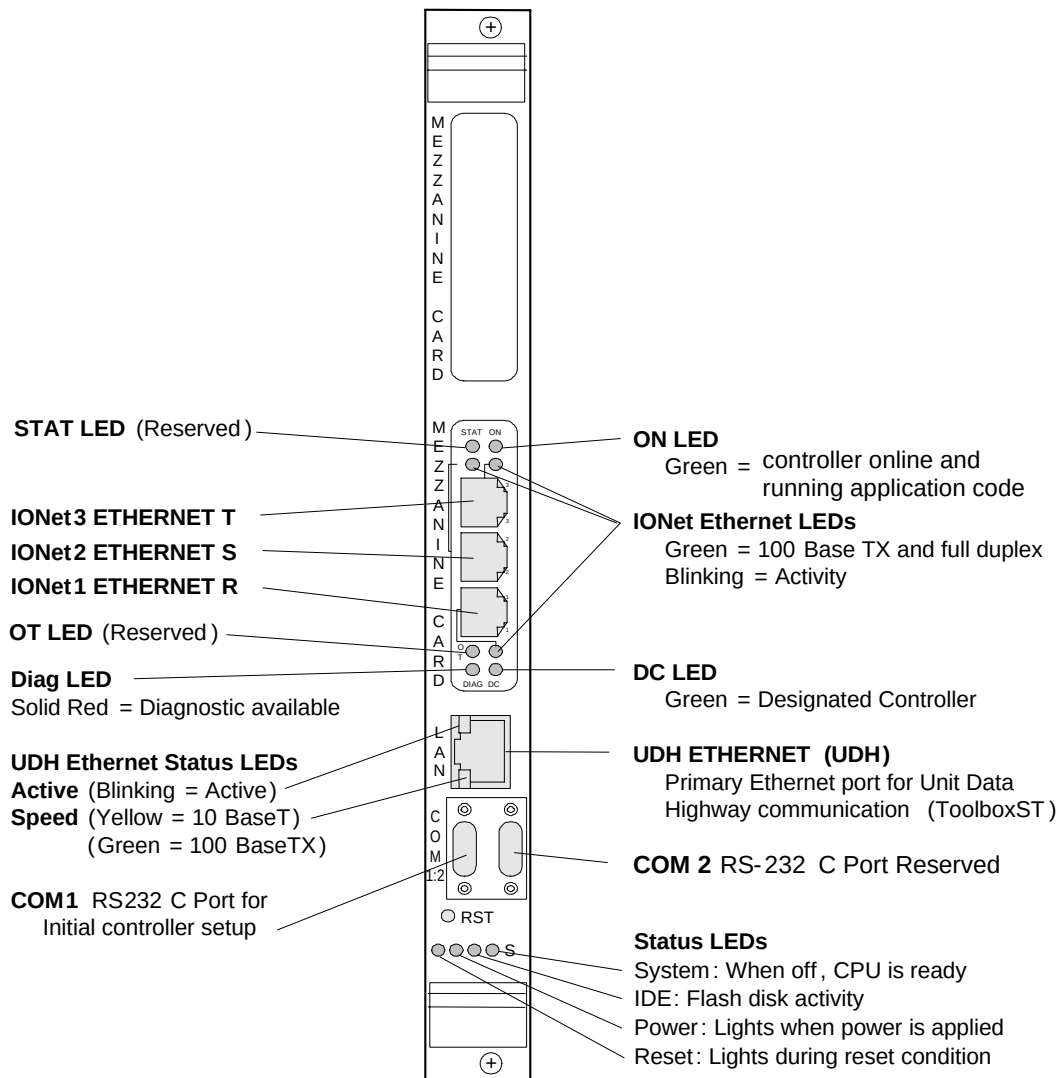
The IS215UCCAH3 is a single-slot board using a 650 MHz Intel<sup>®</sup> Celeron processor. A 10BaseT/100BaseTX (RJ-45) Ethernet port provides connectivity to the Unit Data Highway (UDH). There are two PCI Mezzanine Card (PMC) sites and a watchdog timer.

The processor board is the compute engine of the Mark VIe controller.

## **Modules**

The IS215UCCAM03 is a module assembly that includes the IS215UCCAH3 combined with 128 MB of flash memory, 128 MB of DRAM, and the IS200EPMC.

## UCCA Front View



## UCCAM03 Specifications

| Item                                  | Specification                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Microprocessor                        | Intel Ultra Low Voltage Celeron 650 MHz (8.3 Watts Max.)                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Memory                                | 128 MB DDR SDRAM through one SODIMM<br>128 MB Compact Flash Module<br>256 KB L2 cache<br>Flash-backed SRAM - 8K allocated as NVRAM for controller functions                                                                                                                                                                                                                                                                                                                                              |
| Operating System                      | QNX Neutrino                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Programming                           | Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include:<br><br>Boolean<br>16-bit signed integer<br>16-bit unsigned integer<br>32-bit signed integer<br>32-bit unsigned integer<br>32-bit floating point<br>64-bit long floating point                                                                                                                                                                            |
| Primary Ethernet interface (one port) | TCP/IP protocol used for communication between controller and toolbox<br>TCP/IP protocol used for alarm communication to HMIs<br>EGD protocol for application variable communication with CIMPLICITY <sup>®</sup> HMI and Series 90-70 PLCs<br>Ethernet Modbus <sup>®</sup> protocol supported for communication between controller and third-party DCS                                                                                                                                                  |
| EPMC Ethernet Interface (three ports) | Twisted pair 10BaseT/100BaseTX, RJ-45 connectors:<br>TCP/IP protocols used to communicate between controllers and I/O packs                                                                                                                                                                                                                                                                                                                                                                              |
| COM ports                             | Two micro-miniature 9-pin D connectors:<br><br>COM1 Reserved for diagnostics, 9600 baud, 8 data bits, no parity, 1 stop bit<br>COM2 Not used<br><br>For cabling use either:<br><br>a standard 4 pair UTP cable (e.g. Ethernet cable) joined with a PC <sup>®</sup> null modem connector (GE part #342A4931ABP1) and a controller connector (GE part #342A4931ABP2) or a miniature D shell, null modem serial cable (GE part #336A3582P1), connected with a micro-miniature pigtail (GE part #336A4929G1) |
| Environmental Specifications          | Temperature: Operating 0 to 60°C (32 to +140 °F)<br>Temperature: Storage -40 to +85°C (-40 to +185 °F)<br>Humidity: 5 to 95% non-condensing<br>Altitude: Operating 0 to 10,000 ft. (3,000 m)<br>Altitude: Storage 0 to 40,000 ft (12,000 m)                                                                                                                                                                                                                                                              |
| Power requirements                    | +3.3 V dc, 3.5 A typical, 4.25 A maximum<br>+5 V dc, 150 mA typical, 300 mA maximum                                                                                                                                                                                                                                                                                                                                                                                                                      |



### **Caution**

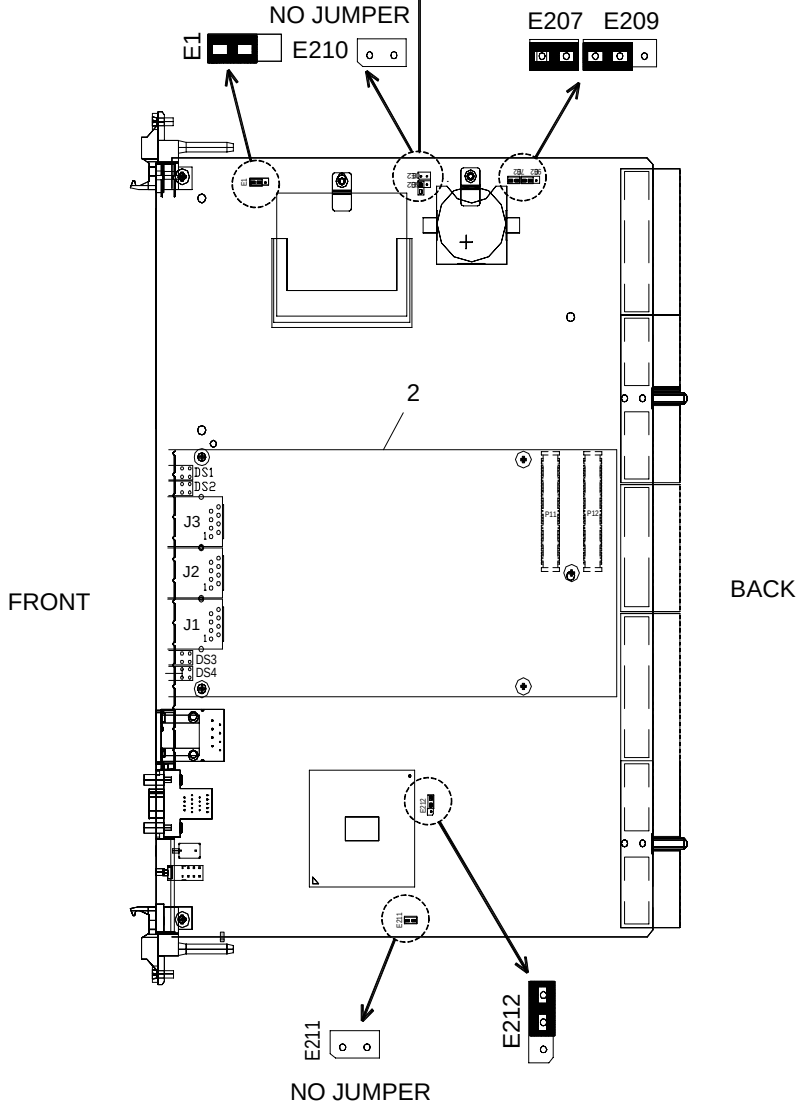
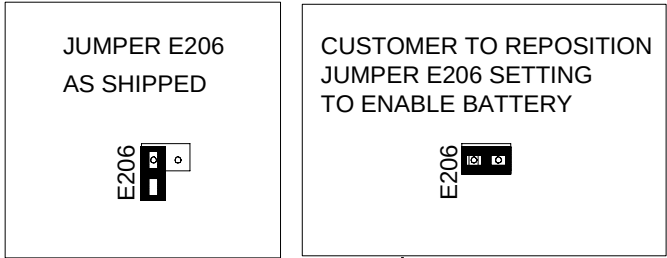
**Airflow requirements as measured at the output side of the heat sink must be greater than 400LFM to prevent overheating and potential damage to the board.**

# UCCA Jumper Location and Settings

\*\*\*

## CPU BOARD JUMPER SETTINGS

| JUMPER NAME        | JUMPER FUNCTION                | JUMPER POSITION |
|--------------------|--------------------------------|-----------------|
| E1                 | PASSWORD CLEAR                 | 1 - 2           |
| E204               | ITP                            | NO JUMPERS      |
| E206               | BATTERY ENABLE                 | 1 - 2 ***       |
| E210, E211<br>E212 | FACTORY RESERVED<br>DO NOT USE |                 |
| E209               | WATCHDOG TIMER<br>RESET ENABLE | 1 - 2           |
| E207               | IGNORE CPCI<br>RESET           | 1 - 2           |



## UCCA Controller Jumper Settings

### UCCC Processor

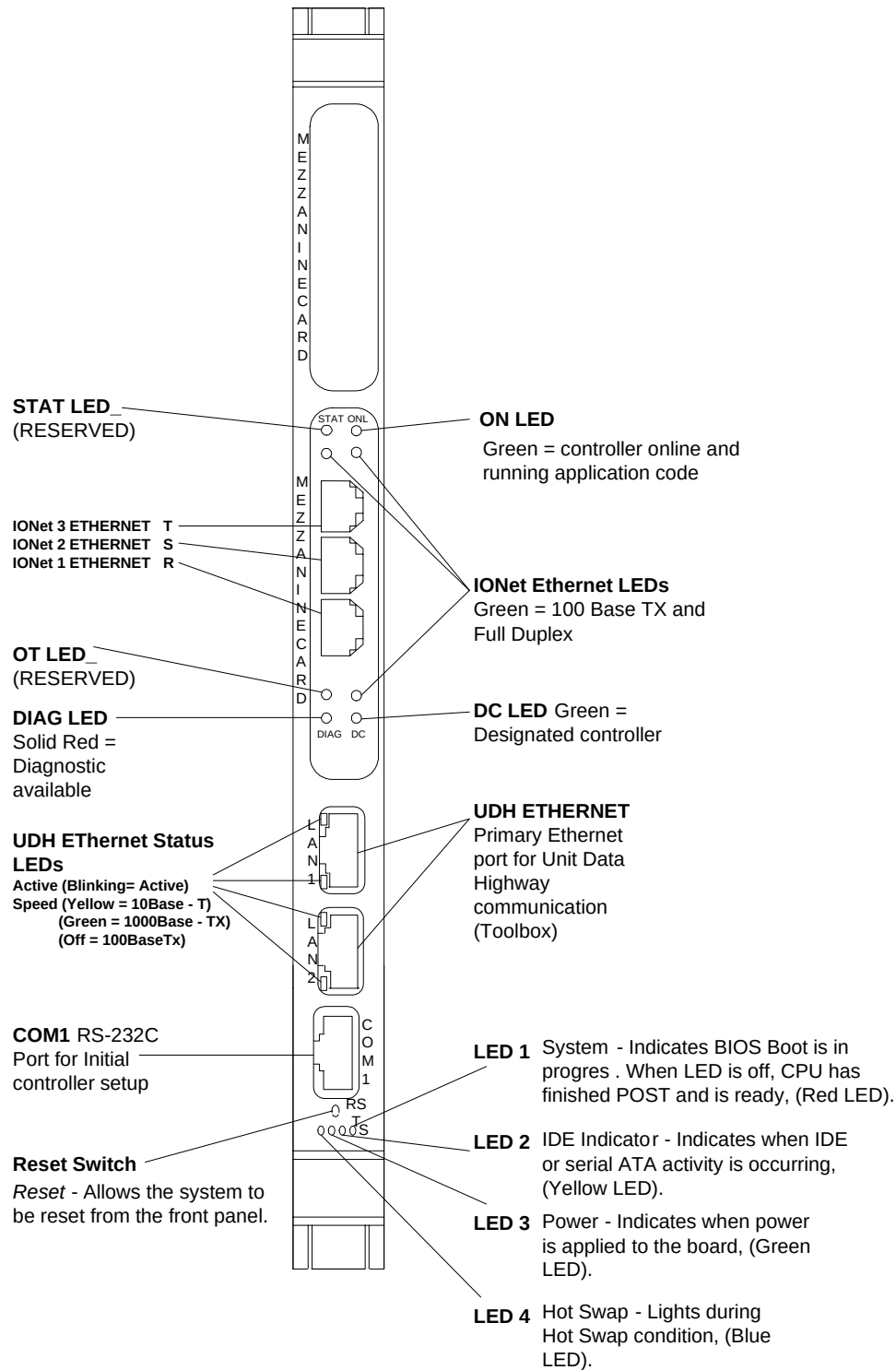
The IS215UCCCCH4 is a single-slot CPCI controller board containing a 1.6 GHz Pentium® M processor. Two 10/100/1000BaseTX Ethernet ports provide connectivity to the UDH and an optional Ethernet network.



## Modules

The IS215UCCCM04 is a module assembly that includes the IS215UCCCH4 combined with 128 MB of flash memory, 256 MB of DRAM, and the IS200EPMC.

### UCCC Front View



## UCCCM04 Specifications

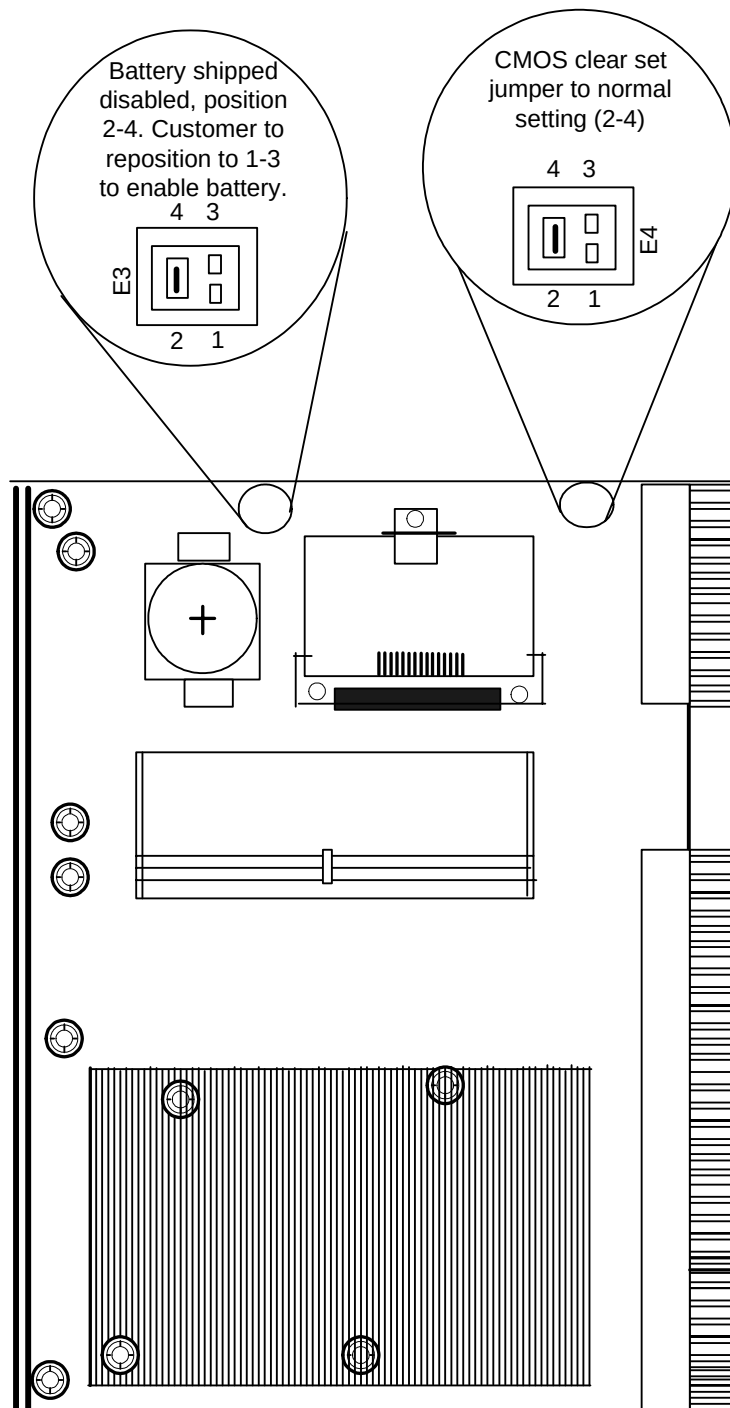
| Item                              | Specification                                                                                                                                                                                                                                                                                                                                                                          |
|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Microprocessor                    | Intel Pentium M processor 1.6 GHz                                                                                                                                                                                                                                                                                                                                                      |
| Memory                            | 256 MB DDR SDRAM through one SODIMM<br>128 MB Compact Flash Module<br>256 KB L2 cache<br>Flash-backed SRAM - 8K allocated as NVRAM for controller functions                                                                                                                                                                                                                            |
| Operating System                  | QNX Neutrino                                                                                                                                                                                                                                                                                                                                                                           |
| Programming                       | Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include:<br><br>Boolean<br>16-bit signed integer<br>16-bit unsigned integer<br>32-bit signed integer<br>32-bit unsigned integer<br>32-bit floating point<br>64-bit long floating point                                                          |
| Primary Ethernet Interface (2)    | Twisted pair 10BaseT/100BaseTX, RJ-45 connectors:<br><br>TCP/IP protocol used for communication between controller and toolbox<br>TCP/IP protocol used for alarm communication to HMIs<br>EGD protocol for application variable communication with CIMPLICITY HMI and Series 90-70 PLCs<br>Ethernet Modbus protocol supported for communication between controller and third party DCS |
| EPMC Ethernet Interface (3 ports) | Twisted pair 10BaseT/100BaseTX, RJ-45 connectors:<br>TCP/IP protocols used to communicate between controllers and I/O packs                                                                                                                                                                                                                                                            |
| COM ports                         | One accessible through RJ45 connector on front panel<br><br>For cabling use a standard 4 pair UTP cable (e.g. Ethernet cable) joined with a PC null modem connector (GE part #342A4931ABP1)                                                                                                                                                                                            |
| Power Requirements                | +5 V dc (+5%, -3%, 4.5 A (typical), 6.75 maximum)<br>+3.3 V dc, (+5%, -3%, 1.5 A (typical), 2.0 A maximum)<br>+12 V dc (+5%, -3%), 50 mA maximum<br>-12 V dc (+5%, -3%), 50 mA maximum                                                                                                                                                                                                 |
| Environmental Specifications      | Operating: 0 to +50°C (32 to +122 °F)<br>Storage: -40 to +85°C (-40 to +185 °F)<br>Relative humidity: 5% to 95%, no-condensing                                                                                                                                                                                                                                                         |
| Mechanical Specifications         | Shock: 10 Gs, 16 ms half sine, 6 axis, 10 pulses each<br>Vibration: 6 Gs RMS (20-2000 Hz) random, 0.0185 G <sup>2</sup> per Hz                                                                                                                                                                                                                                                         |



### **Caution**

Airflow requirements as measured at the output side of the heat sink must be greater than 300LFM to prevent overheating and potential damage to the board.

## UCCC Jumper Location and Settings



## Diagnostic Alarms

The controller detects certain system errors during startup, download, and normal operation. These diagnostic alarms can be displayed and reset from the ToolboxST application, and are recorded in historical manner on WorkstationST\*.

| Alarm | Description                                                              | Possible Cause                                                                                                                                                                       | Solution                                                                                                                                                                                                                                                                                                                  |
|-------|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 259   | [ ] frame overruns have occurred                                         | Runtime sequencer malfunction. One or more frame overruns, which occur when frame idle time is 0, detected.                                                                          | Replace processor module.                                                                                                                                                                                                                                                                                                 |
| 260   | [ ] frame number skips have occurred                                     | Runtime malfunction. Frame number skips have been detected. (Other than during frame synchronization during startup, the frame number should monotonically increase until rollover.) | "                                                                                                                                                                                                                                                                                                                         |
| 279   | Sys - Could not determine platform type from hardware                    | Incorrect firmware version or hardware malfunction The firmware could not recognize the host hardware type.                                                                          | Ensure all connectors are aligned properly and fully seated. Check firmware version for compatibility with platform; if OK, replace processor module.                                                                                                                                                                     |
| 280   | Sys - Platform hardware does not match runtime application               | The platform type identified in the application configuration does not match the actual hardware.                                                                                    | Fix platform type in ToolboxST application, rebuild and download application.                                                                                                                                                                                                                                             |
| 281   | Sys - FPGA not programmed due to platform errors                         |                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                           |
| 282   | Sys - Unable to initialize application independent processes             | Runtime malfunction. An application-independent firmware process could not be started successfully.                                                                                  | Reload firmware and application and reboot. For Controller, if failure persists remove CompactFlash module and reprogram boot loader using ToolboxST Download Flash Bootloader pick. After reinstalling the flash module and rebooting, reload firmware and application. If this does not work, replace processor module. |
| 283   | Sys - Process disconnected illegally.                                    | Runtime or hardware malfunction. A runtime process has crashed.                                                                                                                      | "                                                                                                                                                                                                                                                                                                                         |
| 284   | Process fault detected.                                                  | "                                                                                                                                                                                    | "                                                                                                                                                                                                                                                                                                                         |
| 292   | A seq client did not respond to an overrun event prior to the next frame | Excessive application loading.                                                                                                                                                       | Check application loading and reduce the amount of application code or frequency of execution.                                                                                                                                                                                                                            |
| 294   | Controller CPU over temperature, Temp [ ] °C, Threshold [ ] °C           | Fan loss. excessive ambient temperature, hardware malfunction.                                                                                                                       | Check fan, ambient temperature, dust buildup on processor module; if OK, replace processor module.                                                                                                                                                                                                                        |
| 300   | Application code load failure                                            | Invalid application configuration, firmware or hardware malfunction.                                                                                                                 | Rebuild and download application to all processors; reload firmware and application; replace processor module.                                                                                                                                                                                                            |
| 320   | Alarm - scan buffers full. Alarm process can miss alarm transitions      | Too many alarm variables are changing state too quickly to transmit all of the transitions. Excessive alarms in queue.                                                               | If possible, reduce the number of alarms that can change state at the same time, e.g., filter alarm variables in the application code.                                                                                                                                                                                    |
| 321   | Alarm - not scanning. App stopped sending Data                           | Runtime malfunction. Alarms not being scanned. Processor will likely reboot on a S/W watchdog timeout due to a processor overload.                                                   | If processor does not reboot, condition was transient. Clear alarm and monitor for repeat occurrences, which may indicate spurious processor overloads. Check idle time and reduce application load if necessary.                                                                                                         |

| Alarm | Description                                                                 | Possible Cause                                                                                                                                                                                                                                                                                                                                             | Solution                                                                                                                                                                                       |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 322   | EGD configuration >1400 bytes, may not be supportable by fault tolerant EGD | Number of relevant, consumed UDH EGD variables exceeds fault tolerant EGD limitation. Normal UDH EGD operation is not affected; however, in the event of a UDH EGD failure, some consumed variables may not be transmitted to redundant controllers over the IONet.                                                                                        | Reduce amount of relevant, consumed UDH EGD data.                                                                                                                                              |
| 323   | Received request to send fault tolerant EGD data to redundant controllers   | Redundant processor unable to receive UDH EGD inputs and has requested that EGD data be transferred over the IONet. An EGD exchange timeout has occurred on the requesting processor.                                                                                                                                                                      | Check UDH network and verify that all redundant processors are receiving all of the expected EGD exchanges. Ensure that all relevant devices are powered up and producing data on the network. |
| 324   | Requested fault tolerant EGD data from redundant controllers                | Unable to receive UDH EGD inputs and the exchange data is being requested over the IONet.                                                                                                                                                                                                                                                                  | "                                                                                                                                                                                              |
| 326   | Communication lost from R processor                                         | IONet or hardware malfunction. The S or T processor in a redundant system has lost communication with the R processor.                                                                                                                                                                                                                                     | Verify that the processor is in the Controlling state. Check for disconnected IONet cables or malfunctioning switches. Rebuild and download application.                                       |
| 327   | Communication lost from S processor                                         | IONet or hardware malfunction. The R or T processor in a redundant system has lost communication with the S processor.                                                                                                                                                                                                                                     | "                                                                                                                                                                                              |
| 328   | Communication lost from T processor                                         | IONet or hardware malfunction. The R or S processor in a redundant system has lost communication with the T processor.                                                                                                                                                                                                                                     | "                                                                                                                                                                                              |
| 329   | Data initialization timeout R processor                                     | IONet malfunction, controllers have different application revisions, one or more controllers are powered down, or controller is overloaded by external command messages. Controller unable to complete startup Data Initialization.                                                                                                                        | Check IONets; rebuild and download application, ensure all controllers are powered up, disable jabbering command senders (e.g., Modbus masters) until controller is online.                    |
| 330   | Data initialization timeout S processor                                     | "                                                                                                                                                                                                                                                                                                                                                          | "                                                                                                                                                                                              |
| 331   | Data initialization timeout T processor                                     | "                                                                                                                                                                                                                                                                                                                                                          | "                                                                                                                                                                                              |
| 334   | App frame number skip                                                       | Hardware or IONet malfunction. Frame number skips detected. Frame number should monotonically increase until rollover; alarm occurs following a single frame number skips in successive frames.                                                                                                                                                            | Check IONet (switches, cables); replace processor module.                                                                                                                                      |
| 335   | Process code segment CRC mismatch                                           | Hardware memory failure. A modification has occurred in the code segment for one of the processes.                                                                                                                                                                                                                                                         | Replace processor module.                                                                                                                                                                      |
| 336   | Controller is unlocked                                                      | Mark VleS: leaving Data Init control state and not locked or the controller is unlocked through the ToolboxST application.                                                                                                                                                                                                                                 | Lock the controllers from ToolboxST application before executing safety functions.                                                                                                             |
| 337   | EGD output exchange disagreement detected                                   | IONet malfunction or hardware problem. For at least one output, a difference was detected between the three controllers in a SIS. This alarm remains active until the controllers agree on all outputs. A difference for non-Boolean data generally indicates a deviation of more than 10% from the median value or no IONet EGD configuration is present. | Check IONet (switches, cables); rebuild and download application to all processors; if this doesn't help, replace processor module.                                                            |

| Alarm | Description                                                 | Possible Cause                                                                                                                                                                                                                               | Solution                                                                                                                                                                                                                                        |
|-------|-------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 347   | Running Application does not match the BRANDED Application  | Mark VIeS: Application not branded or different from branded version                                                                                                                                                                         | Reload branded application to controller and I/O packs or use ToolboxST application to brand currently running application.<br><b>Note:</b> the purpose of branding is to label a verified safety application and to ensure that it is running. |
| 348   | Packet loss on IONet 1 exceeded [ ]%                        | Power cycled on I/O producer (controller or I/O pack), IONet malfunction, I/O message corruption. Communication errors have occurred on more than 5% of the data transmissions on IO Net.                                                    | Check IONet (switches, cables); make sure alarm did not occur due to pack reboot, etc.                                                                                                                                                          |
| 349   | Packet loss on IONet 2 exceeded[ ]%                         | "                                                                                                                                                                                                                                            | "                                                                                                                                                                                                                                               |
| 350   | Packet loss on IONet 3 exceeded [ ]%                        | "                                                                                                                                                                                                                                            | "                                                                                                                                                                                                                                               |
| 352   | Blockware app static data CRC mismatch                      | Hardware memory failure. App process data that should not change after the Controller goes online was modified. This may indicate a hardware memory problem.                                                                                 | Replace processor module.                                                                                                                                                                                                                       |
| 353   | Sys Config Shmem CRC mismatch                               | Hardware memory failure. System process data that should not change after the Controller goes online was modified.                                                                                                                           | "                                                                                                                                                                                                                                               |
| 354   | EGD static data CRC mismatch                                | Hardware memory failure. IONet-EGD process data that should not change after the Controller goes online was modified.                                                                                                                        | "                                                                                                                                                                                                                                               |
| 355   | State Exchange Voter disagreement detected                  | IONet malfunction or hardware problem. State Exchange disagreement found.                                                                                                                                                                    | Check IONet (switches, cables); if this doesn't help, replace processor module.                                                                                                                                                                 |
| 356   | NANs in CALC Block detected                                 | NAN received from I/O interface or hardware problem.                                                                                                                                                                                         | Check external devices that may be sending NANs to the controller; if conditions persists, replace processor module.                                                                                                                            |
| 357   | Sequencer client out-of-order execution detected            | Hardware malfunction. Sequencer critical clients scheduled out of order. Alarm occurs following three successive frames of sequencer critical client out-of-order execution detections; after five, controller put in FAILURE control state. | Replace processor module.                                                                                                                                                                                                                       |
| 358   | Sequencer client execution underrun detected                | Hardware malfunction. Sequencer critical client underrun detected. Alarm occurs after a sequencer critical client has been run slower than its nominal rate three times in a row; after five, controller put in FAILURE control state.       | "                                                                                                                                                                                                                                               |
| 359   | Sequencer client execution overrun detected                 | Hardware malfunction. Sequencer critical client overrun detected. Alarm occurs after a sequencer critical client has been run faster than its nominal rate three times in a row; after five, controller put in FAILURE control state.        | "                                                                                                                                                                                                                                               |
| 360   | Sequencer frame period out-of-bounds ( $\pm 5\%$ ) detected | Hardware malfunction. Frame period greater than $\pm 5\%$ of nominal. Alarm occurs following frame period out-of-bounds condition occurring three frames in a row; after five, controller put in FAILURE control state.                      | "                                                                                                                                                                                                                                               |

| Alarm | Description                                                        | Possible Cause                                                                                                                                                                                                                              | Solution                                                                        |
|-------|--------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| 361   | Sequencer frame state timeout out-of-bounds ( $\pm 5\%$ ) detected | Hardware malfunction. Sequencer frame state timeout greater than $\pm 5\%$ of nominal. Alarm occurs following a sequencer frame state timeout being out-of-bounds three frames in row; after five, controller put in FAILURE control state. | "                                                                               |
| 362   | Sequencer frame number skip detected                               | Hardware or IONet malfunction. Frame number skips detected. Frame number should monotonically increase until rollover; alarm occurs following three skips in a row, after five, controller put in FAILURE control state.                    | Check IONet (switches, cables); replace processor module.                       |
| 363   | Seq static data CRC mismatch                                       | Hardware memory failure. Sequencer process data that should not change after the Controller goes online was modified.                                                                                                                       | Replace processor module.                                                       |
| 364   | Too many SEV disagreements in a single packet                      | IONet malfunction or hardware problem. SEV disagreement overflow. Firmware cannot handle more than 128 disagreements at once.                                                                                                               | Check IONet (switches, cables); if this doesn't help, replace processor module. |

**Note** The following IONet EGD input validation alarms are numbered starting from a base of 1000 and uniquely created based on I/O pack topology. This is done so that input validation alarms can be generated for each I/O pack in a configuration. Four error messages are associated with each alarm number and are utilized based on particular validation types.

Alarm ID convention: R I/O pack in TMR module or Simplex, single-net I/O pack:  $1000 + \text{ModuleID}$ ; S I/O pack in TMR module:  $1256 + \text{ModuleID}$ ; T I/O pack in TMR module or dual-net or dual I/O pack on IONet 1:  $1512 + \text{ModuleID}$ ; dual-net or dual I/O pack on IONet 2:  $1768 + \text{ModuleID}$ .

| Alarm     | Description                                                    | Possible Cause                                                                                                   | Solution                                                      |
|-----------|----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| 1000-2024 | I/O module [ ], R pack: exch [ ] timed out, IONet [ ]          | I/O pack comm. malfunction or IONet malfunction. (R, S, or T) I/O pack input packet not received timeout.        | Check I/O pack health, diagnostics, IONet (cables, switches). |
| 1000-2024 | I/O module [ ], S pack: exch [ ] timed out, IONet [ ]          | "                                                                                                                | "                                                             |
| 1000-2024 | I/O module [ ], S pack: exch [ ] timed out, IONet [ ]          | "                                                                                                                | "                                                             |
| 1000-2024 | I/O module [ ]: exch [ ] timed out                             | I/O pack comm. malfunction or IONet malfunction. SMX I/O pack input packet not received timeout.                 | "                                                             |
| 1000-2024 | I/O module [ ]: exch [ ] timed out, IONet [ ]                  | I/O pack comm. malfunction or IONet malfunction. SMX I/O pack, dual network input packet not received timeout.   | "                                                             |
| 1000-2024 | I/O module [ ], R pack: exch [ ] major sig mismatch, IONet [ ] | Controller, I/O pack application mismatch. (R, S, or T) I/O pack input packet major signature mismatch detected. | Rebuild application and download.                             |
| 1000-2024 | I/O module [ ], S pack: exch [ ] major sig mismatch, IONet [ ] | "                                                                                                                | "                                                             |
| 1000-2024 | I/O module [ ], T pack: exch [ ] major sig mismatch, IONet [ ] | "                                                                                                                | "                                                             |

| Alarm     | Description                                                        | Possible Cause                                                                                                           | Solution |
|-----------|--------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|----------|
| 1000-2024 | I/O module [ ]: exch y major sig mismatch                          | Controller, I/O pack application mismatch. SMX I/O pack input packet major signature mismatch detected.                  | "        |
| 1000-2024 | I/O module [ ], R pack: exch [ ] cfg timestamp mismatch, IONet [ ] | Controller, I/O pack application mismatch. (R, S, or T) I/O pack input packet configuration timestamp mismatch detected. | "        |
| 1000-2024 | I/O module [ ], S pack: exch [ ] cfg timestamp mismatch, IONet [ ] | "                                                                                                                        | "        |
| 1000-2024 | I/O module [ ], T pack: exch [ ] cfg timestamp mismatch, IONet [ ] | "                                                                                                                        | "        |
| 1000-2024 | I/O module [ ]: exch [ ] cfg timestamp mismatch                    | Controller, I/O pack application mismatch. SMX I/O pack input packet configuration timestamp mismatch detected.          | "        |
| 1000-2024 | I/O module [ ], R pack: exch [ ] received too short, IONet [ ]     | Controller, I/O pack application mismatch. (R, S, or T) I/O pack input packet received shorter than expected.            | "        |
| 1000-2024 | I/O module [ ], S pack: exch [ ] received too short, IONet [ ]     | "                                                                                                                        | "        |
| 1000-2024 | I/O module [ ], T pack: exch [ ] received too short, IONet [ ]     | "                                                                                                                        | "        |
| 1000-2024 | I/O module [ ]: exch [ ] received too short                        | Controller, I/O pack application mismatch. SMX I/O pack input packet received shorter than expected.                     | "        |

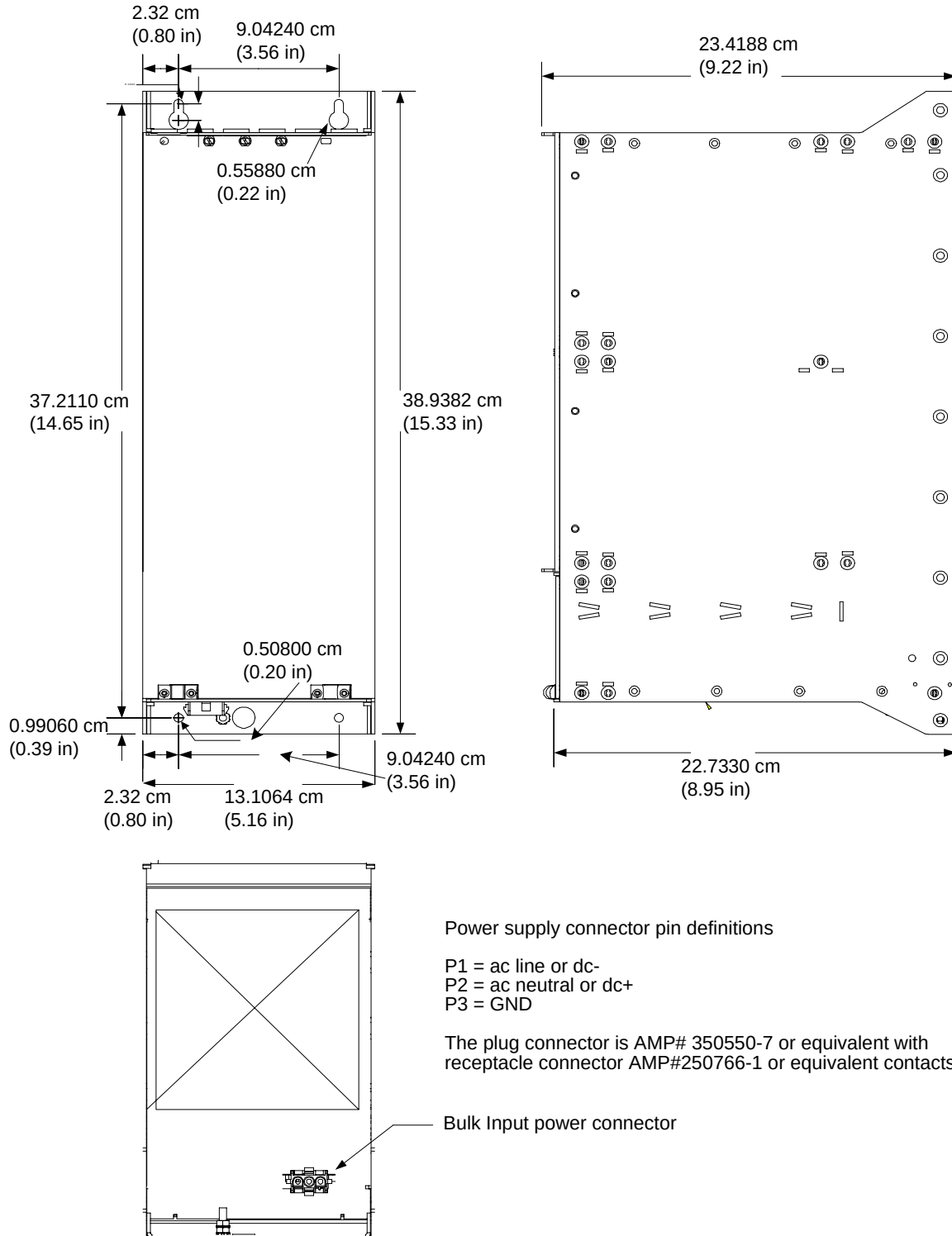
## Enclosure

The CompactPCI<sup>®</sup> (CPCI) control module rack provides an enclosure for the controller, an enclosure for the power supplies(s), and a cooling system. The rack backplane is a CompactPCI (CPCI) compliant backplane, but is only used to connect the power supplies to the controller and cooling fans.



## Installation

The CPCI rack is designed to be wall-mounted. Use the following drawing to determine the placement of the mounting hardware and the enclosure space required.

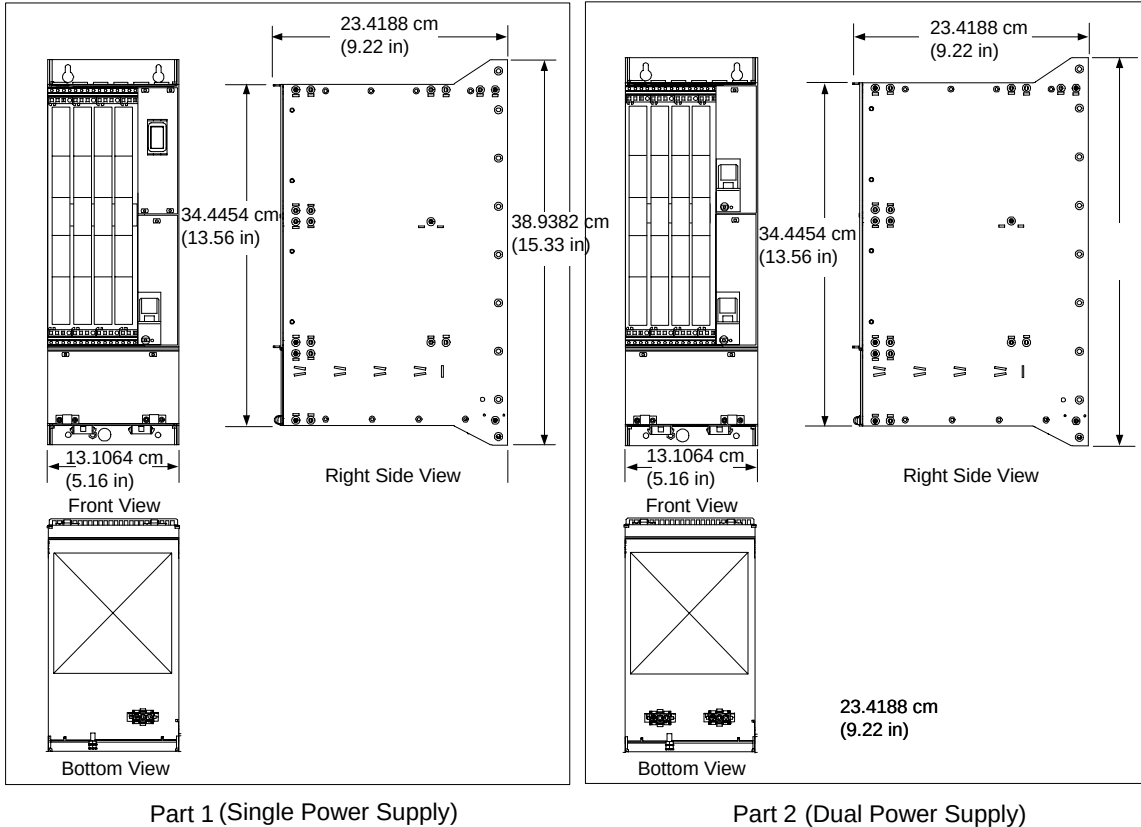


## Operation

Bulk incoming power is supplied to the rack using one or two power connectors. The CPCI power supply converts the bulk input to  $\pm 12$  V dc, 5 V dc, and 3.3 V dc. These voltages are distributed to the controllers and fans through the backplane.

The following rack parts are available.

| Catalog #    | # Power Supplies Ports | Power Inputs |
|--------------|------------------------|--------------|
| 336A4940CTP1 | 1                      | 1            |
| 336A4940CTP2 | 2                      | 2            |



The P1 version contains a on/off switch located in the upper right panel. The switch is connected to the disable outputs pin of the power supply, which turns off power to the controllers and fans. The P2 version does not have a switch so power is removed by ejecting the power supplies, disconnecting the incoming bulk power plugs or using a remote disconnect.

## Specifications

| Item                | Specification                                                                                                                                                                                                                                |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Environment         | Temperature: Operating 0 to +65°C (+32 to +149 °F)<br>Temperature: Storage - 40 to +85°C (-40 to +185 °F)<br>Humidity: 5 to 95% non-condensing<br>Altitude: Operating 0 to 10,000 ft. (3,000 m)<br>Altitude: Storage 0 to 50,000 ft          |
| Air flow provided   | 300 linear feet per minute                                                                                                                                                                                                                   |
| Codes and Standards | UL 508A Safety Standard Industrial Control Equipment<br>CSA 22.2 No. 14 Industrial Control Equipment Class 1 Division 2<br>EN 61010-1 Safety of Electrical Equipment, Industrial Machines<br>IEC 529 Intrusion Protection Codes/NEMA 1/IP 20 |

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## Power Supply(s)

The CPCI power supply takes the incoming bulk power from the CPCI rack and creates  $\pm 12$ , 5, and 3.3 V dc. This power is provided to the backplane for use in the rack, mainly for the controller(s) and cooling fan.

The CPCI rack can hold one or two power supplies. The power supplies plug directly into the backplane using CPCI 47-pin connector. The power supply(s) are hot swap compliant and can be safely removed with powering down CPCI rack.

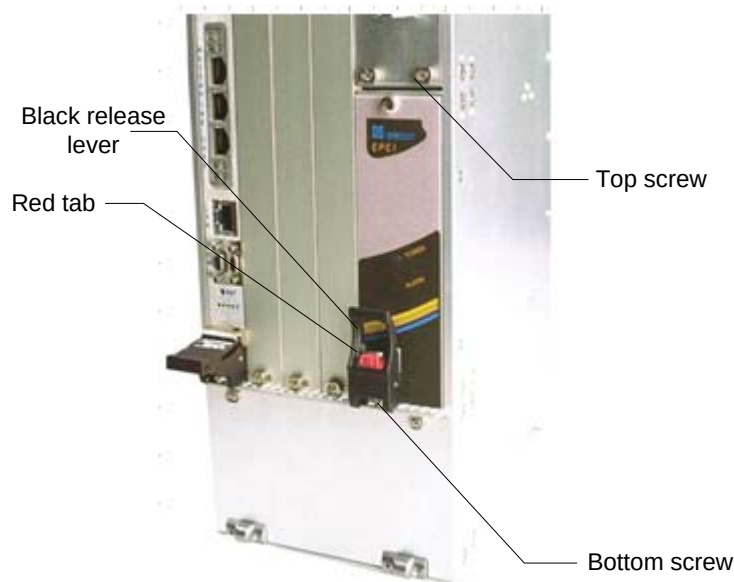
### Installation

#### ➤ To remove the CPCI power supply(s)

- 1 Loosen the two screws holding the power supply in the rack. The bottom screw is located beneath the black ejection lever at the bottom of the power supply faceplate.
- 2 Press down on the red tab inside the black ejection lever to release it.
- 3 Push the black release lever down to unplug the power supply from the backplane.
- 4 Slide the power supply out of the CPCI rack.

#### ➤ To install a new CPCI power supply(s)

- 1 Slide the new power supply(s) into CPCI rack. Ensure the front of the power supply is flush with other components in the enclosure.
- 2 Push the black ejection lever up. The red tab in the black ejection lever will snap up when the power supply is fully inserted.
- 3 Tighten the top and bottom screws.



*Replacing CPCI Power Supply*

## Operation

The power supply is a CPCI Rev 2.11 hot swap compliant 3U power supply using the standard Positronics<sup>®</sup> 47-pin connector. Remote sense and active current share on the +5 and +3.3 V dc outputs along with o-ring FETs allow it to be used in the dual power supply CPCI rack. The  $\pm 12$  V dc outputs use regular o-ring diodes for parallel operation in the dual rack.

The following power supply is supported.

| Catalog # | Input Voltage |
|-----------|---------------|
| 342A4920  | 20-36 V dc    |

## LEDs

The 20-36 V dc power supply has the following LEDs:

- Power: Solid green if all power supply outputs are **OK**. The LED will turn off on any output failure.
- Alarm: Solid red if one or more of the outputs have failed.

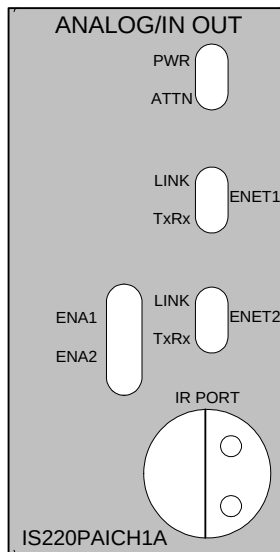
## Specifications

| Item                         | Specification                                                                                                                                                                                                                                                                                     |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Environment                  | Temperature: Operating 0 to +65°C (+32 to +149 °F)<br>Temperature: Storage -40 to +85°C (-40 to +185 °F)<br>Humidity: 5 to 95% non-condensing<br>Altitude: Operating 0 to 10,000 ft. (3,000 m)<br>Altitude: Storage 0 to 50,000 ft<br>Vibration: Random vibration 10 Hz to 2 kHz, 3 axis (1 GRMS) |
| Incoming power               | 20-36 V dc                                                                                                                                                                                                                                                                                        |
| Output power                 | 150 W (De-rated for 65 C operation and 10,000 ft altitude)                                                                                                                                                                                                                                        |
| Over temperature protection  | System shut down due to excessive internal temperature, automatic reset                                                                                                                                                                                                                           |
| Over voltage protection      | Latch style over-voltage protection<br>(110% minimum to 130% of V nom)                                                                                                                                                                                                                            |
| Overload protection          | Fully protected against output overload and short circuit. Automatic recovery upon removal of overload condition                                                                                                                                                                                  |
| Agency Approvals             | UL 1950, UL 1950, EN60950 (TUV)                                                                                                                                                                                                                                                                   |
| Dielectric withstand voltage | Input to output per EN60950 (minimum 1500 V dc)                                                                                                                                                                                                                                                   |
| ESD susceptibility           | Per EN61000-4-2, level 4 (minimum 8 kV)                                                                                                                                                                                                                                                           |
| Radiated Susceptibility      | Per EN61000-4-3, level 3 (minimum 10 V/M)                                                                                                                                                                                                                                                         |
| EFT Burst                    | Per EN61000-4-4, level 3 (minimum $\pm 2$ kV)                                                                                                                                                                                                                                                     |
| Input Surge                  | Per EN61000-4-5, level 3. (Line to Line minimum 1 kV) (Line to Ground minimum 2 kV)                                                                                                                                                                                                               |
| Conducted Disturbance        | Per EN61000-4-6, level 2 (maximum 3 V)                                                                                                                                                                                                                                                            |
| Insulation Resistance        | Input to Output (Nominal 10 M $\Omega$ )                                                                                                                                                                                                                                                          |

# PAIC Analog Input/Output

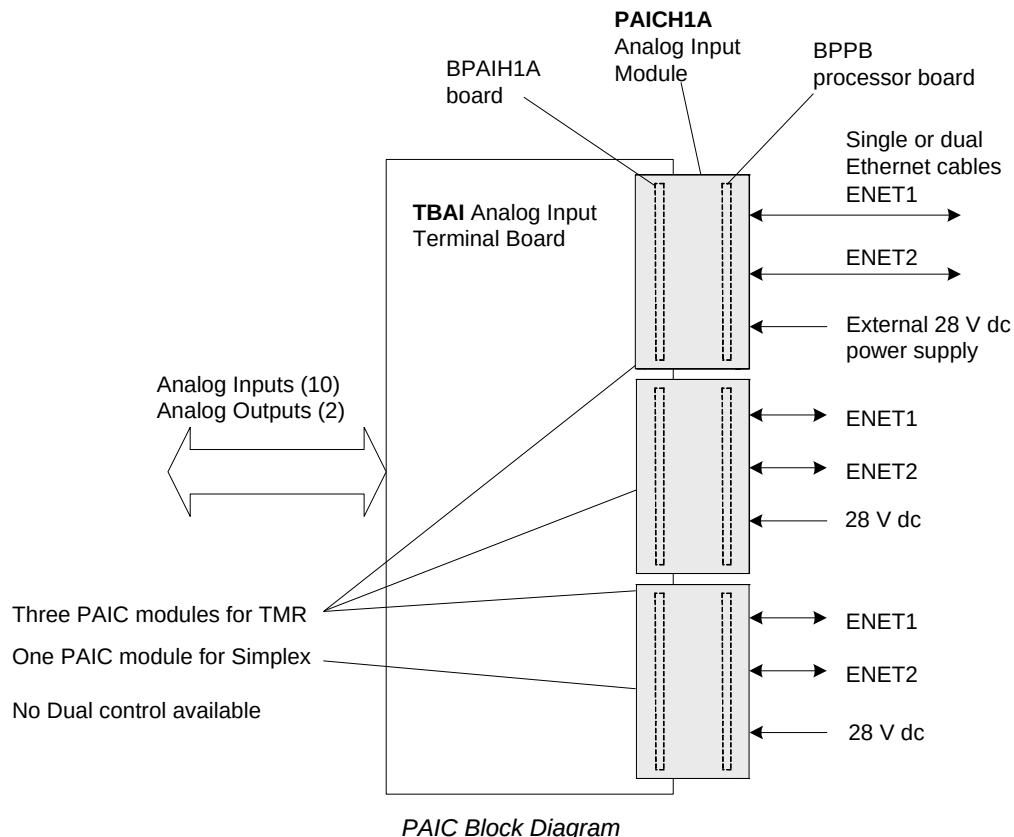
## PAIC Analog Input/Output

### Functional Description



The Analog Input/Output (PAIC) pack provides the electrical interface between one or two I/O Ethernet networks and an analog input terminal board. The pack contains a processor board common to all Mark\* VIE distributed I/O packs and an acquisition board specific to the analog input function. The pack is capable of handling up to 10 analog inputs, the first eight of which can be configured as  $\pm 5$  V or  $\pm 10$  V inputs, or 0-20 mA current loop inputs. The last two inputs may be configured as  $\pm 1$  mA or 0-20 mA current inputs. The load terminal resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the PAIC. The PAICH1 also includes support for two 0-20 mA current loop outputs. The PAICH2 includes extra hardware to support 0-200 mA current on the first output.

Input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PAICH1A is compatible with the analog input terminal board (TBAIH1C), and the STAI board, but not the DIN rail-mounted DTAI board. The following table gives details of the compatibility:

| Terminal Board | TBAIH1C     | DTA       | STAIH1A     |
|----------------|-------------|-----------|-------------|
| Control mode   | Simplex=yes | Dual = no | TMR=yes     |
|                |             | No        | Simplex=yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

While the PAIC will mount on a TBAIH1A or TBAIH1B terminal board the pack will not realize full accuracy of the analog signals due to circuit differences between the terminal board revisions. For this reason, the PAIC is only compatible with the H1C version of TBAI and will report a board compatibility problem with any of the earlier revisions. No physical damage will result if a PAIC is powered up on an older board in error.

## Installation

### ➤ To install the PAIC pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PAIC I/O pack for simplex or three PAIC I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

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**Note** The PAIC mounts directly to a Mark VIe terminal board. Simplex terminal boards have a single DC-37 pin connector that receives the PAIC. TMR-capable terminal boards have three DC-37 pin connectors and can also be used in simplex mode if only one PAIC is installed. The PAIC directly supports all of these connections.

---

# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

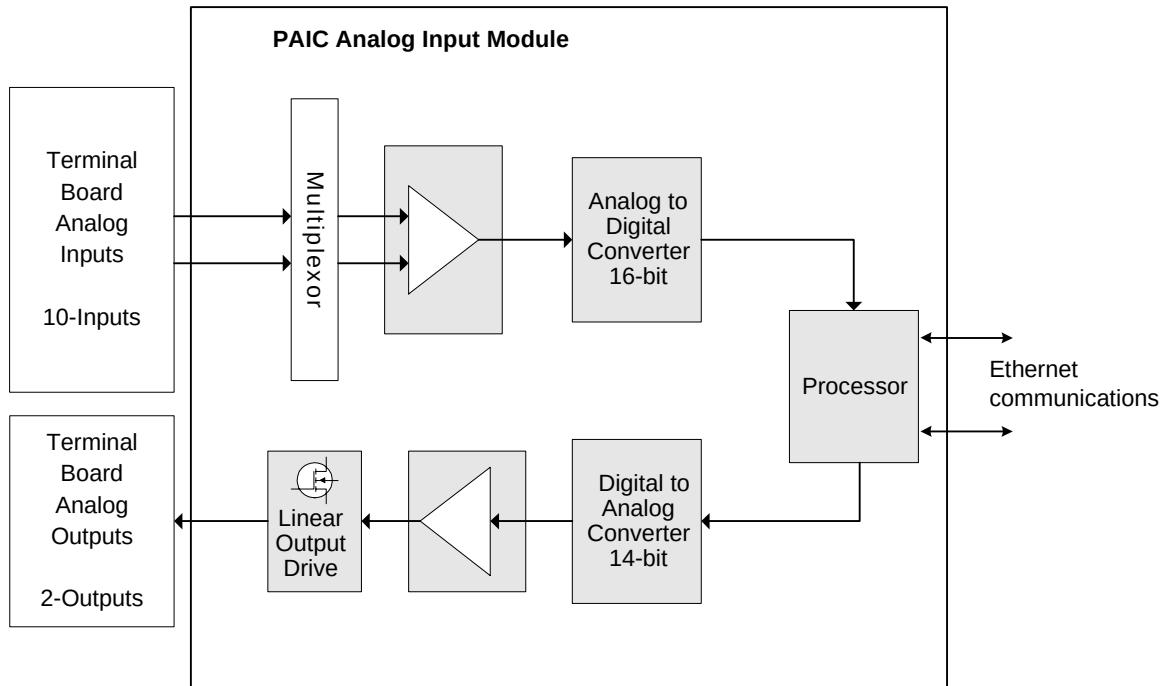
The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## Analog Input Hardware

The PAIC accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an analog multiplexer block, several gain and scaling selections, and a 16-bit analog-to-digital converter (DAC).



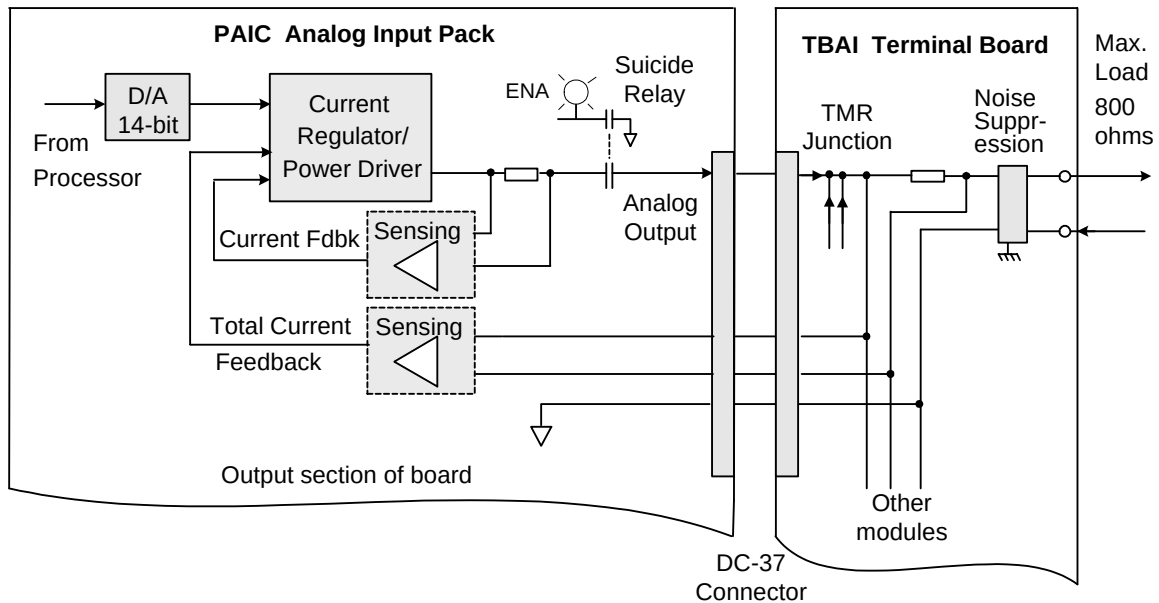
The inputs can be individually configured as  $\pm 5$  V or  $\pm 10$  V scale signals, depending on the input configuration. The terminal board provides a  $250\ \Omega$  burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a passive, low pass filter network with a pole at 75.15 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the PAIC analog input section.



## Analog Output Hardware

The PAIC includes two 0-20 mA analog outputs capable of 18 V compliance running simplex or TMR. A 14-bit DAC commands a current reference to the current regulator loop in the PAIC that senses current both in the PAIC pack and on the terminal board. In TMR mode, the three current regulators in each PAIC share the commanded current loads among themselves. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the PAIC)
- Total current (as sensed from the terminal board, summed current in TMR mode)



Each analog output circuit also includes a normally open mechanical relay to enable or disable operation of the output. The relay is used to remove a failed output from a TMR system allowing the remaining two PAICs to create the correct output without interference from the failed circuit. When the suicide relay is de-activated, the output opens through the relay, open-circuiting that PAIC's analog output from the customer load that is connected to the terminal board. The mechanical relay's second normally open contact is used as a status to indicate position of the relay to the control and includes visual indication with an LED.

## Optional Hardware

The PAIC includes support for additional hardware in the form of an add-on daughterboard that adds 0-200 mA output capability to the first analog output, analog output #1. The 200 mA circuit is capable of 9 V compliance and is identical to the diagram shown with the exception of the P28 power source. Power for the 200 mA circuit is derived from a variable voltage source on the daughterboard to reduce power dissipation of the linear output transistor.

When configured for 200 mA mode operation, the 20 mA suicide relay is automatically opened and the 200 mA suicide relay on the optional daughterboard is closed.

## **ID Line**

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## **Power Management**

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## **Status LEDs**

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## **Connectors**

The pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

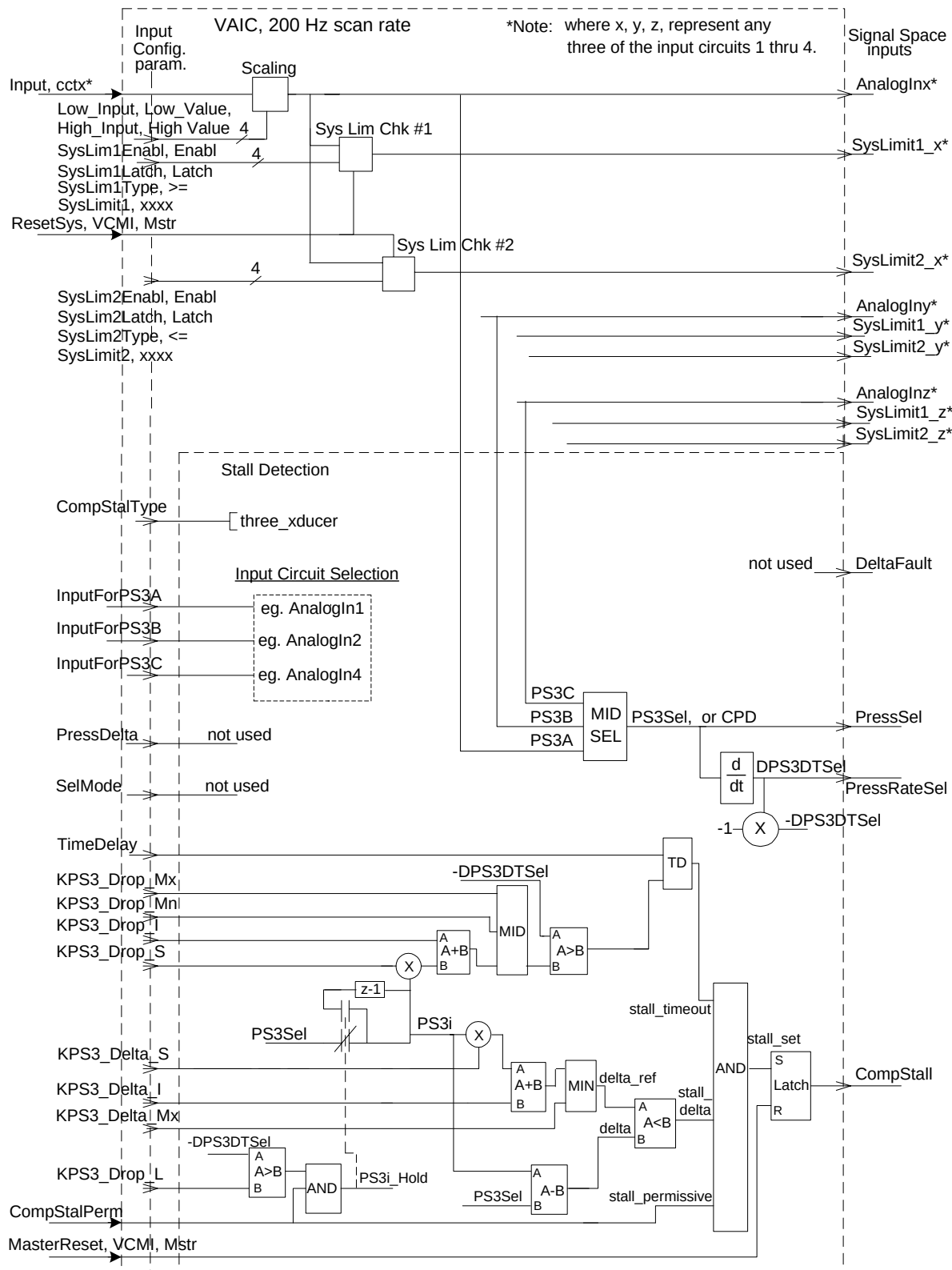
## ***Compressor Stall Detection***

PAIC firmware includes gas turbine compressor stall detection, executed at 200 Hz. Two stall algorithms can be selected. Both use the first four analog inputs, scanned at 200 Hz. One algorithm is for small LM gas turbines and uses two pressure transducers (refer to the figure, *Small (LM) Gas Turbine Compressor Stall Detection Algorithm*). The other algorithm is for heavy-duty gas turbines and uses three pressure transducers (refer to the figure, *Heavy Duty Gas Turbine Compressor Stall Detection Algorithm*).

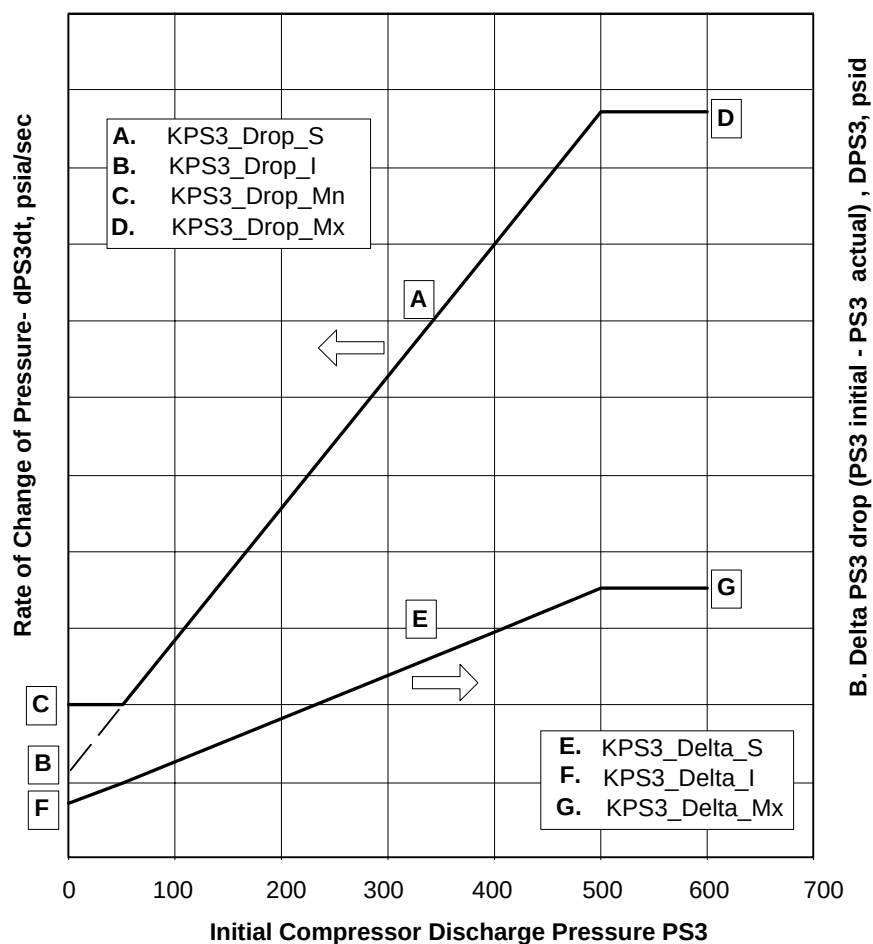
Real-time inputs are separated from the configured parameters for clarity. The parameter CompStalType selects the type of algorithm required, either two transducers or three. PS3 is the compressor discharge pressure. A drop in this pressure (PS3 drop) indicates possible compressor stall. The algorithm also calculates the rate of change of discharge pressure, dPS3dt, and compares these values with configured stall parameters (KPS3 constants).

The compressor stall trip is initiated by PAIC, which sends the signal to the controller where it is used to initiate a shutdown. The shutdown signal can be used to set all the fuel shut-off valves (FSOV) through any relay output.





Heavy Duty Gas Turbine Compressor Stall Detection Algorithm



*Configurable Compressor Stall Detection Parameters*

The variables used by the stall detection algorithm are defined as follows:

| Variable      | Variable Description                             |
|---------------|--------------------------------------------------|
| PS3           | Compressor discharge pressure                    |
| PS3I          | Initial PS3                                      |
| KPS3_Drop_S   | Slope of line for PS3I versus dPS3dt             |
| KPS3_Drop_I   | Intercept of line for PS3I versus dPS3dt         |
| KPS3_Drop_Mn  | Minimum value for PS3I versus dPS3dt             |
| KPS3_Drop_Mx  | Maximum value for PS3I versus dPS3dt             |
| KPS3_Delta_S  | Slope of line for PS3I versus Delta PS3 drop     |
| KPS3_Delta_I  | Intercept of line for PS3I versus Delta PS3 drop |
| KPS3_Delta_Mx | Maximum value for PS3I versus Delta PS3 drop     |

## **Specifications**

The following table provides information specific to the PAIC.

| <b>Item</b>                 | <b>Specification</b>                                                                                                                                                                            |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels          | 12 channels per terminal board (10 AI, 2 AO)                                                                                                                                                    |
| Input span                  | 1 - 5 V dc, $\pm 5$ V dc, $\pm 10$ V dc, or 0-20 mA (Inputs 1-8)<br>0-20 mA or $\pm 1$ mA (Inputs 9-10)                                                                                         |
| Input converter resolution  | 16-bit analog-to-digital converter                                                                                                                                                              |
| Scan time                   | Normal scan 5 ms (200 Hz). Note that controller frame rate is 100 Hz.                                                                                                                           |
| Measurement accuracy        | 0.1% of full scale over the full operating temperature range.                                                                                                                                   |
| Noise suppression on inputs | The ten circuits have a hardware filter with single pole down break at 500 rad/sec. A software filter, using a two pole low pass filter, is configurable for: 0, .75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz |
| Common mode rejection       | Ac common mode rejection 60 dB @ 60 Hz, with up to $\pm 5$ V common mode voltage.<br>Dc common mode rejection 80 dB with from -5 to +7 peak V common mode voltage                               |
| Common mode voltage range   | $\pm 5$ V ( $\pm 2$ V CMR for the $\pm 10$ V inputs)                                                                                                                                            |
| Output converter            | 14-bit D/A converter with 0.5% accuracy                                                                                                                                                         |
| Output load                 | 800 $\Omega$ for 4-20 mA output<br>50 $\Omega$ for 200 mA output                                                                                                                                |
| Power consumption           | 5.3 W typical, 6.2 W worst case                                                                                                                                                                 |
| Compressor stall detection  | Detection and relay operation within 30 seconds                                                                                                                                                 |
| <b>Physical</b>             |                                                                                                                                                                                                 |
| Size                        | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)                                                                                                                        |
| Temperature                 | -30 to +65 °C (-22 to +149 °F)                                                                                                                                                                  |
| Technology                  | Surface mount                                                                                                                                                                                   |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on preset (non-configurable) high and low levels near the end of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. The logic signal, L3DIAG\_xxxx, refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limits.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

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**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

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| Parameter            | Description                                          | Choices                |
|----------------------|------------------------------------------------------|------------------------|
| <b>Configuration</b> |                                                      |                        |
| System Limits        | Enable or disable system limits                      | Enable, disable        |
| Output Voting        | Select type of output voting                         | Simplex, TMR           |
| Min_ MA_Input        | Select minimum current for healthy 4-20 mA input     | 0 to 21 mA             |
| Max_ MA_Input        | Select maximum current for healthy 4-20 mA input     | 0 to 21 mA             |
| CompStalType         | Select compressor stall algorithm (# of transducers) | 0, 2, or 3             |
| InputForPS3A         | Select analog input circuit for PS3A                 | AnalogIn 1, 2, 3, or 4 |
| InputForPS3B         | Select analog input circuit for PS3B                 | AnalogIn 1, 2, 3, or 4 |
| InputForPS3C         | Select analog input circuit for PS3C                 | AnalogIn 1, 2, 3, or 4 |
| SelMode              | Select mode for excessive difference pressure        | Maximum, Average       |
| PressDelta           | Excessive difference pressure threshold              | 5 to 500               |
| TimeDelay            | Time delay on stall detection in (msec)              | 10 to 40               |
| KPS3_Drop_Min        | Minimum pressure rate                                | 10 to 2000             |
| KPS3_Drop_I          | Pressure rate intercept                              | 10 to 100              |



| Parameter         | Description                                                                   | Choices                                        |
|-------------------|-------------------------------------------------------------------------------|------------------------------------------------|
| KPS3_Drop_S       | Pressure rate slope                                                           | .05 to 10                                      |
| KPS3_Delta_S      | Pressure delta slope                                                          | .05 to 10                                      |
| KPS3_Delta_I      | Pressure delta intercept                                                      | 10 to 100                                      |
| KPS3_Delta_Mx     | Pressure delta max                                                            | 10 to 100                                      |
| KPS3_Drop_L       | Threshold pressure rate                                                       | 10 to 2000                                     |
| KPS3_Drop_Mx      | Max pressure rate                                                             | 10 to 2000                                     |
| <b>:IS200TBAI</b> | Terminal board connected to PAIC                                              | Connected, not connected                       |
| AnalogIn1         | First of 10 Analog Inputs – board point. Point edit                           | (Input FLOAT)                                  |
| Input Type        | Current or voltage input type                                                 | Unused, 4-20 mA, $\pm 5$ V, $\pm 10$ V         |
| Low_Input         | Value of current at the low end of scale                                      | -10 to +20                                     |
| Low_Value         | Value of input in engineering units at low end of scale                       | -3.4082 e + 038 to 3.4028 e + 038              |
| High_Input        | Value of current at the high end of scale                                     | -10 to +20                                     |
| High_Value        | Value of input in engineering units at high end of scale                      | -3.4082 e + 038 to 3.4028 e + 038              |
| Input_Filter      | Bandwidth of input signal filter                                              | Unused, 0.75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz        |
| TMR Diff Limit    | Difference limit for voted inputs in % of high-low values                     | 0 to 100                                       |
| Sys Lim 1 Enabl   | Input fault check                                                             | Enable, disable                                |
| Sys Lim 1 Latch   | Input fault latch                                                             | Latch, unlatch                                 |
| Sys Lim 1 Type    | Input fault type                                                              | Greater than or equal Less than or equal       |
| Sys Lim 1         | Input limit in engineering units                                              | -3.4082 e + 038 to 3.4028 e + 038              |
| Sys Lim 2 Enabl   | Input fault check                                                             | Enable, disable                                |
| Sys Lim 2 Latch   | Input fault latch                                                             | Latch, unlatch                                 |
| Sys Lim 2 Type    | Input fault type                                                              | Greater than or equal. Less than or equal      |
| Sys Lim 2         | Input limit in Engineering Units                                              | -3.4082 e + 038 to 3.4028 e + 038              |
| DiagHighEnab      | Enable high input limit                                                       | Enable, disable                                |
| DiagLowEnab       | Enable low input limit                                                        | Enable, disable                                |
| TMRDiffLimit      | Diag limit, TMR input vote difference, in percent of (High_Value - Low_Value) |                                                |
| <b>AnalogOut1</b> | First of two analog outputs - board point                                     | Point edit (Output FLOAT)                      |
| Output_MA         | Type of output current, mA selection                                          | Unused, 0-20 mA, 0-200 mA                      |
| Output_State      | State of the outputs when offline                                             | PwrDownMode<br>Hold Last Value<br>Output_Value |
| Output_Value      | Pre-determined value for the outputs                                          |                                                |
| Low_MA            | Output mA at low value                                                        | 0 to 200 mA                                    |
| Low_Value         | Output in Engineering Units at low mA                                         | -3.4082 e + 038 to 3.4028 e + 038              |
| High_MA           | Output mA at high value                                                       | 0 to 200 mA                                    |
| High_Value        | Output value in Engineering Units at high mA                                  | -3.4082 e + 038 to 3.4028 e + 038              |
| TMR Suicide       | Suicide for faulty output current, TMR only                                   | Enable, disable                                |
| TMR SuicLimit     | Suicide threshold for TMR operation                                           | 0 to 200 mA                                    |
| D/A Err Limit     | Difference between D/A reference and output, in % for suicide, TMR only       | 0 to 100 %                                     |
| Dither Ampl       | Dither % current of Scaled Output mA                                          | 0 to 10                                        |
| Dither_Freq       | Dither rate in Hertz                                                          | Unused, 12.5, 25.0, 33.33, 50.0, 100.0         |

| Board Points<br>(Signals) | Description - Point Edit (Enter Signal Connection) | Direction | Type  |
|---------------------------|----------------------------------------------------|-----------|-------|
| L3DIAG_PAIC               | Board diagnostic                                   | Input     | BIT   |
| LINK_OK_PAIC              | Link Diagnostic Input                              | Input     | BIT   |
| ATTN_PAIC                 | Module Diagnostic                                  | Input     | BIT   |
| IOPackTmpr                | I/O Pack Temperature                               | Input     | FLOAT |
| SysLimit1_1               | System Limit 1                                     | Input     | BIT   |
| :                         | :                                                  | Input     | BIT   |
| SysLimit1_10              | System Limit 1                                     | Input     | BIT   |
| SysLimit2_1               | System Limit 2                                     | Input     | BIT   |
| :                         | :                                                  | Input     | BIT   |
| SysLimit2_10              | System Limit 2                                     | Input     | BIT   |
| OutSuicide1               | Status of Suicide Relay for Output 1               | Input     | BIT   |
| OutSuicide2               | Status of Suicide Relay for Output 2               | Input     | BIT   |
| DeltaFault                | Excessive difference pressure                      | Input     | BIT   |
| CompStall                 | Compressor Stall                                   | Input     | BIT   |
| Out1MA                    | Feedback, Total Output Current, mA                 | Input     | FLOAT |
| :                         | :                                                  | Input     | FLOAT |
| Out2MA                    | Feedback, Total Output Current, mA                 | Input     | FLOAT |
| CompPressSel              | Selected Compressor Press, by Stall Algo.          | Input     | FLOAT |
| PressRate Sel             | Selected Compressor Press rate, by Stall Algor.    | Input     | FLOAT |
| CompStallPerm             | Compressor Stall Permissive                        | Output    | BIT   |

## Alarms

### PAIC Specific Alarms

| Alarm ID | Alarm Description                                                | Possible Cause                                                                                     | Solution                                                                                   |
|----------|------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|
| 32-43    | Analog Input [ ] unhealthy                                       | Excitation to transducer, bad transducer, terminal board jumper settings, or open or short-circuit | Check field wiring and configuration for the indicated analog input channel.               |
| 44-45    | Output [ ] Individual current feedback input unhealthy           | Field wiring problem, field device problem, I/O pack failure, terminal board failure.              | Confirm correct I/O pack 28V input power. Check field wiring and device. Replace I/O pack. |
| 46-47    | Output [ ] Total current feedback input unhealthy                |                                                                                                    |                                                                                            |
| 48-49    | Output [ ] Reference current feedback input unhealthy            |                                                                                                    |                                                                                            |
| 66-67    | Output [ ] Individual current too high relative to total current | Board failure                                                                                      |                                                                                            |
| 70-71    | Output [ ] Total current varies from reference current           | Board failure, or open circuit                                                                     |                                                                                            |
| 74-75    | Output [ ] Reference current error                               | Board failure (D/A converter)                                                                      |                                                                                            |
| 78-79    | Output [ ] Individual current unhealthy                          | Board failure                                                                                      |                                                                                            |
| 82-83    | Output [ ] Suicide relay non-functional                          | Board failure (Relay or driver)                                                                    |                                                                                            |

| Alarm ID | Alarm Description                                                                                                                                                      | Possible Cause                                                                                                                                                  | Solution                                                                                                                      |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| 86-87    | Output [ ] 20/200 mA selection non-functional                                                                                                                          | Configured output type does not match berg jumper selection, or board failure (relay).                                                                          |                                                                                                                               |
| 90-91    | Output [ ] 20/200 mA suicide active                                                                                                                                    | Board failure                                                                                                                                                   |                                                                                                                               |
| 92-93    | Output [ ] Suicide on overcurrent, check terminal board jumper                                                                                                         | Incorrect setting of terminal board 20/200mA jumper, hardware failure in I/O pack.                                                                              | Check terminal board jumper. Replace I/O pack.                                                                                |
| 96       | ConfigCompatCode mismatch; Firmware: [ ] The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board. | A tre file has been installed that is incompatible with the firmware. Either the tre file or firmware must change. Contact the factory                          |                                                                                                                               |
| 99       | +/-15v Power supply input status not OK                                                                                                                                | The internal power supply that provides analog circuit control power is not operating correctly                                                                 | Check I/O pack ground quality through mounting bolts. Confirm 28v input power is within 26.6 - 29.4V range. Replace I/O pack. |
| 100      | Dither Time is frozen or out of range - %3.1f                                                                                                                          | The time signal used to generate a dither on the valve output signal does not appear to be changing. This may cause a frozen valve to occur.                    | Cycle power on I/O pack. Replace I/O pack.                                                                                    |
| 101      | Reference Voltage out of limits                                                                                                                                        | The reference voltage for the analog inputs is more than +/- 5% from the expected value. Indicates a reference, multiplexor, or A/D converter hardware problem. | Check I/O pack ground quality through mounting bolts. Cycle power on I/O pack. Replace I/O pack.                              |
| 102      | Null Voltage out of limits                                                                                                                                             | The Null voltage for the analog inputs is more than 5% from the expected value. Indicates a reference, multiplexor, or A/D converter hardware problem.          | Check I/O pack ground quality through mounting bolts. Cycle power on I/O pack. Replace I/O pack.                              |
| 128-223  | Logic Signal [ ] Voting mismatch<br>The identified status signal from this board disagrees with the voted value.                                                       | A problem with a status input. This could be the device, the wire to the terminal board, or the terminal board.                                                 |                                                                                                                               |
| 224-235  | Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ]                                                                                                                 | Voter disagreement between the R, S and T IO Packs                                                                                                              | Adjust the TMR threshold limit or correct the cause of the difference                                                         |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need: [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

---

## ***TBAI Analog Input/Output***

### ***Functional Description***

The Analog Input/Output (TBAI) terminal board supports 10 analog inputs and 2 outputs. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The analog outputs can be set up for 0-20 mA or 0-200 mA current. Inputs and outputs have noise suppression circuitry to protect against surge and high frequency noise.

TBAI has three DC-37 pin connectors provided on TBAI for connection to the I/O processors. Simplex applications are supported using a single connector (JR1). TMR applications are supported using all three connectors.

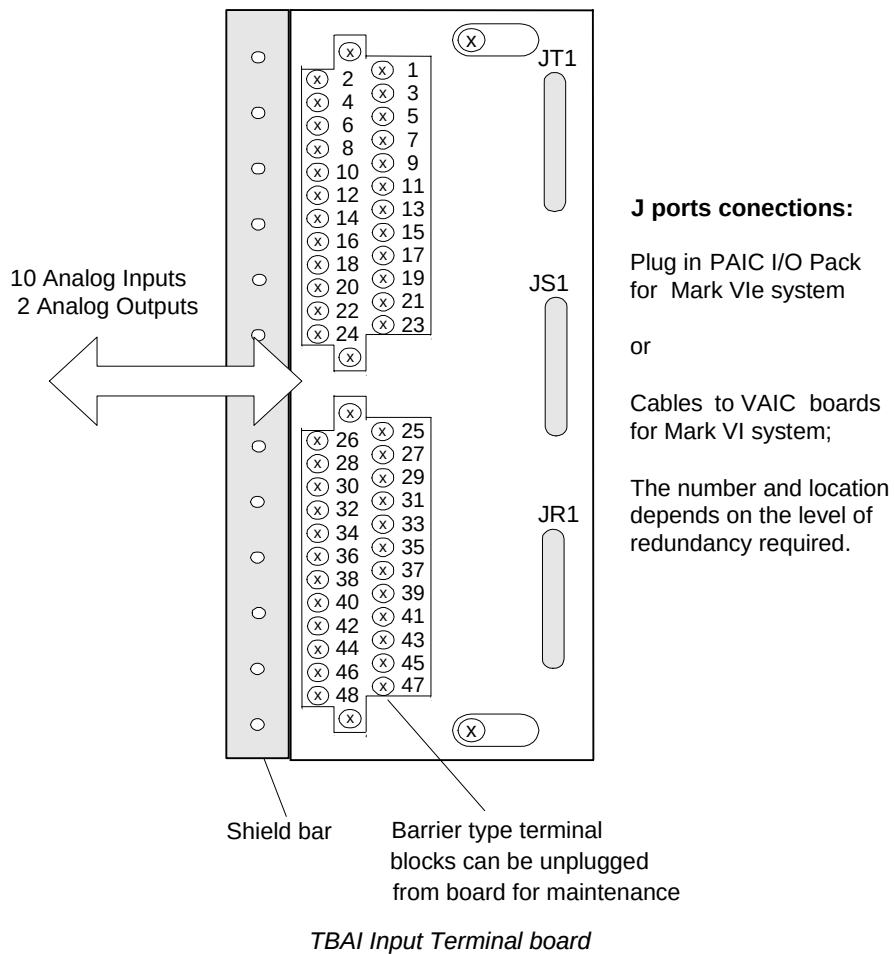
In TMR applications, the input signals are fanned to the three connectors for the R, S, and T controls. TMR outputs combine the current of the three connected output drivers and determine the total current with a measuring shunt. TBAI then presents the total current signal to the I/O processors for regulation to the commanded setpoint.

### ***Mark VI Systems***

In the Mark\* VI system, TBAI works with VAIC processor and supports simplex and TMR applications. One or two TBAs can be connected to the VAIC. In TMR systems, TBAI is cabled to three VAIC boards.

## Mark VIe Systems

In the Mark VIe system, TBAI works with the PAIC I/O pack and supports simplex and TMR applications. In TMR systems, three PAICs plug directly into the TBAI.



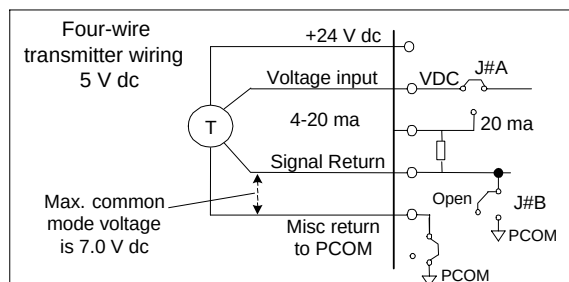
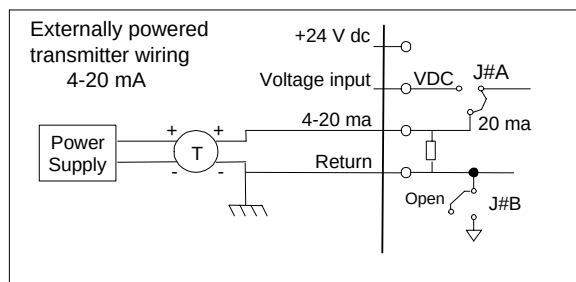
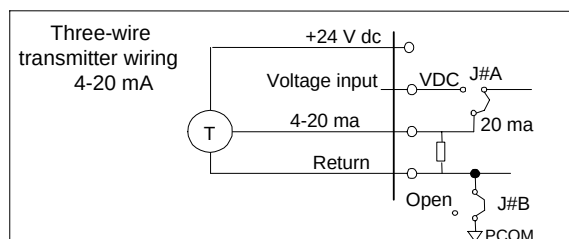
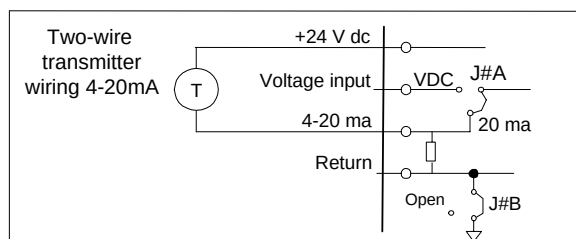
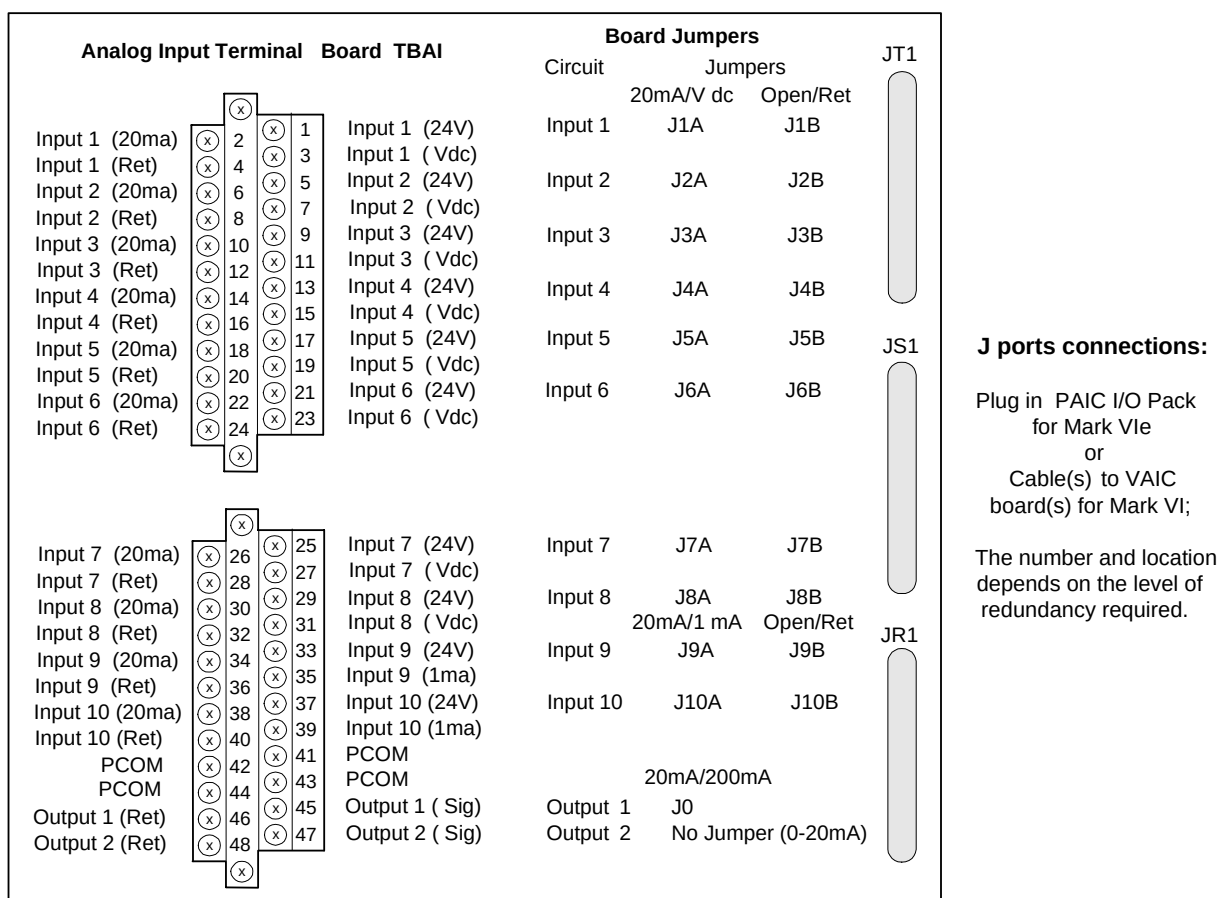
## Installation

Connect the input and output wires directly to two I/O terminal blocks mounted on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal attachment point is located adjacent to each terminal block.

TBAI can accommodate the following analog I/O types:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage  $\pm 5$  V,  $\pm 10$  V dc
- Analog output, 0-20 mA
- Analog output, 0-200 mA

The following diagram shows the wiring connections, jumper positions, and cable connections for TBAI.



TBAI Terminal Board Wiring

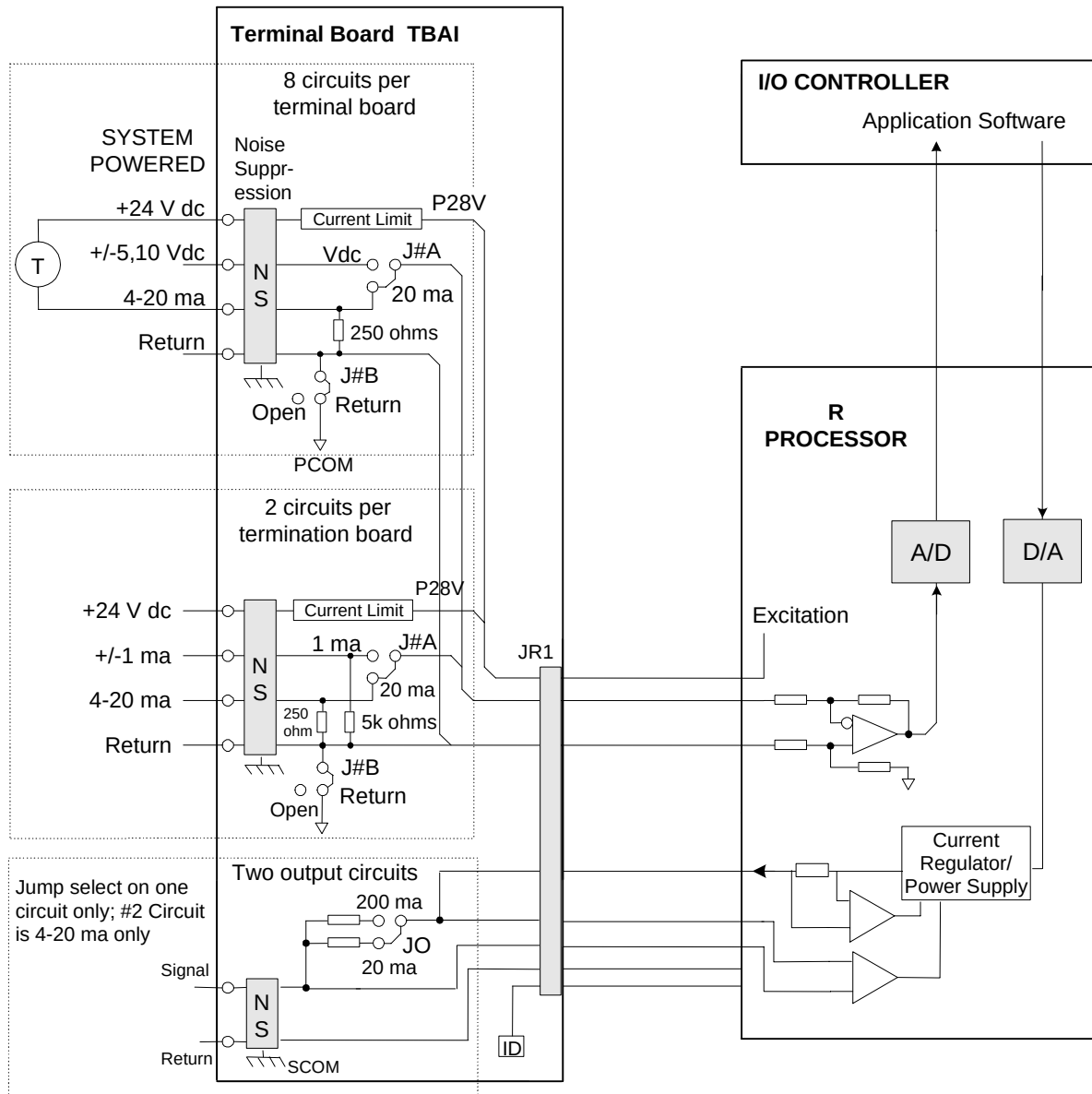
## Operation

TBAI provides a 24 V dc power source for all the transducers. The inputs can be configured as current or voltage inputs using jumpers (J#A and J#B). One of the two analog output circuits is 4-20 mA and the other can be configured as 4-20 mA or 0-200 mA. The following table displays the analog I/O capacity of TBAI.

| Quantity | Analog Input Types                         | Quantity | Analog Output Types |
|----------|--------------------------------------------|----------|---------------------|
| 8        | $\pm 10$ V dc, or $\pm 5$ V dc, or 4-20 mA | 1        | 0-20 mA or 0-200 mA |
| 2        | 4-20 mA, or $\pm 1$ mA                     | 1        | 0-20 mA             |

**Note** With the noise suppression and filtering, the input ac CMR is 60 dB, and the dc CMR is 80 dB.

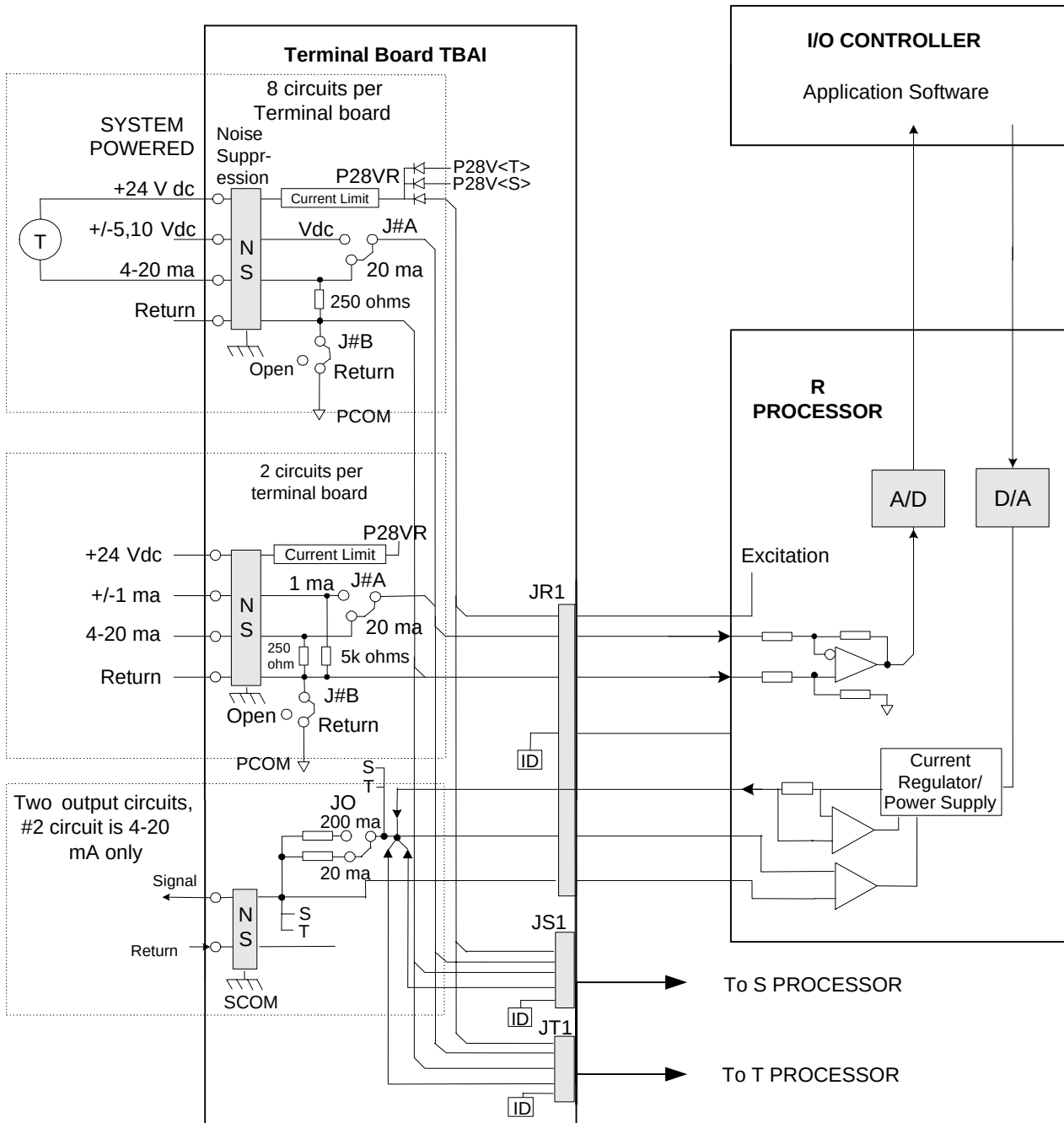
Each 24 V dc power output is rated to deliver 21 mA continuously and is protected against operation into a short circuit. Transmitters/transducers can be powered by the 24 V dc source in the control system, or can be independently powered. Jumper JO selects the type of current output. Diagnostics monitor each output and a suicide relay in the I/O controller disconnects the corresponding output if a fault cannot be cleared by a command from the processor.



Simplex Analog Inputs and Outputs



In a TMR system, analog inputs fan out to the three I/O controllers (VAIC or PAIC). The 24 V dc power to the transducers comes from all three controllers and is diode shared on TBAI. Each analog current output is fed by currents from all three controllers. The actual output current is measured with a series resistor, which feeds a voltage back to each I/O controller. The resulting output is the voted middle value (median) of the three currents. The following figure shows TBAI in a TMR system.



Analog Inputs and Outputs, TMR

## Specifications

| Item                     | Specification                                                                                                                                                                                  |
|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels       | 12 channels (10 AI, 2 AO)                                                                                                                                                                      |
| Input span, transmitters | 1-5 V dc from 4-20 mA current input                                                                                                                                                            |
| Outputs                  | 24 V outputs provide 21 mA each connection                                                                                                                                                     |
| Maximum lead resistance  | 15 $\Omega$ maximum two-way cable resistance, cable length up to 300 m (984 ft)                                                                                                                |
| Output load              | 500 $\Omega$ for 4-20 mA output, TBAIH1B with VAICH1C<br>800 $\Omega$ for 4-20 mA output, TBAIH1C with VAICH1D<br>800 $\Omega$ for 4-20 mA output, TBAIH1C with PAIC<br>50 $\Omega$ for 200 mA |
| <b>Physical</b>          |                                                                                                                                                                                                |
| Fault detection          | Monitor total output current<br>Check connector ID chip for hardware incompatibility                                                                                                           |
| Temperature              | -30 to 65°C (-22 to +149 °F)                                                                                                                                                                   |
| Size                     | 10.16 cm wide x 33.02 cm high ( 4.0 in x 13 in)                                                                                                                                                |

## Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

The terminal board is configured by jumpers. For the location of these jumpers, refer to the installation diagram. The jumper choices are as follows:

- Jumpers J1A through J8A select either current input or voltage input.
- Jumpers J1B through J8B select whether the return is connected to common or is left open.
- Jumpers J9A and J10A select either 1 mA or 20 mA input current.
- Jumpers J9B and J10B select whether the return is connected to common or is left open.
- Jumper J0 sets output 1 to either 20 mA or 200 mA.

---

# ***STAI Simplex Analog Input***

## ***Functional Description***

The Simplex Analog Input (STAI) terminal board is a compact analog input terminal board that accepts 10 analog inputs and two analog outputs, and connects to the PAIC pack. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The two analog outputs are 0-20 mA but one can be jumper configured to 0-200 mA current. Only a simplex version of the board is available.

High-density Euro-block type terminal blocks are used. An on-board ID chip identifies the board to the PAIC for system diagnostic purposes.

## ***Mark VIe Systems***

In Mark\* VIe systems, the PAIC I/O pack works with the STAI. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet. Only simplex systems are supported.

All revisions of STAI are compatible with all PAICs.

## ***Installation***

The STAI plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN-rail. Optionally, the STAI plus insulator mounts on a sheet metal assembly and then bolts directly to a cabinet. There are two types of Euro-block terminal blocks available as follows:

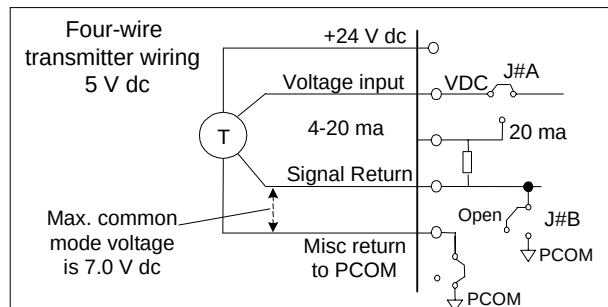
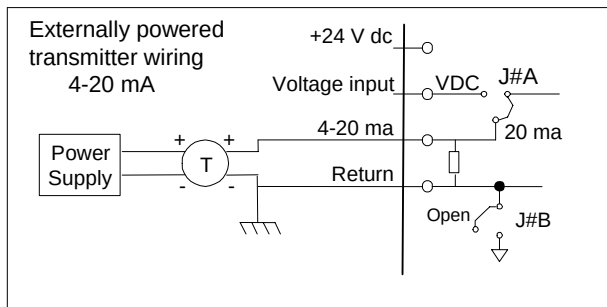
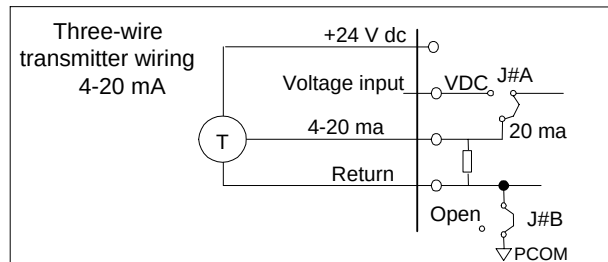
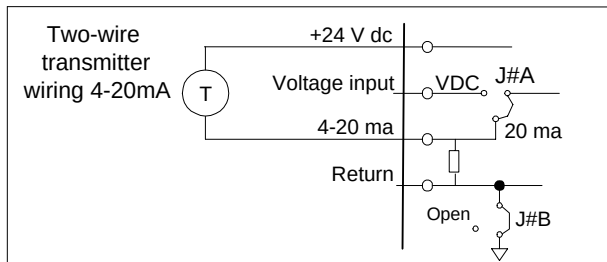
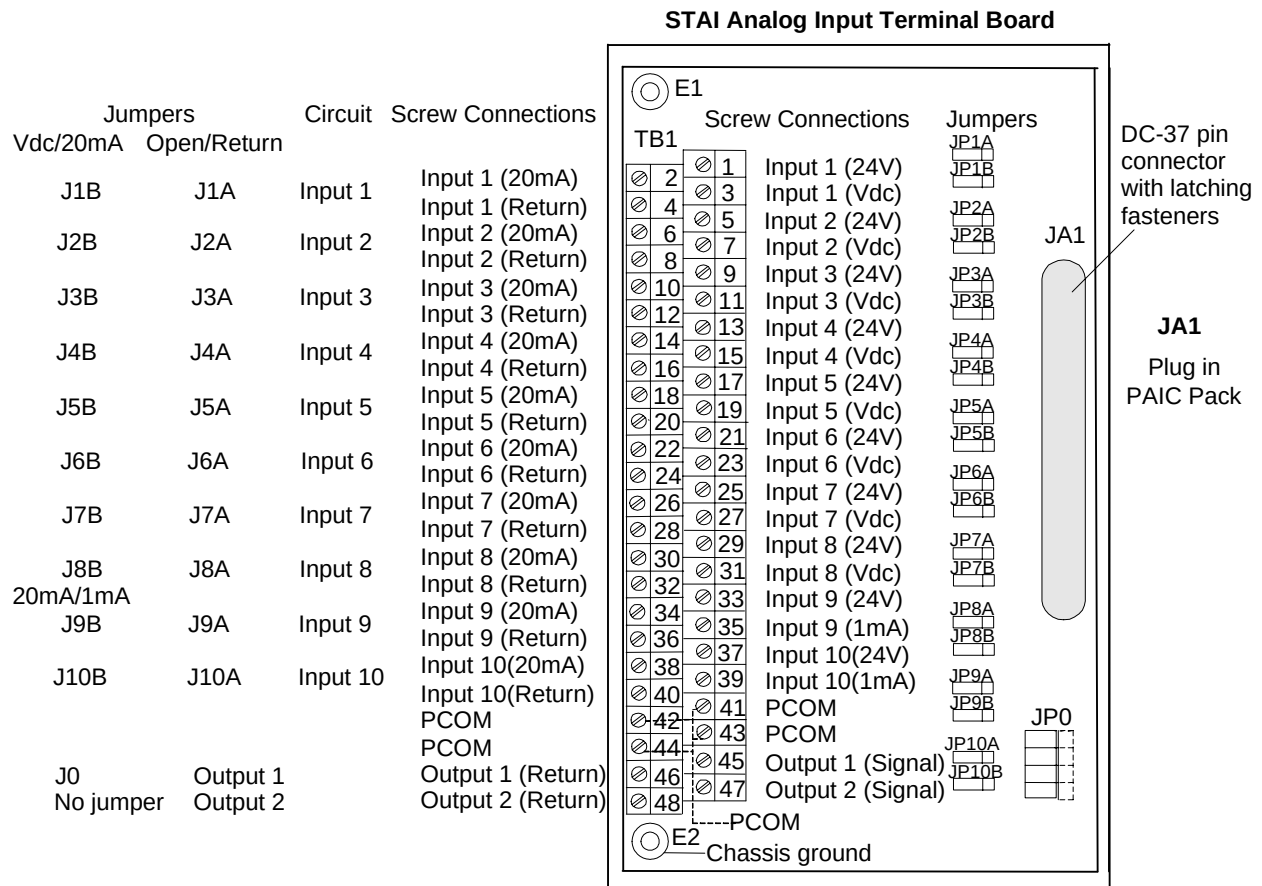
- STAIH1 has a permanently mounted terminal block with 48 terminals
- STAIH2 has a right angle header accepting a range of commercially available pluggable terminal blocks, with a total of 48 terminals

Typically #18 AWG wires (shielded twisted pair) are used. I/O cable shield terminal is provided adjacent to the terminal blocks.

The following types of analog inputs and outputs can be accommodated:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage  $\pm 5$  V,  $\pm 10$  V dc
- Analog output, 0-20 mA current
- Analog output, 0-200 mA current

Wiring, jumper positions, and cable connections appear on the wiring diagram.



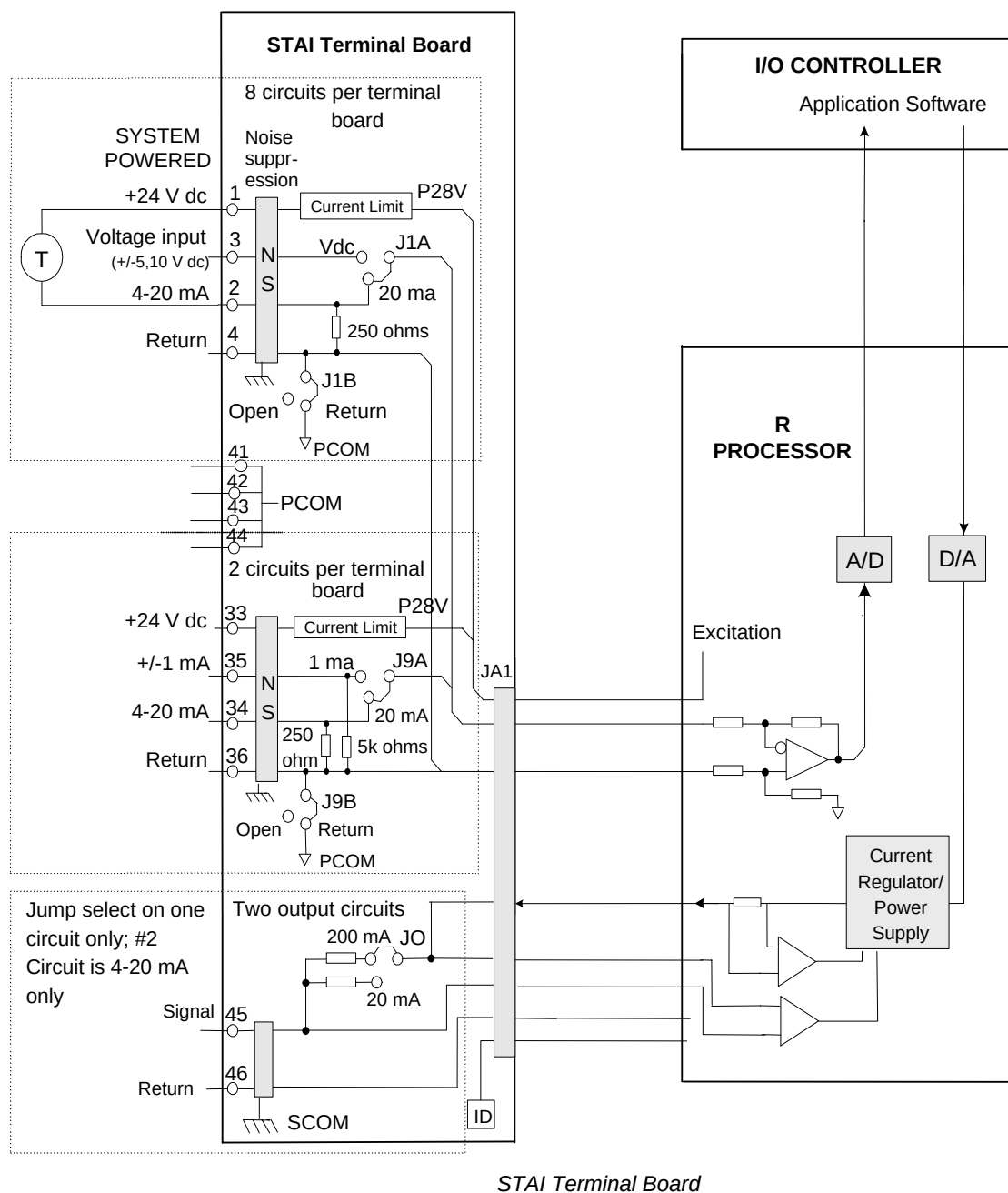
STAI Wiring, Cabling, and Jumper Positions

## Operation

24 V dc power is available on the terminal board for all the transmitters (transducers). There is a choice of current or voltage inputs using jumpers. One of the two analog output circuits is 4-20 mA, and the other can be jumper configured for 4-20 mA or 0-200 mA. There is only one cable connection, so the terminal board cannot be used for TMR applications as with TBAI.

The following table displays the analog input/output capacity of the STAI terminal board.

| Quantity | Analog Input Types                         | Quantity | Analog Output Types  |
|----------|--------------------------------------------|----------|----------------------|
| 8        | $\pm 10$ V dc, or $\pm 5$ V dc, or 4-20 mA | 1        | 0-20 mA, or 0-200 mA |
| 2        | 4-20 mA, or $\pm 1$ mA                     | 1        | 0-20 mA              |



## Specifications

| Item                     | Specification                                                                                 |
|--------------------------|-----------------------------------------------------------------------------------------------|
| Number of channels       | 12 channels (10 AI, 2 AO)                                                                     |
| Input span, transmitters | 1 - 5 V dc across a precision resistor (usually 250 $\Omega$ )                                |
| Maximum lead resistance  | 15 $\Omega$ maximum two-way cable resistance, cable length up to 300 m (984 ft).              |
| Outputs                  | 24 V dc outputs rated at 21 mA each                                                           |
| Load on output currents  | 800 $\Omega$ burden for 4-20 mA output with PAIC pack<br>50 $\Omega$ burden for 200 mA output |
| <b>Physical</b>          |                                                                                               |
| Size                     | 15.9 cm high x 10.2 cm wide (6.25 in. x 4.0 in.)                                              |
| Temperature              | -30 to +65°C (-22 to +149 °F)                                                                 |
| Technology               | Surface mount                                                                                 |

## Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

The terminal board is configured by jumpers. For the location of these jumpers, refer to the installation diagram. The jumper choices are as follows:

- Jumpers J1A through J8A select either current input or voltage input.
- Jumpers J1B through J8B select whether the return is connected to common or is left open.
- Jumpers J9A and J10A select either 1 mA or 20 mA input current.
- Jumpers J9B and J10B select whether the return is connected to common or is left open.
- Jumper J0 sets output 1 to either 20 mA or 200 mA.

# ***PAMB Acoustic Monitoring Input***

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## ***PAMB Acoustic Monitoring Input***

### ***Functional Description***

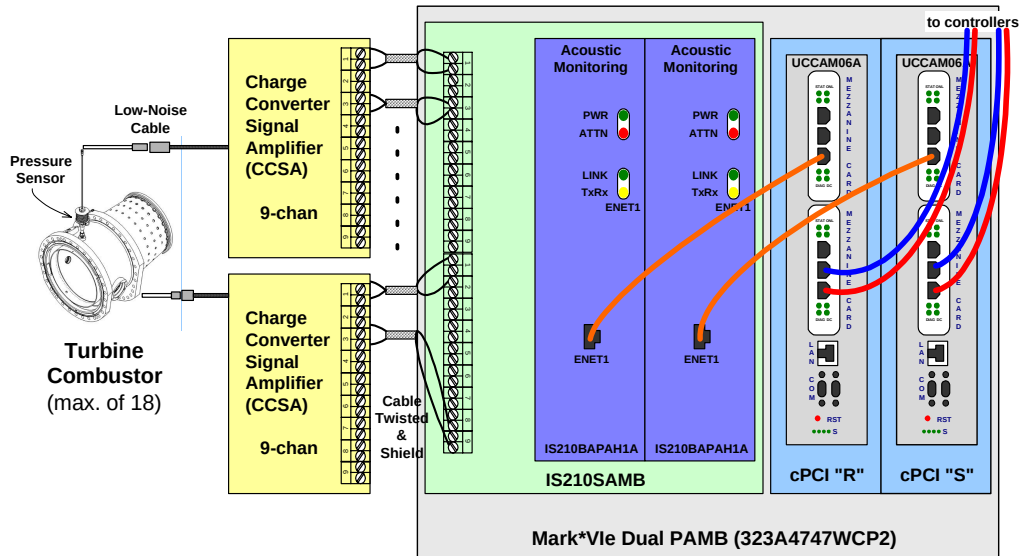
The Mark\* VIe Acoustic Monitoring Input (PAMB) pack supports combustion dynamics for all frame 6, 7, and 9 gas turbines. The PAMB I/O module includes the IS215BAPAH1A Analog Processor (BAPA) and the Acoustic Monitoring (SAMB) terminal board grouped together as an application subassembly, and the IS215UCCAM06A CompactPCI<sup>®</sup> (CPCI) processor module.

PAMB accepts dynamic pressure data from SAMB. The analog signal is conditioned to remove dc bias and amplify ac content (to maximize resolution) before it is digitized by an analog-to-digital (A/D) converter. A field programmable gate array (FPGA) sequences, digitizes, and filters the dynamic pressure signals and controls the high-speed serial link (HSSL) protocol for the Ethernet link between the BAPA and UCCA.

The UCCA, which mounts in a CPCI rack, is a LAN module that serves as the PAMB processing engine. The UCCA was selected for acoustic monitoring because it provides the additional processing capacity required for the fast fourier transform (FFT) analysis, sorting function, proprietary algorithms, sensor diagnostics, and so on.

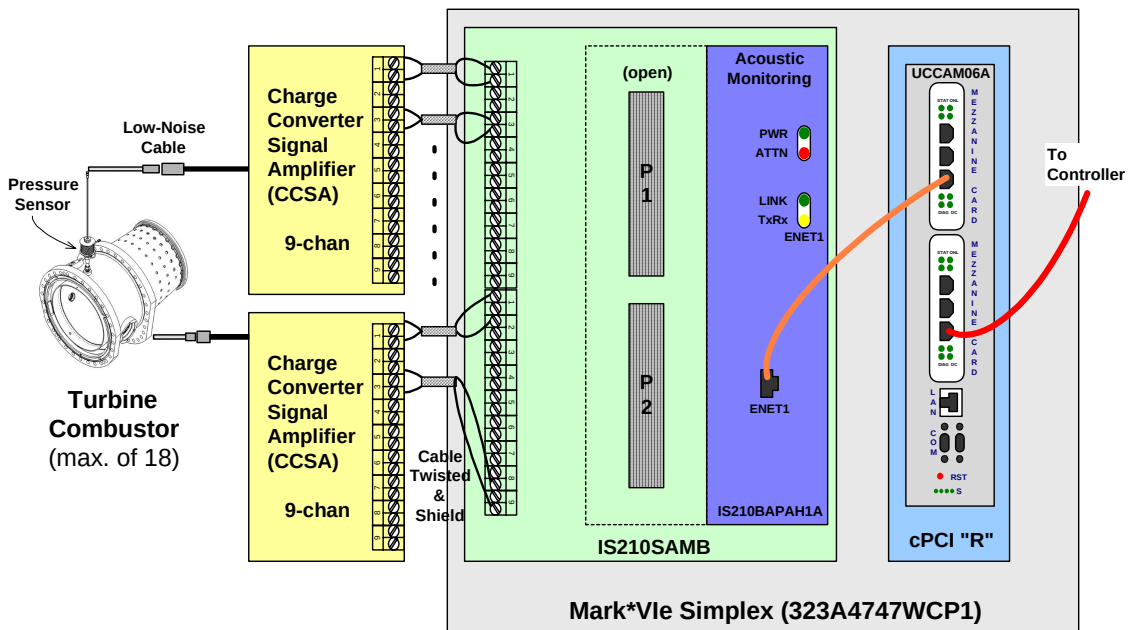
Two versions of the Acoustic Monitoring System are offered, as follows:

- **Dual Acoustic Monitoring System (323A4747WCP2)**. SAMB fans all 18 inputs to each PAMB. PAMB 1 (left) communicates with the UCCA connected to IONet R. PAMB 2 (right) communicates with the UCCA connected to IONet S. The controller's application code votes which PAMB data to use, based on the signal health.



*Dual Acoustic Monitoring System Overview*

- **Simplex Acoustic Monitoring System (323A4747WCP1)** – Simplex version of 323A4747WCP2. Controller application code is not required to vote signals from PAMB.



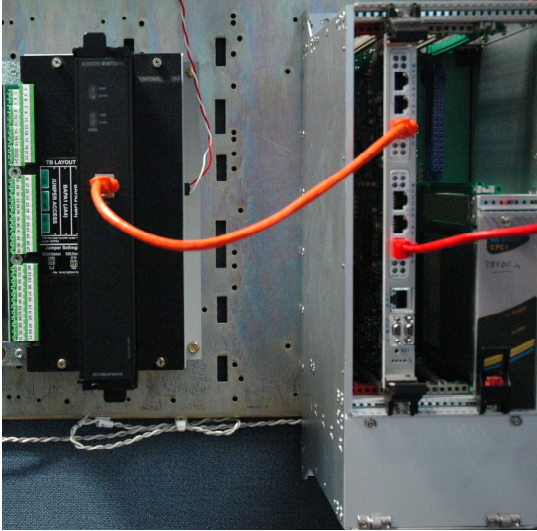
*Simplex Acoustic Monitoring System Overview*



# Compatibility

PAMBH1A is compatible with the following acoustic monitoring terminal boards:

| Terminal Board SAMBH1A                                                                                                                                                                                                                            |               |            |          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|------------|----------|
| Control Mode                                                                                                                                                                                                                                      | Simplex - Yes | Dual - Yes | TMR - No |
| <ul style="list-style-type: none"><li>Simplex uses one I/O pack with one or two network connections.</li><li>Dual uses two I/O packs with one network connection.</li><li>TMR uses three I/O packs with one network connection on each.</li></ul> |               |            |          |



Simplex PAMB Mounted on SAMB Terminal Board

## Installation

A GE field service technician should install the PAMB. Technicians should refer to Support Central website *Acoustic Monitoring Module (PAMB) Installation* in a Mark VIe Control, for complete installation instructions.

See *Installation* in the SAMB section of this document for installation instructions for the SAMB terminal board and dynamic pressure inputs.

## Operation

The PAMB includes the following features.

- Signal conditioning for up to 18 combustion dynamic pressure inputs:
  - GE Energy Charge-Converter Signal Amplifier (CCSA) or Piezotronics<sup>®</sup> sensors for heavy-duty turbines are supported
  - Differential inputs and adjustable gains
  - Fast synchronous-sampled A/D with 16x over-sampling
  - FPGA pre-processor with finite impulse response (FIR) filters
  - Open wire detection
- Analysis capability per channel:
  - Windowed FFT analysis
  - Rolling average per bin
  - 50/60 Hz rejection filters
  - Sort function providing peak pressure amplitude for six different frequency bands
  - Maximum peak detect for each frequency band
  - Average channel peak-to-peak amplitudes per frequency band
  - Alarm detection if peak-to-peak amplitude exceeds configurable level for each frequency band
  - List capture for all 18 channels if alarm is detected or user requests capture
  - Proprietary functions

## Processor

The processor module contains a CPCI processor board (IS200UCCAH1A), an Ethernet-based IONet communication mezzanine board (IS200EPMCH1A), and one HSSL Ethernet mezzanine board (IS200EPMCH3A). It contains the following:

- High-speed processor with random access memory (RAM) and flash memory
- Six fully-independent 10/100 Ethernet ports with connectors
- Two universal asynchronous receiver-transmitter (UART) type serial ports with connectors
- Hardware watchdog timer and reset circuit
- Status-indication LEDs
- Electronic ID
- Compact flash support

UCCA connects to BAPA through the HSSL interface. The PAMB is designed so that the UCCA and the BAPA can be located in different locations. Each module can be powered independently. At power up, the BAPA waits for UCCA to initiate communications. After communication is established, the application FPGA is programmed.

The processor application code contains the logic to allow PAMB to operate on one or two IONet inputs. When using two IONet inputs, both network paths are active at all times. A failure of either network will not disturb I/O pack operation and will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system in which the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

## ***Analog Processor***

The analog processor includes the following features:

- Eighteen analog signal-conditioning channels
  - Differential inputs
  - Adjustable gains of 1x, 2x, 4x, and 8x
  - Dc bias nulling
  - Multiplexer to bypass signal input and apply test signal
  - Anti-alias filters to support 5 kHz bandwidth
- Twenty-four A/D input channels
  - Six channels per converter
  - 16-bit converter
- Application FPGA
  - A/D converter control
  - D/A converter control
  - Eighteen channels of FIR filtering
  - Configuration registers
  - HSSL control
- Boots FPGA with programmable read-only memory (PROM)
  - Bootstrap function
  - Tx / Rx mini-MACs
  - PHY sync
- PHY0 and PHY1 physical Ethernet layers
- Power supplies
  - P28 input
  - P15 and N15 outputs
  - P5 output
  - 3.3 V, 2.5 V, and 1.2 V outputs

## Acoustic Monitoring Firmware

The PAMC firmware supports 18 input channels. The main features are:

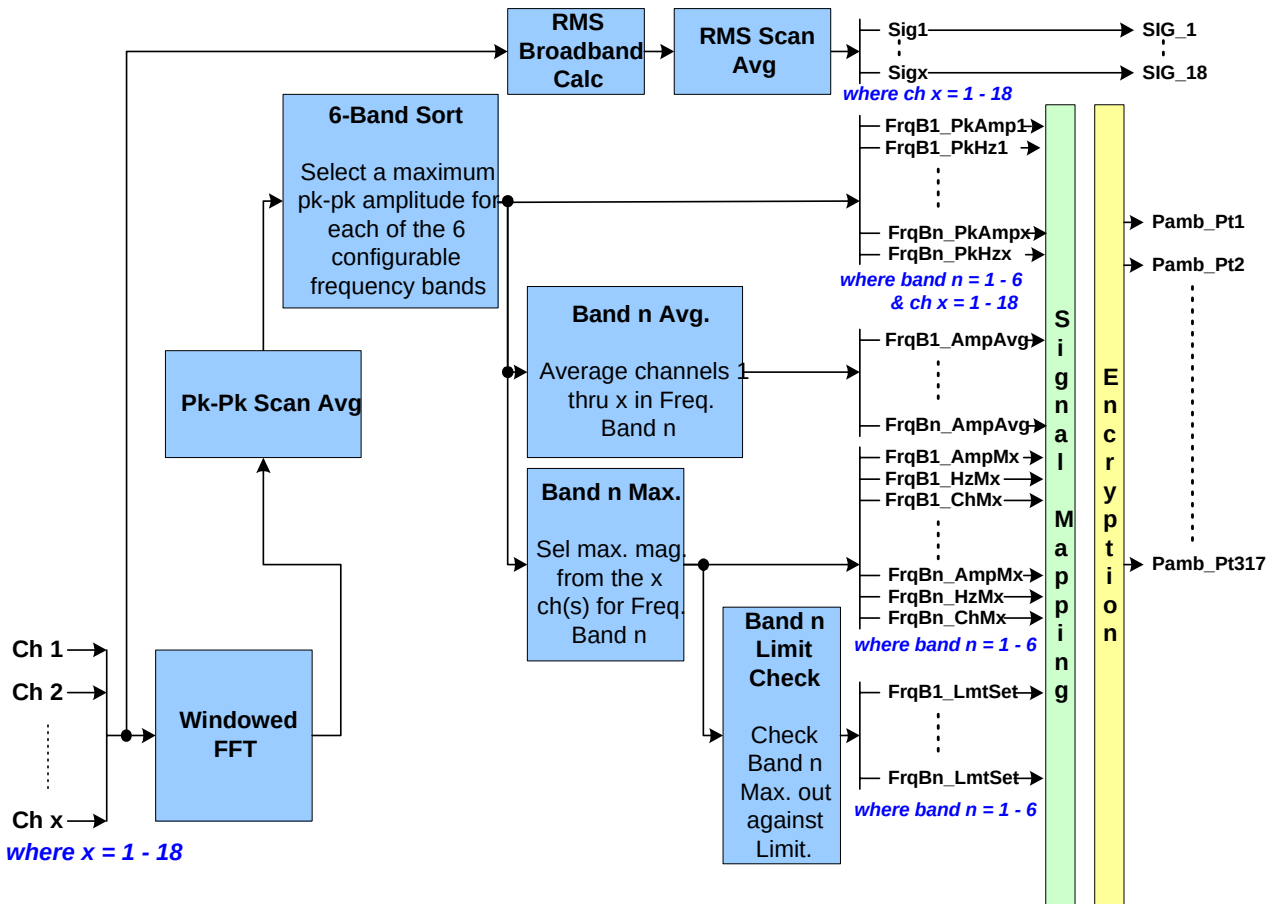
- **RMS Broadband Calculation** – Calculates the broadband root-mean-square (RMS) energy of the time-domain sampled data in the frequency range of 0 to 5000 Hz. The output is the input of the RMS Scan Average.
- **RMS Scan Average** – Average multiple scans of broadband RMS values. A scan is defined by the amount of time-domain sampled combustion data to calculate a windowed FFT of some defined length. The output is the system input, SIGx (where x is the channel number), passed to the controller.
- **Windowed FFT** – Calculates the frequency domain peak-to-peak magnitude and bin frequency, based on time-domain sampled combustion input data. The configuration defines the type of FFT window function used, the FFT length (amount of input data collected for the calculation), and the sample frequency. The output feeds the Peak-to-Peak Scan Average.
- **Peak-to-Peak Scan Average** – Provides a frequency domain peak-to-peak magnitude average per frequency bin, over multiple scans. The configuration defines the number of scans used in the rolling average calculation. The output is the input for the Six-Band Sort function.
- **Six-Band Sort** – Average frequency domain peak-to-peak data is sorted into six separate frequency bands, as displayed in the following table.

*Frequency Bands*

| Freq Band # | Configuration Band Name |
|-------------|-------------------------|
| 1           | Low (Low)               |
| 2           | Middle (Mid)            |
| 3           | High (High)             |
| 4           | Low Low (LoLo)          |
| 5           | Trans (Trns)            |
| 6           | Screech (Scrch)         |

The maximum of the average peak-to-peak magnitudes from each frequency band and its corresponding frequency bin are selected and output as system inputs for the controller.

- **Band n Average** – Calculates the average peak-to-peak magnitude over all enabled healthy input channels, based on the output of the Six-Band Sort.
- **Band n Maximum** – Calculates the maximum peak-to-peak magnitude over all input channels enabled, based on the Six-Band Sort data. The six frequency band maximums are output for use by the controller.
- **Band n Limit Check** – A frequency band limit check based on the Band n Maximum output data.



Acoustic Monitoring Block Diagram

### A/D Compensation

The A/D compensation function eliminates any gain or offset error due to initial component inconsistency. An auto-calibration function executes each time the module is reset. The auto-calibration function compares each of the 18 analog channels against a standard A/D channel. This A/D channel is calibrated using a standard high-precision voltage reference and the A/D common.

## ***Input Units to Engineering Value Conversion***

The Acoustic Monitoring System converts the hardware input units to the engineering units (EU) needed for the system calculation. For the conversion of mV to psi, the range is 20 to 600 mV per psi. Four configuration parameters are provided per channel to define the equation for the transfer function.

$$\text{Value (EU in counts)} = \text{GUnitConversion} * \text{Input (millivolts in counts)} + \text{Offset}$$

where

$$\text{GUnitConversion} = (\text{High\_Value} - \text{Low\_Value}) / (\text{High\_Input} - \text{Low\_Input})$$

$$\text{Offset} = \text{High\_Value} - \text{GUnitConversion}_n * \text{High\_Input}$$

where High\_Value, Low\_Value, High\_Input + Low Input are the configuration parameters.

## ***A/D Gain Adjust***

The configuration parameter, Gain, controls the channel gain in the hardware. This parameter is defined for each channel. This allows low-level signals to be amplified to provide better resolution in the A/D conversion hardware. The gain options are 1x, 2x, 4x, and 8x. The channel control writes the gain setup to the FPGA input amplifier 4x and 2x gain control registers. The signal level calculated by PAMC firmware does not change with the Gain parameter because the signal is divided by the gain factor in the firmware, resulting in a net gain of 1 for the signal regardless of the gain factor used. The maximum expected signal level should not exceed 10 V (saturation) after the gain is applied as indicated in the following table.

*Rules for Selecting Gain Value*

| <b>Gainx</b> | <b>Maximum magnitude of input signal after dc bias is removed (volts)</b> |
|--------------|---------------------------------------------------------------------------|
| 1            | 10                                                                        |
| 2            | 5                                                                         |
| 4            | 2.5                                                                       |
| 8            | 1.25                                                                      |

## ***RMS Calculation and Rolling Average***

The RMS calculation function performs an RMS calculation on the ac acoustic information sampled for a given scan. The RMS is defined as follows:

$$\text{rms\_Chx} = \text{SQRT} ( (\text{AC\_Input}(0)**2 + \text{AC\_Input}(1)**2 + \dots + \text{AC\_Input}(\text{Buffer\_Length})**2) / \text{Buffer\_Length} )$$

Where x is the channel number.

The rolling average function provides a smoothing function to reduce the vibration in the signal.

## Capture Lists

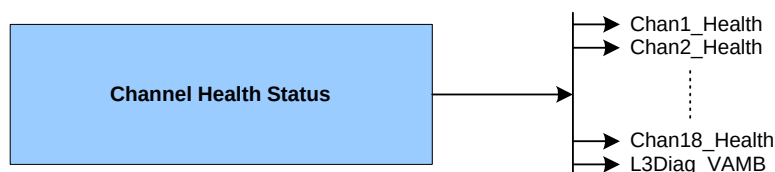
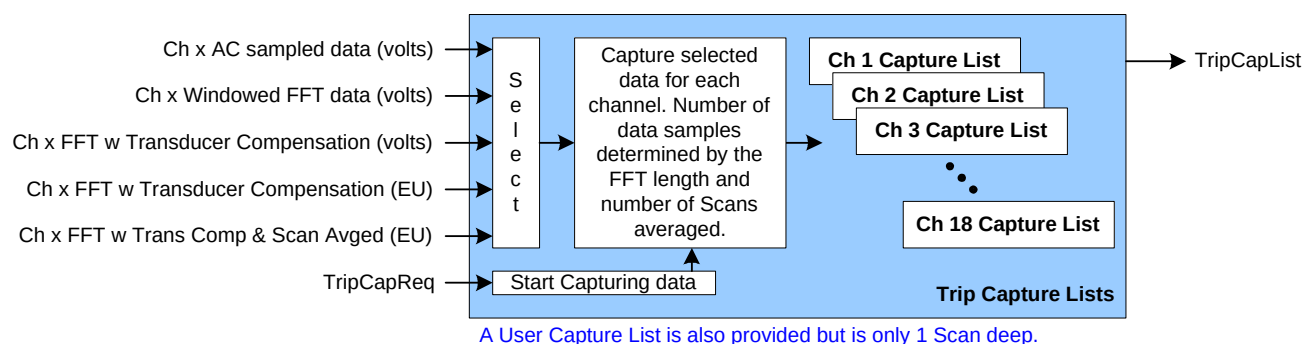
Two capture lists are available, as follows:

- **Trip Capture Lists** – This function provides circular buffers that input internally calculated data, which is selected based on a configuration parameter. The circular buffers can capture up to 32 scans of information for each of 18 channels. The following internal data can be captured:
  - Time-domain sampled input data (in volts)
  - Frequency-domain FFT peak-to-peak magnitude (in volts)
  - FFT output data with transducer compensation (in volts)
  - FFT output data with transducer compensation (in EU)
  - Scan-averaged FFT output data with transducer compensation (in EU)

Trip Capture Lists are *pre-triggered*, meaning for a 32 scan FFT average, data is scanned 32 times before the triggered event and none after the event. The triggered event is activated by the signal space input, *TripCapReq*. Running on the HMI or OSM computer, AM Gateway software uploads the captured lists and transfers the data to the Atlanta Remote DLN Tuning Center for analysis.

- **User Capture Lists** – This function provides circular buffers that are only one scan in length (compared to the Trip Capture, with 32 scan buffers). The User Capture buffers can input the same internal data as the Trip Capture buffers. The AM Gateway software can upload these lists. User capture lists are activated through the AM Gateway or other compatible applications.

## PAMB Acoustic Monitoring Diagnostic Support



*PAMB Acoustic Monitoring Diagnostic Support*

## Specifications

| Item                                                                                                                               | Specification                                                                                                                                                                                                          |
|------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input channels                                                                                                                     | 18 dynamic pressure inputs                                                                                                                                                                                             |
| Output channels                                                                                                                    | 18 buffered outputs                                                                                                                                                                                                    |
| Gain adjustment options                                                                                                            | 1x, 2x, 4x, and 8x                                                                                                                                                                                                     |
| Bias – minimum adjust                                                                                                              | -13.5 $\pm$ 0.25 V dc                                                                                                                                                                                                  |
| Bias – maximum adjust                                                                                                              | +13.5 $\pm$ 0.25 V dc                                                                                                                                                                                                  |
| Input accuracy from terminal point to inputs, SIGx for passband = 0 to 5 kHz                                                       | $\leq 2.0$ % of full scale = 10 V dc for Gain = 1x<br>$\leq 2.0$ % of full scale = 5 V dc for Gain = 2x<br>$\leq 2.0$ % of full scale = 2.5 V dc for Gain = 4x<br>$\leq 2.0$ % of full scale = 1.25 V dc for Gain = 8x |
| Input accuracy (dc + ac) from terminal point to peak-peak signal –space values through FFT analysis for passband = 0 to 3.2 kHz    | $\leq 0.5$ % of full scale = 10 V dc for Gain = 1x<br>$\leq 0.5$ % of full scale = 5 V dc for Gain = 2x<br>$\leq 0.5$ % of full scale = 2.5 V dc for Gain = 4x<br>$\leq 0.5$ % of full scale = 1.25 V dc for Gain = 8x |
| Input accuracy (dc + ac) from terminal point to peak-peak signal-space values through FFT analysis for passband = 3.2 kHz to 5 kHz | $\leq 2.0$ % of full scale = 10 V dc for Gain = 1x<br>$\leq 2.0$ % of full scale = 5 V dc for Gain = 2x<br>$\leq 2.0$ % of full scale = 2.5 V dc for Gain = 4x<br>$\leq 2.0$ % of full scale = 1.25 V dc for Gain = 8x |
| Input passband frequency                                                                                                           | 0 to 5 kHz                                                                                                                                                                                                             |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board ID to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- Each input has sensor limit checking, open circuit detection, dc bias autonulling, and excessive dc bias detection. Alarms are generated for these diagnostics. Refer to the tables *I/O Pack Alarms* and *Point Configuration*. *RESET\_SYS* resets these alarms.

Details of the individual diagnostics are available in the ToolboxST\* application. The diagnostic signals can be individually reset with *RESET\_DIA* if they go healthy.



## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Module Parameter | Description (Point Level Configuration)                                                                                                                                                                                                                                                        | Choices                              |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| BinReject        | Defines the number of side bins that will be rejected when the search function is applied to the FFT results for channels 1 – 18.0 = no bins rejected                                                                                                                                          | 0 to 6                               |
| Config_Mode      | Defines the source of the currently active configuration. ToolboxST allows only mode toolbox as a selection. The remote gateway configurator forces mode to tuning configurator without user control.                                                                                          | ToolboxST only                       |
| E_Bnds_Vis       | Enables visibility of the parameters associated with the energy bands processing. This visibility is restricted to authorized GE personnel and requires the correct code to enable visibility.                                                                                                 | 0 to 2147483647                      |
| FFT_Length       | Defines the number of samples that will be used in FFT calculation                                                                                                                                                                                                                             | 1024, 2048, 4096, 8192, 16382, 32768 |
| FFT_TF_SelA      | Boolean that selects the internal test file as the input to all acoustic monitoring channels instead of the actual analog input signals                                                                                                                                                        | HW_Input to File                     |
| EventLstSel      | Defines the sample site for the event capture list:<br>Disable: list not used<br>FFT_Out: FFT output scaled in volts<br>TC_Out: FFT output after transducer compensation<br>PSI_Out: FFT outputs scaled in PSI<br>Avg_Out: PSI_Out after averaging filter<br>Raw_Input: Input time domain data | Disable to Avg_Out                   |
| HiB_Limit        | Defines the limit for the max peak-peak amplitude signal in the high frequency band                                                                                                                                                                                                            | 0 to 50 psi                          |
| HiScrChBrkPt     | Defines the frequency boundary between the high and screech frequency bands                                                                                                                                                                                                                    | 0 to 3200 Hz                         |
| LoLoB_Limit      | Defines the limit for the max peak-peak amplitude signal in the low-low frequency band                                                                                                                                                                                                         | 0 to 50 psi                          |
| LowB_Limit       | Defines the limit for the max peak-peak amplitude signal in the low frequency band                                                                                                                                                                                                             | 0 to 50 psi                          |
| LowLow_EndPt     | Defines the ending frequency of the low-low frequency band                                                                                                                                                                                                                                     | 0 to 5000 Hz                         |
| LowLowStrtPt     | Defines the starting frequency of the low-low frequency band                                                                                                                                                                                                                                   | 0 to 5000 Hz                         |
| LowMid_BrkPt     | Defines the frequency boundary between low and mid frequency bands                                                                                                                                                                                                                             | 0 to 5000 Hz                         |
| Low_StrtPt       | Defines the starting frequency of the low band                                                                                                                                                                                                                                                 | 0 to 5000 Hz                         |
| MaxVoltCCSA      | Max sensor volts for a CCSA type sensor                                                                                                                                                                                                                                                        | -30 to 30 V                          |
| MaxVoltCustm     | Max sensor volts for a custom type sensor                                                                                                                                                                                                                                                      | -30 to 30 V                          |
| MaxVoltPCB       | Max sensor volts for a PCB type sensor                                                                                                                                                                                                                                                         | -30 to 30 V                          |
| MidB_Limit       | Defines the limit for the max peak-peak amplitude signal in the mid frequency band                                                                                                                                                                                                             | 0 to 50 psi                          |
| MidHi_BrkPt      | Defines the frequency boundary between mid and high frequency bands                                                                                                                                                                                                                            | 0 to 5000 Hz                         |
| MinVoltCCSA      | Minimum sensor volts for a CCSA type sensor                                                                                                                                                                                                                                                    | -30 to 30 V                          |
| MinVoltCustm     | Minimum sensor volts for a custom type sensor                                                                                                                                                                                                                                                  | -30 to 30 V                          |
| MinVoltPCB       | Minimum sensor volts for a PCB type sensor                                                                                                                                                                                                                                                     | -30 to 30 V                          |
| NumEventScns     | Defines the number of scans an event buffer contains*Note. If the sample location is Raw_Input the max scan allowed is 1.                                                                                                                                                                      | 1 to 32 scans                        |

| Module Parameter                | Description (Point Level Configuration)                                                                                                                                                                                                                                                                           | Choices                 |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|
| OpLstSel                        | Defines sample site for spectrum on demand capture or diagnostic list:<br>Disable: list not used<br>Raw_Input: input time domain data<br>FFT_Out: FFT output scaled in volts<br>TC_Out: FFT output after transducer compensation<br>PSI_Out: FFT outputs scaled in PSI<br>Avg_Out: PSI_Out after averaging filter | Disable to Avg_Out      |
| PL_Fil_Freq                     | Defines the power line frequency that the notch filter will remove from the spectral content of the FFT output                                                                                                                                                                                                    | 50 or 60 Hz             |
| PL_Fil_Tol                      | Power line filter signature tolerance calculated vs theoretical. 10% = 0.1.                                                                                                                                                                                                                                       | 0 to 1.0                |
| PL_Fil_Width                    | Defines the bandwidth of the power line notch filter. The bandwidth will be $\pm$ value centered about the configured power line frequency.                                                                                                                                                                       | 0 to 100 Hz             |
| SampleRate                      | Defines the FFT sample rate for all the acoustic monitoring channels                                                                                                                                                                                                                                              | 12,877 Hz only          |
| ScanPrAvgFFT                    | Number of scans per average in acoustic monitoring filtered FFT output                                                                                                                                                                                                                                            | 1 to 32 scans           |
| ScanPrAvgRMS                    | Number of scans per average in the RMS calculation                                                                                                                                                                                                                                                                | 1 to 32 scans           |
| SearchInAvg(1) – SearchInAvg(6) | Selects whether the sort function for pk-pk amplitudes uses the present scan or an average value                                                                                                                                                                                                                  | No average, Average     |
| Session_Time                    | Scheduled time for temporary configuration mode. This time is forced to zero in the ToolboxST entry. This value is set to the user-selected time in the temporary gateway remote configurator.                                                                                                                    | 0                       |
| ScrchB_Limit                    | Defines the limit level for the maximum peak-peak amplitude signal in the screech frequency band                                                                                                                                                                                                                  | 0 to 50 psi             |
| Scrch_EndPt                     | Defines the ending frequency of the screech frequency band                                                                                                                                                                                                                                                        | 0 to 5000 Hz            |
| T_FilWidth                      | Width ( $\pm$ Hz) of the filter that excludes the transverse frequency FFT coefficients and all FFT coefficients designated by this filter from the screech band search                                                                                                                                           | 0 to 100 Hz             |
| TMC_Gain(1) – TMC_Gain(30)      | Transducer mounting compensation gain to characterize gain response                                                                                                                                                                                                                                               | 0 to 10                 |
| TMC_Freq(1) – MC_Freq(30)       | Frequency corresponding to the gain value entered                                                                                                                                                                                                                                                                 | 0 to 5000 Hz            |
| TrnsB_Limit                     | Defines the limit for the max peak-peak amplitude signal in the transverse frequency band                                                                                                                                                                                                                         | 0 to 50 Psi             |
| Trns_Bnd_Enb                    | Enable calculations associated with the transverse band and exclude its FFT coefficients from the screech band                                                                                                                                                                                                    | Disable, Enable         |
| Trns_EndPt                      | Defines the ending frequency of the transverse frequency band                                                                                                                                                                                                                                                     | 0 to 5000 Hz            |
| Trns_StrtPt                     | Defines the starting frequency of the transverse frequency band                                                                                                                                                                                                                                                   | 0 to 5000 Hz            |
| WindowSelect                    | Selects windowing function for sampled data for Channel A and B:<br>Rectangular<br>Hamming<br>Hanning<br>Triangular<br>Blackman<br>Blackman-Har(ris)<br>Flat Top                                                                                                                                                  | Rectangular to Flat Top |
| Gain                            | Analog input resolution adjustment to amplify signal before digital conversion. Gain factor * (maximum signal peak voltage) must be less than 10 V to prevent saturation.                                                                                                                                         | 1,2,4, 8 V / V          |
| Bias                            | Dc bias voltage subtracted from the analog signal input for dc bias compensation. Only used when InputUse is custom or file.                                                                                                                                                                                      | -11.6 to +11.6 V dc     |

| Module Parameter | Description (Point Level Configuration)                                                                                                                         | Choices                         |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|
| Bias_Range       | Allowable deviation of dc bias used for dc bias diagnostics. Only used when InputUse is custom or file.                                                         | -30 to 30 V                     |
| Can_Id           | Combustor can be wired to this terminal board signal. This normally corresponds to the signal number to avoid confusion; wire terminal board signal 1 to can 1. | 1 to 18                         |
| High_Input       | Defines point 2 X-axis value in mV for SAMB terminal point that is used to calculate gain and offset for conversion to EU                                       | 0 to 9998.8 mV                  |
| High_Value       | Defines point 2 Y-axis value in EU for SAMB terminal point that is used to calculate gain and offset for conversion from mV to EU                               | 0 to 99999 psi                  |
| InputUse         | Selects the sensor type used on the signal.                                                                                                                     | Unused, CCSA, PCB, Custom, File |
| Low_Input        | Defines point 1 X-axis value in mV for SAMB terminal point that is used to calculate gain and offset for conversion to EU                                       | 0 to 9998.8 mV                  |
| Low_Value        | Defines point 1 Y-axis value in EU for SAMB terminal point that is used to calculate gain and offset for the conversion from mV to EU                           | 0 to 99999 psi                  |
| PL_Fil_En        | Enables the power line notch filter                                                                                                                             | Disable, Enable                 |
| DiagHighEnab     | Enables high input sensor limit diagnostics                                                                                                                     | Disable, Enable                 |
| DiagLowEnab      | Enables low input sensor limit diagnostics                                                                                                                      | Disable, Enable                 |
| BiasNullEnab     | Enables automatic dc bias nulling                                                                                                                               | Disable, Enable                 |
| DiagOCChk        | Enables open sensor error diagnostic test                                                                                                                       | Disable, Enable                 |
| DiagBiasNull     | Enables excessive dc bias diagnostic test                                                                                                                       | Disable, Enable                 |
| DiagSigSat       | Enables signal saturation diagnostic test                                                                                                                       | Disable, Enable                 |

*PAMB Board Points*

| Board Points (Signals) | Description – Point Edit(Enter Signal Connection)               | Direction | Type    |
|------------------------|-----------------------------------------------------------------|-----------|---------|
| L3DIAG_PAMB            | Board Diagnostic active (non-voted signal)                      | Input     | BIT     |
| Can1_Health            | Combustor can 1 signal health                                   | Input     | BIT     |
| :                      | :                                                               |           |         |
| Can18_Health           | Combustor can 18 signal health                                  | Input     | BIT     |
| Test_Config            | Card is temporarily remotely configured                         | Input     | BIT     |
| Test_Mode              | Signals are from internal test sources, not from terminal board | Input     | BIT     |
| TripCapList            | A capture list triggered by TripCapReq is available             | Input     | BIT     |
| UserCapList            | A capture list manually requested by a user is available        | Input     | BIT     |
| PambBool_1             | General Electric Proprietary Information                        | Input     | BIT     |
| :                      | :                                                               |           |         |
| PambBool_6             | General Electric Proprietary Information                        | Input     | BIT     |
| PambPt_0               | General Electric Proprietary Information                        | Input     | INTEGER |
| :                      | :                                                               |           |         |
| PambPt_317             | General Electric Proprietary Information                        | Input     | INTEGER |
| Num_Of_Scans           | Scan (block of FFT data) number of this data (1 – 32)           | Input     | INTEGER |
| Num_Avg_Scns           | Number of scans (block of FFT data) averaged (1 – 32)           | Input     | INTEGER |
| Session_Tmr            | Time remaining for remote tuning session                        | Input     | INTEGER |
| TripCapReq             | Request for trip capture buffer collection                      | Input     | BIT     |

# Alarms

## PAMB Specific Alarms

| Alarm ID | Alarm Description                                                            | Possible Cause                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Solution |
|----------|------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 38       | Flashdisk error: Unable to revert to flash configuration after remote access | Permanent configuration data on card is corrupted. Download firmware to card or replace UCCA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |          |
| 41-58    | Chan x: Open circuit test failed                                             | Open circuit detected for terminal board signal Sig x, where x is the identified point. Check wiring and sensor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| 61-78    | Chan x: Bias nulling error                                                   | Dc bias designated for sensor type is outside of range detected for sensor. Check sensor type in configuration parameter InputUse or check dc bias voltage on signal.                                                                                                                                                                                                                                                                                                                                                                                                                                   |          |
| 81-98    | Chan x: Input signal saturated                                               | Peak input voltage is saturating input. Decrease configuration parameter Gain for designated signal or check for sensor problem.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |          |
| 101-118  | Chan x: Sensor limit exceeded                                                | Peak input voltage exceeds limit for selected sensor type. Check sensor type in configuration parameter InputUse or check for sensor problem.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |          |
| 120      | BAPA ADC reference input calibration failure                                 | BAPA failed calibration test at power up. Replace BAPA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |
| 121-138  | BAPA Chan x ADC calibration failure                                          | BAPA failed calibration test at power up. Replace BAPA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |
| 139-156  | BAPA Chan x DAC calibration failure                                          | BAPA failed calibration test at power up. Replace BAPA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |          |
| 212      | Communication failure with remote acquisition Link 1 Code x                  | The PAMB/UCCA cannot communicate with remote acquisition hardware (terminal board and BAPA) through the HSSL cable. Cable may be disconnected or connected to wrong device, the BAPA may be powered down or bad, or UCCA interface to the HSSL may be bad. Code indicates specific failure type. Common codes include:<br>51xxxxxx: Remote acquisition target returning bad id<br>52xxxxxx: Download to BAPA failed<br>53xxxxxx: Link loss detected<br>54xxxxxx: Receive packet error detected<br>55xxxxxx: Transmit packet error (excessive naks)<br>57xxxxxx: No data received from BAPA in 5 seconds |          |
| 213      | EPMC H3 missing or bad on link                                               | Top mezzanine (EPMC) card on UCCA is missing or bad.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |          |
| 214      | Serial Link 1 Configuration failure code x                                   | PAMB/UCCA failed to setup HSSL properly. Replace UCCA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |          |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                            |
|-------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                               |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                          |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                               |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                               |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                               |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                        |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                             |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                            |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                              |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                            |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                     |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                 |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                  |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                           |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                     |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                  |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                          |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                             |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                              |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                      |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                              |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                  |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ]P_Id= [ ], =Expctd= [ ], Rcvd= [ ]  | Message version mismatch                                                                                                                                  |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                             |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                               |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                  |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                             |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                               |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                           |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

## ***SAMB Acoustic Monitoring Input***

### ***Functional Description***

The Mark\* VIe Acoustic Monitoring (SAMB) terminal board is a dual terminal board providing 18 inputs for the Acoustic Monitoring System. SAMB provides two terminal points per input channel for a maximum of 18 channels on 36 terminals. It also provides an additional 18 buffered outputs on 36 terminals to connect external instrumentation for monitoring the ac voltage signal that represents the dynamic pressure signals from the combustor. SAMB includes passive electromagnetic interference (EMI) filters to protect against very high frequency noise generated by external sources.

SAMB includes the following features:

- Eighteen signal interface channels for acoustic monitoring, supporting dedicated-dual configuration
- Channels 1 – 9 are configurable to support PCB Piezotronics<sup>®</sup> sensors or charge converter signal amplifier (CCSA) outputs. Sensor power for the PCB sensors is independent of the sensor power for channels 10 – 18.
- Channels 10 – 18 are configurable to support PCB Piezotronics sensors or CCSA outputs. Sensor power for the PCB sensors is independent of the sensor power for channels 1 – 9.
- Eighteen buffered outputs providing ac signal content of the dynamic pressure signals without dc bias voltage
- Thirty-six Euro-style terminal points for the customer inputs
- Thirty-six Euro-style terminal points for the buffered outputs
- EMI protection for all inputs
- EMI filtered inputs fanned to the A and B slots

## ***Installation***

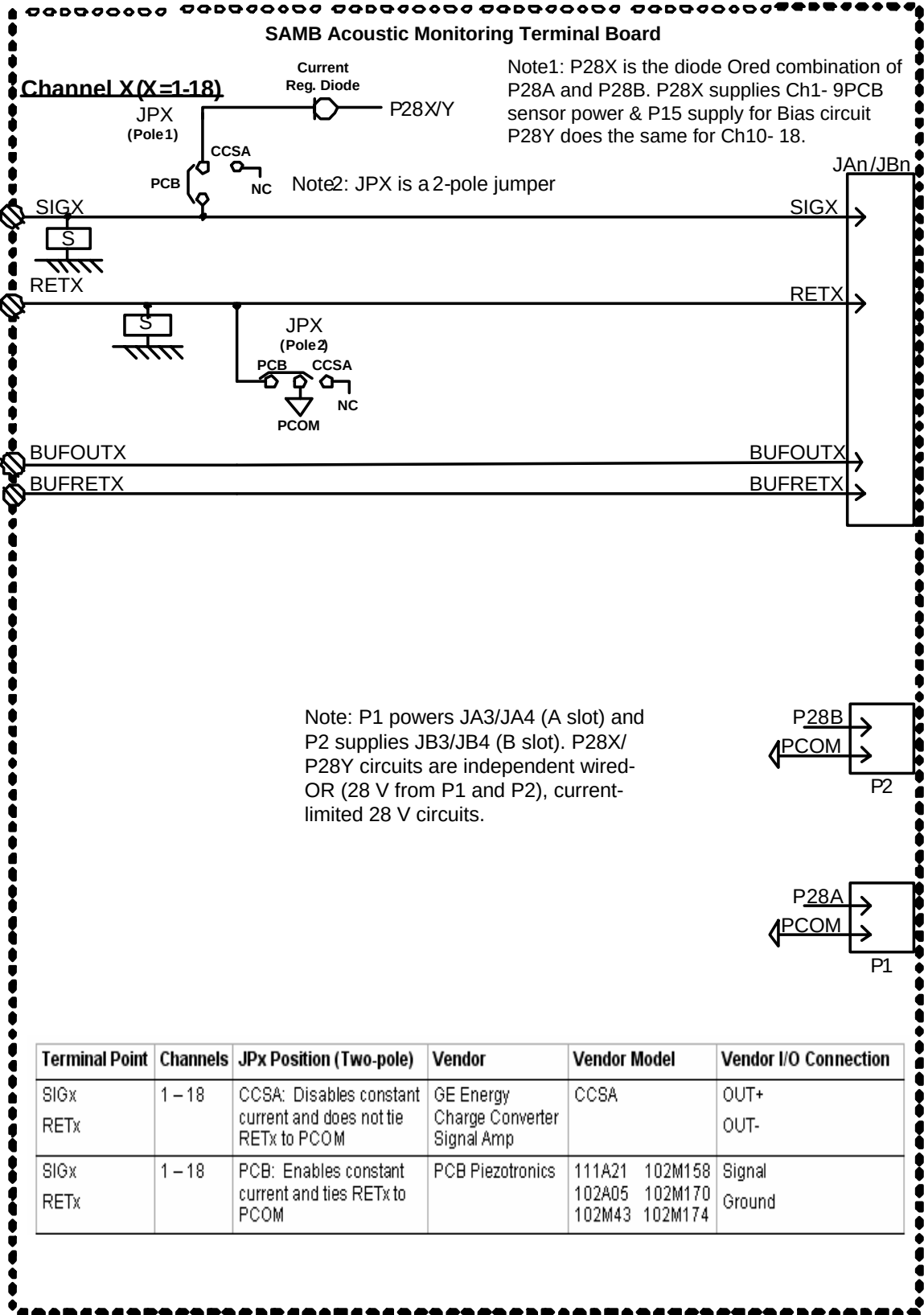
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**Note** A GE field service technician should install the PAMB. Technicians should refer to Support Central website *Acoustic Monitoring Module (PAMB) Installation* in a Mark VIe Control, for complete installation instructions.

The figure, *SAMB Acoustic Monitoring Terminal Board*, shows the functionality of one of the 18 channels supported by SAMB and PAMB. Connect the CCSA or PCB sensors and the buffered outputs to the terminal blocks, as described in the table, *Terminal Point Definitions*.

---

Hardware jumpers connect the constant current source to the SIGx line for the PCB sensors. Each channel has hardware jumper, JPx (where x equals the input number). The jumper should be in the CCSA position if the GE CCSA for Endevco<sup>®</sup> sensors or any other voltage output device is used. The jumper should be in the PCB position if a PCB sensor or any other current output device is used.



*SAMB Acoustic Monitoring Terminal Board*



*Terminal Point Definitions*

| Ch. # | Point | Signal   | Description             | Point | Signal | Description                      |
|-------|-------|----------|-------------------------|-------|--------|----------------------------------|
| 1     | 1     | BUFOUT1  | Buffered output, signal | 2     | SIG1   | Dynamic pressure voltage, signal |
|       | 3     | BUFRET1  | Buffered output, return | 4     | RET1   | Dynamic pressure voltage, return |
| 2     | 5     | BUFOUT2  | Buffered output, signal | 6     | SIG2   | Dynamic pressure voltage, signal |
|       | 7     | BUFRET2  | Buffered output, return | 8     | RET2   | Dynamic pressure voltage, return |
| 3     | 9     | BUFOUT3  | Buffered output, signal | 10    | SIG3   | Dynamic pressure voltage, signal |
|       | 11    | BUFRET3  | Buffered output, return | 12    | RET3   | Dynamic pressure voltage, return |
| 4     | 13    | BUFOUT4  | Buffered output, signal | 14    | SIG4   | Dynamic pressure voltage, signal |
|       | 15    | BUFRET4  | Buffered output, return | 16    | RET4   | Dynamic pressure voltage, return |
| 5     | 17    | BUFOUT5  | Buffered output, signal | 18    | SIG5   | Dynamic pressure voltage, signal |
|       | 19    | BUFRET5  | Buffered output, return | 20    | RET5   | Dynamic pressure voltage, return |
| 6     | 21    | BUFOUT6  | Buffered output, signal | 22    | SIG6   | Dynamic pressure voltage, signal |
|       | 23    | BUFRET6  | Buffered output, return | 24    | RET6   | Dynamic pressure voltage, return |
| 7     | 25    | BUFOUT7  | Buffered output, signal | 26    | SIG7   | Dynamic pressure voltage, signal |
|       | 27    | BUFRET7  | Buffered output, return | 28    | RET7   | Dynamic pressure voltage, return |
| 8     | 29    | BUFOUT8  | Buffered output, signal | 30    | SIG8   | Dynamic pressure voltage, signal |
|       | 31    | BUFRET8  | Buffered output, return | 32    | RET8   | Dynamic pressure voltage, return |
| 9     | 33    | BUFOUT9  | Buffered output, signal | 34    | SIG9   | Dynamic pressure voltage, signal |
|       | 35    | BUFRET9  | Buffered output, return | 36    | RET9   | Dynamic pressure voltage, return |
| 10    | 37    | BUFOUT10 | Buffered output, signal | 38    | SIG10  | Dynamic pressure voltage, signal |
|       | 39    | BUFRET10 | Buffered output, return | 40    | RET10  | Dynamic pressure voltage, return |
| 11    | 41    | BUFOUT11 | Buffered output, signal | 42    | SIG11  | Dynamic pressure voltage, signal |
|       | 43    | BUFRET11 | Buffered output, return | 44    | RET11  | Dynamic pressure voltage, return |
| 12    | 45    | BUFOUT12 | Buffered output, signal | 46    | SIG12  | Dynamic pressure voltage, signal |
|       | 47    | BUFRET12 | Buffered output, return | 48    | RET12  | Dynamic pressure voltage, return |
| 13    | 49    | BUFOUT13 | Buffered output, signal | 50    | SIG13  | Dynamic pressure voltage, signal |
|       | 51    | BUFRET13 | Buffered output, return | 52    | RET13  | Dynamic pressure voltage, return |
| 14    | 53    | BUFOUT14 | Buffered output, signal | 54    | SIG14  | Dynamic pressure voltage, signal |
|       | 55    | BUFRET14 | Buffered output, return | 56    | RET14  | Dynamic pressure voltage, return |
| 15    | 57    | BUFOUT15 | Buffered output, signal | 58    | SIG15  | Dynamic pressure voltage, signal |
|       | 59    | BUFRET15 | Buffered output, return | 60    | RET15  | Dynamic pressure voltage, return |
| 16    | 61    | BUFOUT16 | Buffered output, signal | 62    | SIG16  | Dynamic pressure voltage, signal |
|       | 63    | BUFRET16 | Buffered output, return | 64    | RET16  | Dynamic pressure voltage, return |
| 17    | 65    | BUFOUT17 | Buffered output, signal | 66    | SIG17  | Dynamic pressure voltage, signal |
|       | 67    | BUFRET17 | Buffered output, return | 68    | RET17  | Dynamic pressure voltage, return |
| 18    | 69    | BUFOUT18 | Buffered output, signal | 70    | SIG18  | Dynamic pressure voltage, signal |
|       | 71    | BUFRET18 | Buffered output, return | 72    | RET18  | Dynamic pressure voltage, return |

## Operation

SAMB inputs an ac voltage signal from the CCSA proportional to the dynamic pressure sensed by the Endevco pressure sensors. SAMB inputs the dynamic pressure directly from PCB pressure sensors as an ac voltage riding on a dc bias voltage. The terminal board provides configuration options to support the hardware listed in the following table:

*SAMB Connections*

| Terminal Point | Channels | JPx Position (Two-pole)                                       | Vendor                                | Vendor Model               |                               | Vendor I/O Connection |
|----------------|----------|---------------------------------------------------------------|---------------------------------------|----------------------------|-------------------------------|-----------------------|
| SIGx<br>RETx   | 1 – 18   | CCSA: Disables constant current and does not tie RETx to PCOM | GE Energy Charge Converter Signal Amp | CCSA                       |                               | OUT+<br>OUT-          |
| SIGx<br>RETx   | 1 – 18   | PCB: Enables constant current and ties RETx to PCOM           | PCB Piezotronics                      | 111A21<br>102A05<br>102M43 | 102M158<br>102M170<br>102M174 | Signal<br>Ground      |

Each channel provides a constant current source that can be connected to SIGx (where x is the channel number) for the PCB sensors. The jumper JPx (where x equals the channel number) is a two-pole jumper that controls the constant current power supply and whether RETx is tied to the power ground, PCOM. When JPx is in the CCSA position, the constant current is disabled and RETx is not tied to PCOM. When JPx is in the PCB position, the constant current is connected to SIGx, providing approximately 3 mA of current to power the PCB sensor. The RETx line is tied to PCOM to provide a return path for the constant current.

A high impedance dc bias allows PAMB to detect an open connection between the charge amplifier (or PCB sensor) and the SAMB terminal board. Each input circuit has +28 V dc bias only.

## Specifications

| Item                        | Specification                                                                    |
|-----------------------------|----------------------------------------------------------------------------------|
| Input channels              | 18 dynamic pressure inputs                                                       |
| Output channels             | 18 buffered outputs                                                              |
| Power inputs                | 2 P28 inputs, each with a 2-pin connector                                        |
| Bias circuit                | P28 on each channel with < 0.2 % dc error                                        |
| Dc output gain              | 1 ±0.5%                                                                          |
| Allowable offset on outputs | 30 mV ±10%                                                                       |
| Output impedance            | 40 Ω ±50%                                                                        |
| Test points                 | 2 with > ±10 V dc range, < 0.5% error tolerance, and = 2.5 mV / count resolution |
| <b>Physical</b>             |                                                                                  |
| Size                        | 14.3 cm high x 23.1 cm wide (5.625 in x 9.1 in)                                  |
| Temperature                 | -30 to 65°C (-22 to 149 °F)                                                      |
| Cooling                     | Free air convection                                                              |
| Humidity                    | 5 to 95% non-condensing                                                          |

## Diagnostics

The SAMB terminal board has its own ID device, which is interrogated by PAMB. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the JA4 or JB4 connector location. This ID is checked as part of the power-up diagnostics.

# ***PAMC Acoustic Monitoring Input***

---

## ***PAMC Acoustic Monitoring Input***

### ***Functional Description***

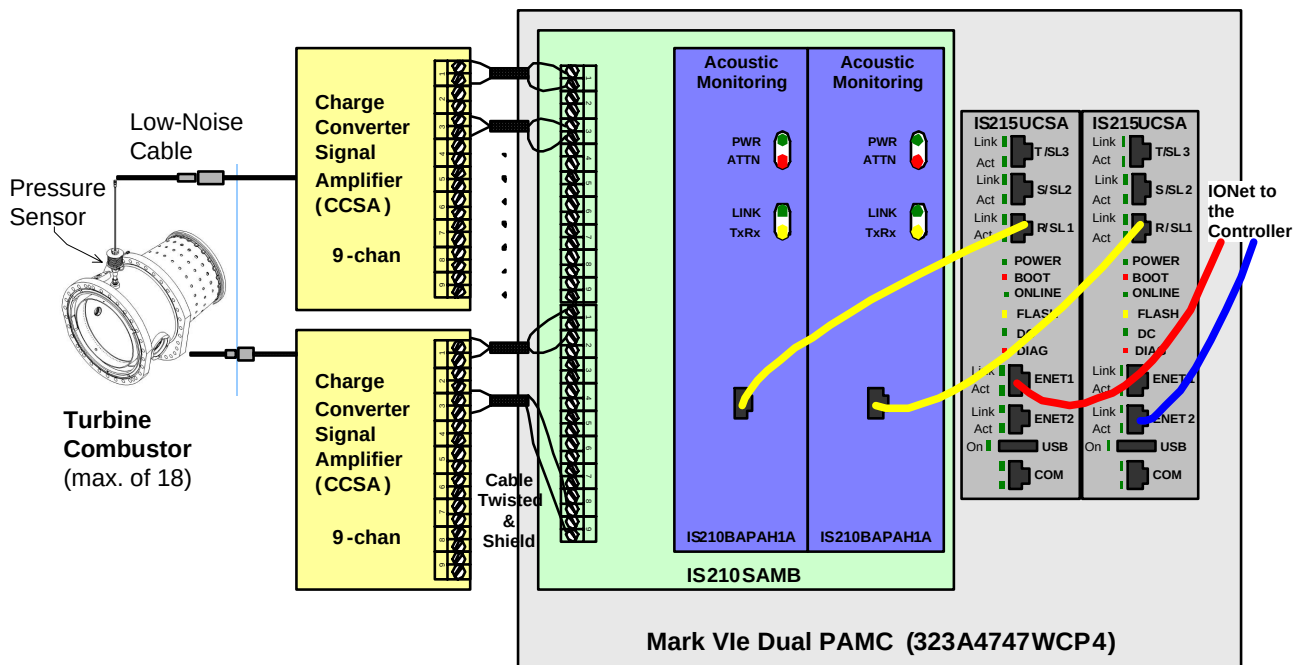
The Mark\* VIe Acoustic Monitoring (PAMC) I/O module supports combustion dynamics for all frame 6, 7, and 9 gas turbines. The PAMC I/O module includes the IS215BAPAH1A Analog Processor (BAPA) and the Acoustic Monitoring (SAMB) terminal board grouped together as an application subassembly, and the IS220UCSAH1A standalone processor module.

PAMC accepts dynamic pressure data from SAMB. The analog signal is conditioned to remove dc bias and amplify ac content (to maximize resolution) before it is digitized by an analog-to-digital (A/D) converter. A field programmable gate array (FPGA) sequences, digitizes, and filters the dynamic pressure signals and controls the high-speed serial link (HSSL) protocol for the Ethernet link between the BAPA and UCSA.

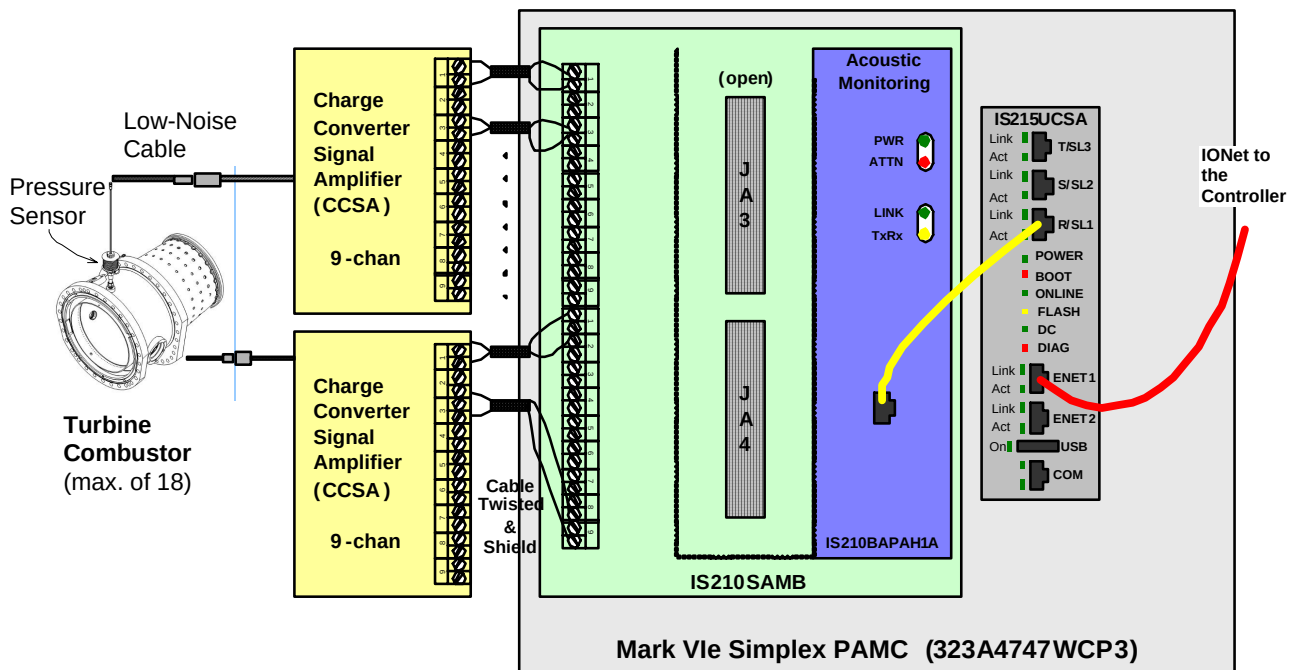
The UCSA, which mounts as a standalone module, is a LAN module that serves as the PAMC processing engine. The UCSA was selected for acoustic monitoring because it provides the additional processing capacity required for the fast Fourier transform (FFT) analysis, sorting function, proprietary algorithms, sensor diagnostics, and so on.

Two versions of the Acoustic Monitoring system are offered, as follows:

**Dual Acoustic Monitoring System (323A4747WCP4).** SAMB fans all 18 inputs to each BAPA. BAPA 1 (left) communicates with the UCSA connected to IONet R. BAPA 2 (right) communicates with the UCSA connected to IONet S. The controller's application code votes which PAMC data to use, based on the signal health.



**Simplex Acoustic Monitoring System (323A4747WCP3)** – Simplex version of 323A4747WCP3. Controller application code is not required to vote signals from PAMC.



## Compatibility

PAMCH1A is compatible with the following acoustic monitoring terminal boards:

| Terminal Board | SAMBH1A       |            |          |
|----------------|---------------|------------|----------|
| Control Mode   | Simplex - Yes | Dual - Yes | TMR - No |

## Installation

The installation procedures in this document only cover the addition of the PAMC I/O module into a MarkVIe system without using the PAMC signal space inputs. A qualified GE technician must install the PAMC signal space inputs.

Refer to the section, *SAMB Installation* to install the SAMB terminal board and dynamic pressure inputs.

## Operation

The PAMC includes the following features.

- Signal conditioning for up to 18 combustion dynamic pressure inputs:
  - GE Energy Charge-Converter Signal Amplifier (CCSA) or Piezotronics<sup>®</sup> sensors for heavy-duty turbines are supported
  - Differential inputs and adjustable gains
  - Fast synchronous-sampled A/D with 16x over-sampling
  - FPGA pre-processor with finite impulse response (FIR) filters
  - Open wire detection
- Analysis capability per channel:
  - Windowed FFT analysis
  - Rolling average per bin
  - 50/60 Hz rejection filters
  - Sort function providing peak pressure amplitude for six different frequency bands
  - Maximum peak detect for each frequency band
  - Average channel peak-to-peak amplitudes per frequency band
  - Alarm detection if peak-to-peak amplitude exceeds configurable level for each frequency band
  - List capture for all 18 channels if alarm is detected or user requests capture

## UCSA LEDs

The UCSA module has the following LEDs:

- **Power** displays solid green when the internal 5 V supply is up and regulating. The PAMC converts the incoming 28 V dc to 5 V dc. All other internal supplies are derived from the 5 V.
- **Boot** displays solid red or blinking red during the boot process. The boot blink codes are described below.
- **Online** displays solid green when the PAMC is online and running application code.
- **Flash** blinks amber when any flash device is being accessed.
- **DC** is not used in the PAMC application.
- **Diag** displays solid red when the PAMC has a diagnostic available. The diagnostic can be viewed and cleared using the ToolboxST\* application.
- **Link** displays solid green if the Ethernet hardware interface on the PAMC has established a link with an Ethernet port.
- **Act** indicates packet traffic on an Ethernet interface. If traffic is low, this LED may blink but in most systems, it is on solid.
- **On** displays solid green when the USB is active.

The boot LED is lit continuously during the boot process unless an error is detected. If an error is detected, the LED blinks at a 1 Hz frequency. While blinking, the LED is on for 500 ms and off for 500 ms. The number of blinks indicates the failed state. After the blink section, the LED turns off for three seconds.

The boot blink codes are:

- 1: Failed Serial Presence Detect (SPD) EEPROM
- 2: Failed to initialize DRAM or DRAM tests failed
- 3: Failed NOR flash file system check
- 4: Failed to load FPGA or PCI failed
- 5: Compact Flash device not found
- 6: Failed to start IDE driver
- 7: Compact Flash image not valid

If the CompactFlash image is valid but the runtime firmware has not been loaded, the boot LED blinks continuously at a 1 Hz rate. Once the firmware is loaded, the boot LED turns off.

### UCSA Boot LED Blink Codes

The boot LED is lit continuously during the boot process unless an error is detected. If an error is detected, the LED blinks at a 1 Hz frequency. While blinking, the LED is on for 500 ms and off for 500 ms. The number of blinks indicates the failed state. After the blink section, the LED turns off for three seconds.

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If the CompactFlash image is valid but the runtime firmware has not been loaded, the boot LED blinks continuously at a 1 Hz rate. Once the firmware is loaded, the boot LED turns off.

## ***UCSA Processor***

The UCSA processor module contains a processor board (IS200UCSAH1A).

- High-speed processor with random access memory (RAM) and flash memory
- Two fully-independent 10/100 Ethernet ports with connectors Enet1 and Enet2 for connecting to the main controllers' Ionet ports.
- Three fully-independent high speed serial link ports with connectors R/SL1, S/SL2, T/SL3. Only R/SL1 is used in the PAMC for connecting to a IS210BAPAH1A analog processor board.
- One universal asynchronous receiver-transmitter (UART) type serial port with RJ-45 connector
- Hardware watchdog timer and reset circuit
- Status-indication LEDs (described above)
- Electronic ID
- Compact flash support

UCSA connects to BAPA through the R/SL1 high speed serial link (HSSL) interface. The PAMC is designed so that the UCSA and the BAPA can be located in different locations (up to 100 meters of high speed serial link cable length). Each module can be powered independently. At power up, the BAPA waits for UCSA to initiate communications. After communication is established, the application FPGA is programmed.

The processor application code contains the logic to allow a UCSA to operate on one or two IONet inputs. When using two IONet inputs, both network paths are active at all times. A failure of either network does not disturb I/O pack operation and is indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system in which the second port is only used after a primary port failure is detected. The Ethernet ports on the UCSA auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

## ***BAPA Analog Processor***

The analog processor includes the following features:

- Eighteen analog signal-conditioning channels
  - Differential inputs
  - Adjustable gains of 1x, 2x, 4x, and 8x
  - Dc bias nulling
  - Multiplexer to bypass signal input and apply test signal
  - Anti-alias filters to support 5 kHz bandwidth
- Twenty-four A/D input channels
  - Six channels per converter
  - 16-bit converter
- Application FPGA
  - A/D converter control
  - D/A converter control
  - Eighteen channels of FIR filtering
  - Configuration registers
  - HSSL control
- Boots FPGA with programmable read-only memory (PROM)
  - Bootstrap function
  - TX / RX mini-MACs
  - PHY sync
- PHY0 and PHY1 physical Ethernet layers
- Power supplies
  - P28 input
  - P15 and N15 outputs
  - P5 output
  - 3.3 V, 2.5 V, and 1.2 V outputs



## Acoustic Monitoring Firmware

The PAMC firmware supports 18 input channels. The main features are:

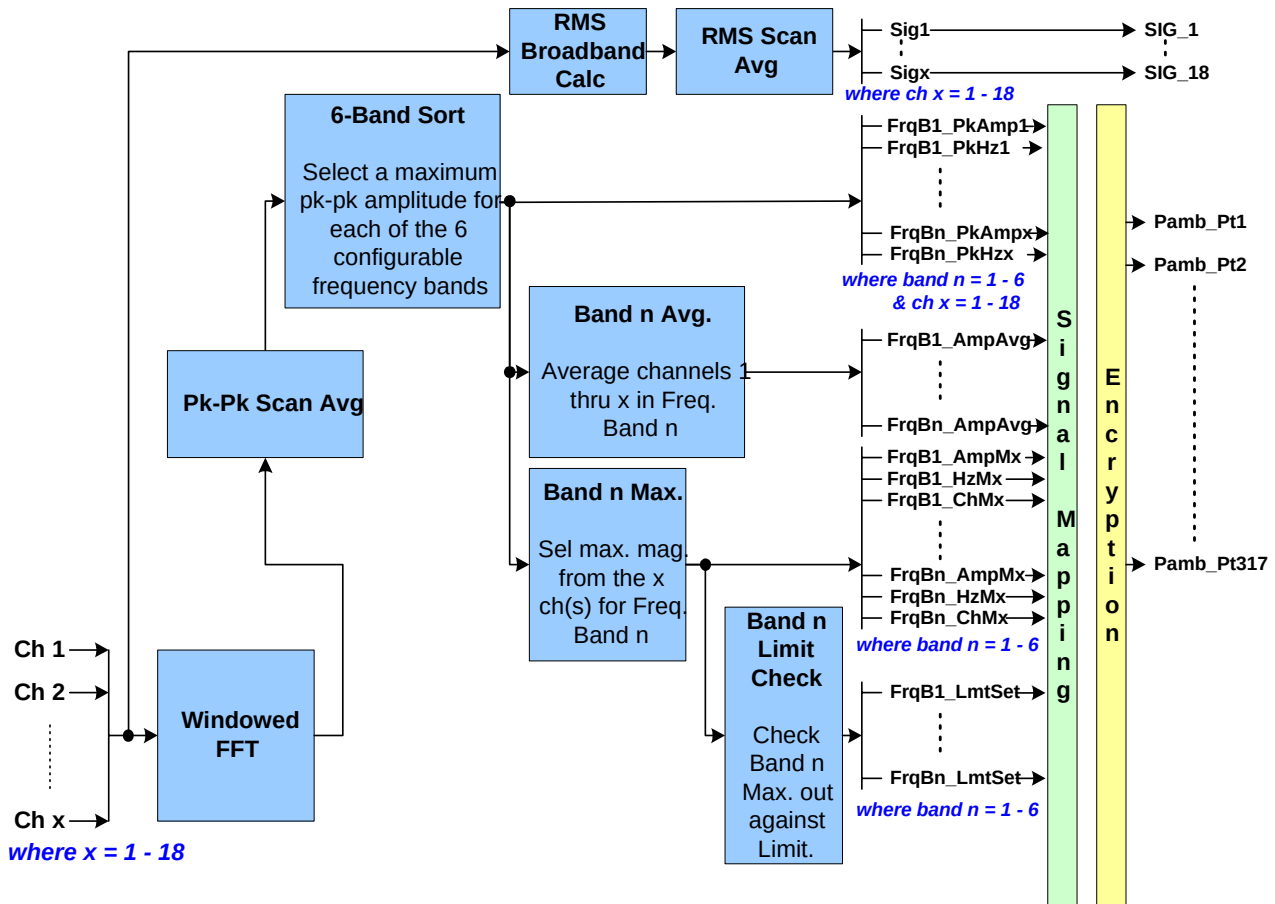
- **RMS Broadband Calculation** – Calculates the broadband root-mean-square (RMS) energy of the time-domain sampled data in the frequency range of 0 to 5000 Hz. The output is the input of the RMS Scan Average.
- **RMS Scan Average** – Average multiple scans of broadband RMS values. A scan is defined by the amount of time-domain sampled combustion data to calculate a windowed FFT of some defined length. The output is the system input, SIGx (where x is the channel number), passed to the controller.
- **Windowed FFT** – Calculates the frequency domain peak-to-peak magnitude and bin frequency, based on time-domain sampled combustion input data. The configuration defines the type of FFT window function used, the FFT length (amount of input data collected for the calculation), and the sample frequency. The output feeds the Peak-to-Peak Scan Average.
- **Peak-to-Peak Scan Average** – Provides a frequency domain peak-to-peak magnitude average per frequency bin, over multiple scans. The configuration defines the number of scans used in the rolling average calculation. The output is the input for the Six-Band Sort function.
- **Six-Band Sort** – Average frequency domain peak-to-peak data is sorted into six separate frequency bands, as displayed in the following table.

### *Frequency Bands*

| Freq Band # | Configuration Band Name |
|-------------|-------------------------|
| 1           | Low (Low)               |
| 2           | Middle (Mid)            |
| 3           | High (High)             |
| 4           | Low Low (LoLo)          |
| 5           | Trans (Trns)            |
| 6           | Screech (Scrch)         |

The maximum of the average peak-to-peak magnitudes from each frequency band and its corresponding frequency bin are selected and output as system inputs for the controller.

- **Band n Average** – Calculates the average peak-to-peak magnitude over all enabled healthy input channels, based on the output of the Six-Band Sort.
- **Band n Maximum** – Calculates the maximum peak-to-peak magnitude over all input channels enabled, based on the Six-Band Sort data. The six frequency band maximums are output for use by the controller.
- **Band n Limit Check** – A frequency band limit check based on the Band n Maximum output data.



Acoustic Monitoring Block Diagram

## A/D Compensation

The A/D compensation function eliminates any gain or offset error due to initial component inconsistency. An auto-calibration function executes each time the module is reset. The auto-calibration function compares each of the 18 analog channels against a standard A/D channel. This A/D channel is calibrated using a standard high-precision voltage reference and the A/D common.

## ***Input Units to Engineering Value Conversion***

The Acoustic Monitoring System converts the hardware input units to the engineering units (EU) needed for the system calculation. For the conversion of mV to psi, the range is 20 to 600 mV per psi. Four configuration parameters are provided per channel to define the equation for the transfer function.

$$\text{Value (EU in counts)} = \text{GUnitConversion} * \text{Input (millivolts in counts)} + \text{Offset}$$

where

$$\text{GUnitConversion} = (\text{High\_Value} - \text{Low\_Value}) / (\text{High\_Input} - \text{Low\_Input})$$

$$\text{Offset} = \text{High\_Value} - \text{GUnitConversion} * \text{High\_Input}$$

where High\_Value, Low\_Value, High\_Input + Low Input are the configuration parameters.

## ***A/D Gain Adjust***

The configuration parameter, Gain, controls the channel gain in the hardware. This parameter is defined for each channel. This allows low-level signals to be amplified to provide better resolution in the A/D conversion hardware. The gain options are 1x, 2x, 4x, and 8x. The channel control writes the gain setup to the FPGA input amplifier 4x and 2x gain control registers. The signal level calculated by PAMC firmware does not change with the Gain parameter because the signal is divided by the gain factor in the firmware, resulting in a net gain of 1 for the signal regardless of the gain factor used. The maximum expected signal level should not exceed 10 V (saturation) after the gain is applied as indicated in the following table.

*Rules for Selecting Gain Value*

| <b>Gainx</b> | <b>Maximum magnitude of input signal after dc bias is removed (volts)</b> |
|--------------|---------------------------------------------------------------------------|
| 1            | 10                                                                        |
| 2            | 5                                                                         |
| 4            | 2.5                                                                       |
| 8            | 1.25                                                                      |

## ***RMS Calculation and Rolling Average***

The RMS calculation function performs an RMS calculation on the ac acoustic information sampled for a given scan. The RMS is defined as follows:

$$\text{rms\_Chx} = \text{SQRT} \left( (\text{AC\_Input}(0)**2 + \text{AC\_Input}(1)**2 + \dots + \text{AC\_Input}(\text{Buffer\_Length})**2) / \text{Buffer\_Length} \right)$$

Where x is the channel number.

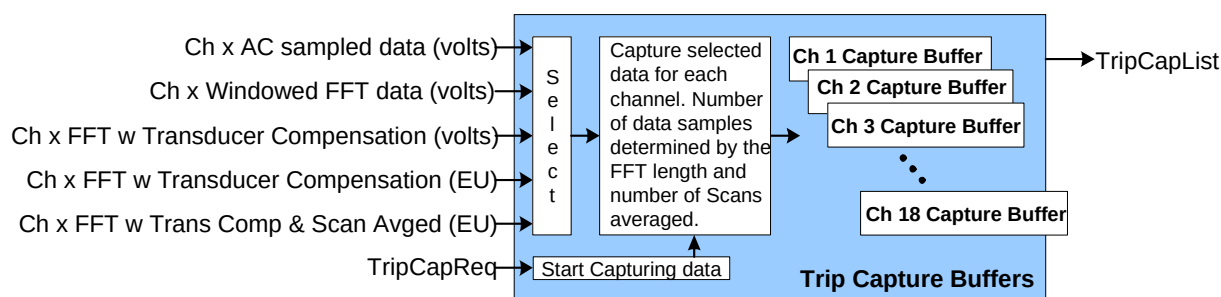
The rolling average function provides a smoothing function to reduce the vibration in the signal.

## Capture Buffers

Two capture buffers are available, as follows:

- **Trip Capture Buffers** - This function provides capture buffers that input internally calculated data, which is selected based on a configuration parameter. The capture buffers can be configured (parameter NumEventScans) to capture up to 32 scans of information for each of 18 channels. Parameter EventListSel can be used to configure the trip capture buffer to collect any one of the following internal data:
  - Time-domain sampled input data (in volts)
  - Frequency-domain FFT peak-to-peak magnitude (in volts)
  - FFT output data with transducer compensation (in volts)
  - FFT output data with transducer compensation (in EU)
  - Scan-averaged FFT output data with transducer compensation (in EU) (default)

Trip Capture Buffers are pre-triggered; meaning for a 32 scan FFT average, data is scanned 32 times before the triggered event and none after the event. The triggered event is activated by the signal space input, TripCapReq. Running on the HMI or OSM computer, AM Gateway software uploads the captured buffers to the computer on which the Gateway is running.



*PAMC Acoustic Monitoring Diagnostic Support*

- **User Capture Buffers** - This function provides capture buffers that are only one scan in length (compared to the trip capture with up to 32 scans). The user capture buffers can be configured using parameter OpListSel to collect any of the internal data listed above for trip capture buffers. The AM Gateway software can upload these buffers. User capture buffers are activated through the AM Gateway or other compatible applications. The diagram shown above for trip capture buffers is the same for user capture buffers except for the trigger source.

## Specifications

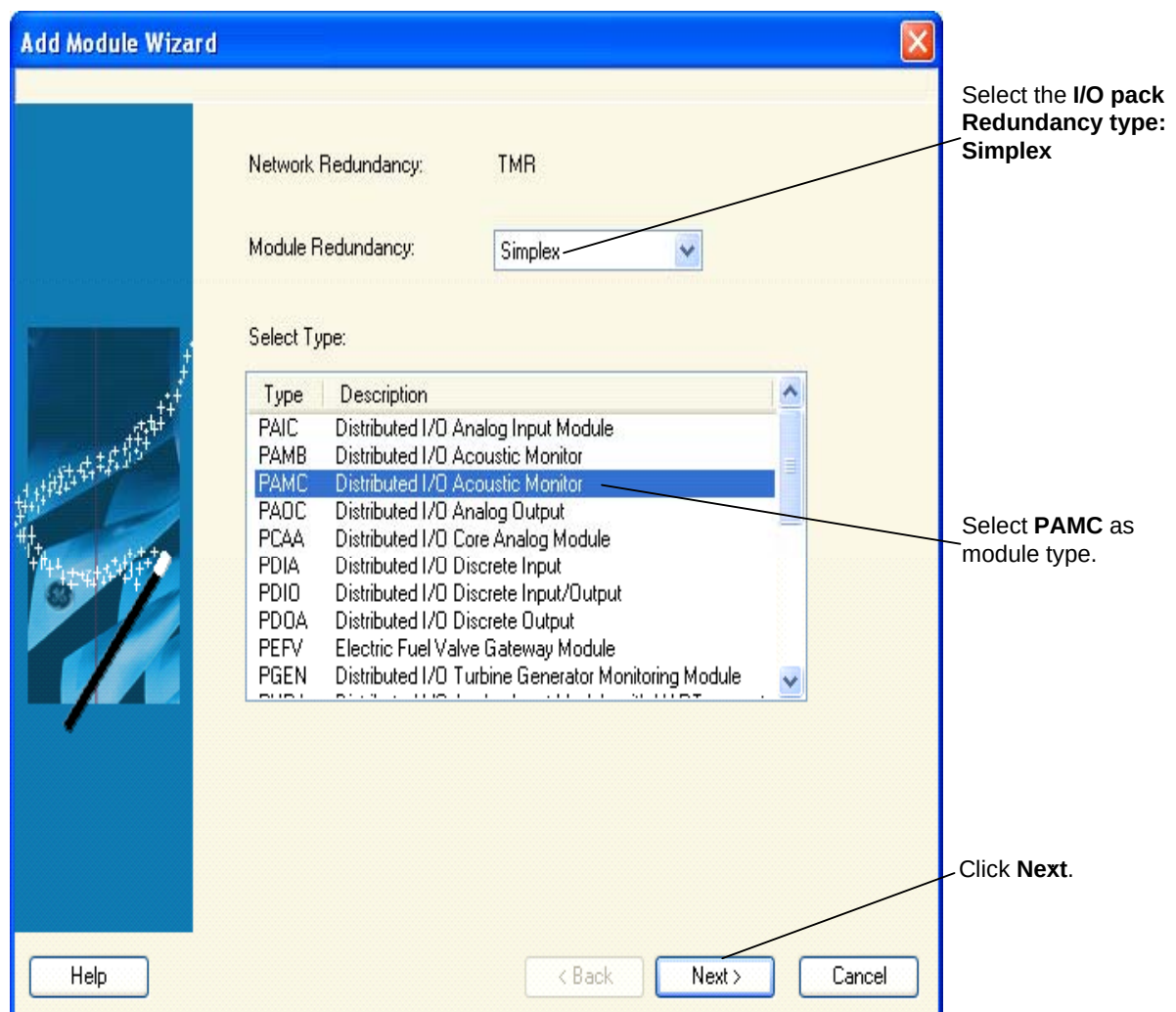
| Item                                                                         | Specification                                                                                                                                                                                      |
|------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input channels                                                               | 18 dynamic pressure inputs                                                                                                                                                                         |
| Output channels                                                              | 18 buffered outputs                                                                                                                                                                                |
| Gain adjustment options                                                      | 1x, 2x, 4x, and 8x                                                                                                                                                                                 |
| Bias – minimum adjust                                                        | -13.5 ±0.25 V dc                                                                                                                                                                                   |
| Bias – maximum adjust                                                        | +13.5 ±0.25 V dc                                                                                                                                                                                   |
| Input accuracy from terminal point to inputs, SIGx for passband = 0 to 5 kHz | ≤ 2.0 % of full scale = 10 V dc for Gain = 1x<br>≤ 2.0 % of full scale = 5 V dc for Gain = 2x<br>≤ 2.0 % of full scale = 2.5 V dc for Gain = 4x<br>≤ 2.0 % of full scale = 1.25 V dc for Gain = 8x |

| Item                                                                                                                               | Specification                                                                                                                                                                                                          |
|------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Input accuracy (dc + ac) from terminal point to peak-peak signal –space values through FFT analysis for passband = 0 to 3.2 kHz    | $\leq 0.5\%$ of full scale = 10 V dc for Gain = 1x<br>$\leq 0.5\%$ of full scale = 5 V dc for Gain = 2x<br>$\leq 0.5\%$ of full scale = 2.5 V dc for Gain = 4x<br>$\leq 0.5\%$ of full scale = 1.25 V dc for Gain = 8x |
| Input accuracy (dc + ac) from terminal point to peak-peak signal-space values through FFT analysis for passband = 3.2 kHz to 5 kHz | $\leq 2.0\%$ of full scale = 10 V dc for Gain = 1x<br>$\leq 2.0\%$ of full scale = 5 V dc for Gain = 2x<br>$\leq 2.0\%$ of full scale = 2.5 V dc for Gain = 4x<br>$\leq 2.0\%$ of full scale = 1.25 V dc for Gain = 8x |
| Input passband frequency                                                                                                           | 0 to 5 kHz                                                                                                                                                                                                             |

## ToolboxST Procedures

### ➤ To add a PAMC control I/O pack

- 1 From the Mark VIe **Component Editor**, click the **Hardware** tab.
- 2 From the **Tree View**, right-click the **Distributed I/O** item and select **Add Module**. The **Insert Module Wizard** dialog box displays.



Use the **Version** drop-down list to select a module version. Listed module versions depend on the available compatibility codes.

**Add Module Wizard**

Version: PAMC\_1\_1

Release Notes

☒ Module Required

**I/O Pack Configurations**

| PackRef | HW Form | Location | Connection A | Connection B |
|---------|---------|----------|--------------|--------------|
| PackR   | H1A     | L25R     | IoNet1       |              |

Help < Back Next > Cancel

Click the **Release Notes** button to view additional information about the currently selected module version.

To ensure that hardware failures are identified and corrected prior to controller system operation, it is highly **recommended** that the **Module Required** check box be selected. If it is, the module must be present and functioning for the controller to go online.

Click **Next** to preview configuration information.

**Add Module Wizard**

**Module Configuration**

Name: PAMC-25

I/O Packs: 1

Required: Yes

**I/O Pack Configuration**

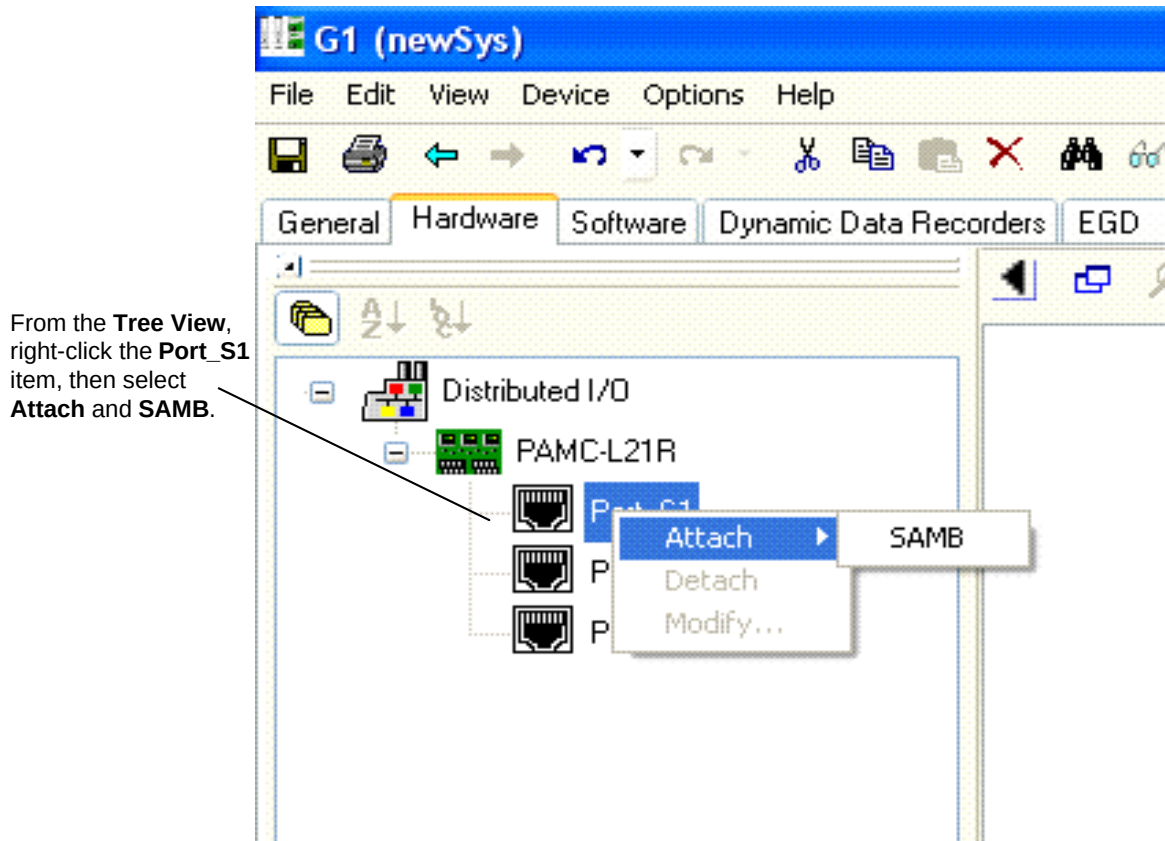
| I/O Pack | HW Form | Location | Port A | Port B |
|----------|---------|----------|--------|--------|
| 1        | H1A     | L25R     | IoNet1 |        |

Help < Back Finish Cancel

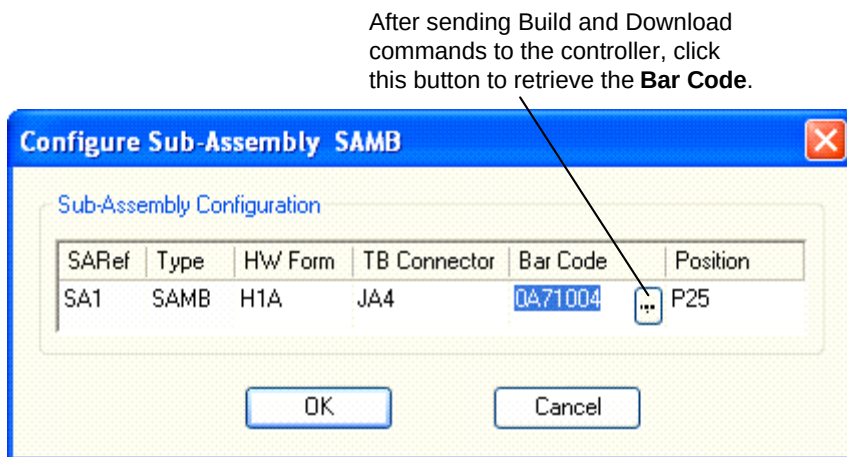
Click **Finish** to add the new module.

➤ To add a SAMP module

- 1 From the **Component Editor**, click the **Hardware** tab.



- 2 The **Configure Sub-Assembly SAMP** dialog box displays.



**Note** Additional attachments cannot be added to other ports.

- 3 Enter the **TB Connector** that the BAPA is plugged into and the **Bar Code** of the SAMP. The bar code is located underneath the cover plate over the JB4 connector if no BAPA is plugged into this connector. If a BAPA is plugged into JB4, remove this BAPA to view the bar code or use the bar code retrieval method shown below.

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board ID to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- Each input has sensor limit checking, open circuit detection, dc bias autonulling, and excessive dc bias detection. Alarms are generated for these diagnostics. Refer to the tables I/O Pack Alarms and Point Configuration.

Details of the individual diagnostics are available in the ToolboxST application. I/O block SYS\_OUTPUTS, input RSTDIAF can be used to direct all I/O modules to clear from the alarm queue all diagnostics in the normal healthy state.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter    | Description (SAMB Level Configuration)                                                                                                                                                                                                                                                         | Choices                                                                  |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| BinReject    | Defines the number of side bins that are rejected when the search function is applied to the FFT results for channels 1 – 18, = no bins rejected                                                                                                                                               | 0 to 6 (default: 3)                                                      |
| Config_Mode  | Defines the source of the currently active configuration. ToolboxST allows only mode Toolbox as a selection. The remote gateway configurator forces mode to tuning configurator without user control.                                                                                          | Toolbox only                                                             |
| E_Bnds_Vis   | Enables visibility of the parameters associated with the energy bands processing. This visibility is restricted to authorized GE personnel and requires the correct code to enable visibility.                                                                                                 | 0 to 2147483647 (default: 0)                                             |
| FFT_Length   | Defines the number of samples that are used in FFT calculation                                                                                                                                                                                                                                 | 1024, 2048, 4096, 8192, 16382, 32768 (default: 8192)                     |
| FFT_TF_SelA  | Boolean that selects the internal test file as the input to all acoustic monitoring channels instead of the actual analog input signals                                                                                                                                                        | HW_Input or File (default: HW.Input)                                     |
| EventLstSel  | Defines the sample site for the event capture list:<br>Disable: list not used<br>FFT_Out: FFT output scaled in volts<br>TC_Out: FFT output after transducer compensation<br>PSI_Out: FFT outputs scaled in PSI<br>Avg_Out: PSI_Out after averaging filter<br>Raw_Input: Input time domain data | Avg_Out, Disable, FFT_Out, PSI_Out, Raw_Input, TC_Out (default: Avg_Out) |
| HiB_Limit    | Defines the limit for the max peak-peak amplitude signal in the high frequency band                                                                                                                                                                                                            | 0 to 50 psi (default: 50)                                                |
| HiScrChBrkPt | Defines the frequency boundary between the high and screech frequency bands                                                                                                                                                                                                                    | 0 to 5000 Hz (default: 500)                                              |
| LoLoB_Limit  | Defines the limit for the max peak-peak amplitude signal in the low-low frequency band                                                                                                                                                                                                         | 0 to 50 psi (default: 50)                                                |
| LowB_Limit   | Defines the limit for the max peak-peak amplitude signal in the low frequency band                                                                                                                                                                                                             | 0 to 50 psi (default: 50)                                                |



| Parameter                       | Description (SAMB Level Configuration)                                                                                                                                                                                                                                                                            | Choices                                                                  |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| LowLow_EndPt                    | Defines the ending frequency of the low-low frequency band                                                                                                                                                                                                                                                        | 0 to 5000 Hz (default: 30)                                               |
| LowLowStrtPt                    | Defines the starting frequency of the low-low frequency band                                                                                                                                                                                                                                                      | 0 to 5000 Hz (default: 10)                                               |
| LowMid_BrkPt                    | Defines the frequency boundary between low and mid frequency bands                                                                                                                                                                                                                                                | 0 to 5000 Hz (default: 120)                                              |
| Low_StrtPt                      | Defines the starting frequency of the low band                                                                                                                                                                                                                                                                    | 0 to 5000 Hz (default: 30)                                               |
| MaxVoltCCSA                     | Max sensor volts for a CCSA type sensor                                                                                                                                                                                                                                                                           | -30 to 30 V (default: 8.658)                                             |
| MaxVoltCustm                    | Max sensor volts for a custom type sensor                                                                                                                                                                                                                                                                         | -30 to 30 V (default: 5.29)                                              |
| MaxVoltPCB                      | Max sensor volts for a PCB type sensor                                                                                                                                                                                                                                                                            | -30 to 30 V (default: 4.75)                                              |
| MidB_Limit                      | Defines the limit for the max peak-peak amplitude signal in the mid frequency band                                                                                                                                                                                                                                | 0 to 50 psi (default: 50)                                                |
| MidHi_BrkPt                     | Defines the frequency boundary between mid and high frequency bands                                                                                                                                                                                                                                               | 0 to 5000 Hz (default: 240)                                              |
| MinVoltCCSA                     | Minimum sensor volts for a CCSA type sensor                                                                                                                                                                                                                                                                       | -30 to 30 V (default: 8.658)                                             |
| MinVoltCustm                    | Minimum sensor volts for a custom type sensor                                                                                                                                                                                                                                                                     | -30 to 30 V (default: 5.25)                                              |
| MinVoltPCB                      | Minimum sensor volts for a PCB type sensor                                                                                                                                                                                                                                                                        | -30 to 30 V (default: -15.25)                                            |
| NumEventScns                    | Defines the number of scans an event buffer contains*Note. If the sample location is Raw_Input the max scan allowed is 1.                                                                                                                                                                                         | 1 to 100 scans (default: 32)                                             |
| OpLstSel                        | Defines sample site for spectrum on demand capture or diagnostic list:<br>Disable: list not used<br>Raw_Input: input time domain data<br>FFT_Out: FFT output scaled in volts<br>TC_Out: FFT output after transducer compensation<br>PSI_Out: FFT outputs scaled in PSI<br>Avg_Out: PSI_Out after averaging filter | Avg_Out, Disable, FFT_Out, PSI_Out, Raw_Input, TC_Out (default: Avg_Out) |
| PL_Fil_Freq                     | Defines the power line frequency that the notch filter removes from the spectral content of the FFT output                                                                                                                                                                                                        | 50_Hz, 60_Hz (default: 60_Hz)                                            |
| PL_Fil_Tol                      | Power line filter signature tolerance calculated vs theoretical. 10% = 0.1.                                                                                                                                                                                                                                       | 0 to 1.0 (default: 0.1)                                                  |
| PL_Fil_Width                    | Defines the bandwidth of the power line notch filter. The bandwidth is $\pm$ value centered about the configured power line frequency.                                                                                                                                                                            | 0 to 100 Hz (default: 0.5)                                               |
| SampleRate                      | Defines the FFT sample rate for all the acoustic monitoring channels                                                                                                                                                                                                                                              | 12,877 Hz only                                                           |
| ScanPrAvgFFT                    | Number of scans per average in acoustic monitoring filtered FFT output                                                                                                                                                                                                                                            | 1 to 100 scans (default: 48)                                             |
| ScanPrAvgRMS                    | Number of scans per average in the RMS calculation                                                                                                                                                                                                                                                                | 1 to 32 scans (default: 1)                                               |
| SearchInAvg(1) – SearchInAvg(6) | Selects whether the sort function for pk-pk amplitudes uses the present scan or an average value                                                                                                                                                                                                                  | No average, Average (default: Average)                                   |
| Session_Time                    | Scheduled time for temporary configuration mode. This time is forced to zero in the ToolboxST entry. This value is set to the user-selected time in the temporary gateway remote configurator.                                                                                                                    | 0 only                                                                   |
| ScrchB_Limit                    | Defines the limit level for the maximum peak-peak amplitude signal in the screech frequency band                                                                                                                                                                                                                  | 0 to 50 psi (default: 50)                                                |
| Scrch_EndPt                     | Defines the ending frequency of the screech frequency band                                                                                                                                                                                                                                                        | 0 to 5000 Hz (default: 3000)                                             |
| T_FilWidth                      | Width ( $\pm$ Hz) of the filter that excludes the transverse frequency FFT coefficients and all FFT coefficients designated by this filter from the screech band search                                                                                                                                           | 0 to 100 Hz (default: 40)                                                |
| TMC_Gain(1) – TMC_Gain(30)      | Transducer mounting compensation gain to characterize gain response                                                                                                                                                                                                                                               | 0 to 30 (default: 1)                                                     |
| TMC_Freq(1) – MC_Freq(30)       | Frequency corresponding to the gain value entered                                                                                                                                                                                                                                                                 | 0 to 5000 Hz (default: n*100)                                            |

| Parameter    | Description (SAMB Level Configuration)                                                                         | Choices                                                                                      |
|--------------|----------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|
| TrnsB_Limit  | Defines the limit for the max peak-peak amplitude signal in the transverse frequency band                      | 0 to 50 Psi (default: 50)                                                                    |
| Trns_Bnd_Enb | Enable calculations associated with the transverse band and exclude its FFT coefficients from the screech band | Disable, Enable (default: Enable)                                                            |
| Trns_EndPt   | Defines the ending frequency of the transverse frequency band                                                  | 0 to 5000 Hz (default: 1150)                                                                 |
| Trns_StrtPt  | Defines the starting frequency of the transverse frequency band                                                | 0 to 5000 Hz (default: 950)                                                                  |
| WindowSelect | Selects windowing function for sampled data for Channel A and B:                                               | Rectangular<br>Hamming<br>Hanning<br>Triangular<br>Blackman<br>Blackman-Har(ris)<br>Flat Top |

### *IS200SAMB Variable Definitions and Configuration*

| Sigx                      | Analog input x – Card Point                                                                                                                                               | Point Edit (Input FLOAT)                          |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|
| <b>Where x = 1 thr 18</b> |                                                                                                                                                                           |                                                   |
| Gain                      | Analog input resolution adjustment to amplify signal before digital conversion. Gain factor * (maximum signal peak voltage) must be less than 10 V to prevent saturation. | 1x, 2x, 4x, 8x (default: 8x)                      |
| Bias                      | Dc bias voltage subtracted from the analog signal input for dc bias compensation. Only used when InputUse is custom or file.                                              | -11.67 to 11.67 (default: 0)                      |
| Bias_Range                | Allowable deviation of dc bias used for dc bias diagnostics. Only used when InputUse is custom or file.                                                                   | 0 to 10 (default: 1)                              |
| Can_Id                    | Combustor can be wired to this terminal board signal. This normally corresponds to the signal number to avoid confusion; wire terminal board signal 1 to can 1.           | 1 to 18 (default: 11)                             |
| High_Input                | Defines point 2 X-axis value in mV for SAMB terminal point that is used to calculate gain and offset for conversion to EU                                                 | -10000 to 10000 (default: 170)                    |
| High_Value                | Defines point 2 Y-axis value in EU for SAMB terminal point that is used to calculate gain and offset for conversion from mV to EU                                         | Any positive real (default: 1)                    |
| InputUse                  | Selects the sensor type used on the signal.                                                                                                                               | Unused, CCSA, PCB, Custom, File (default: Unused) |
| Low_Input                 | Defines point 1 X-axis value in mV for SAMB terminal point that is used to calculate gain and offset for conversion to EU                                                 | -10000 to 10000                                   |
| Low_Value                 | Defines point 1 Y-axis value in EU for SAMB terminal point that is used to calculate gain and offset for the conversion from mV to EU                                     | Any positive real (default: 0)                    |
| PL_Fil_En                 | Enables the power line notch filter                                                                                                                                       | Disable, Enable (default: Disable)                |
| DiagHighEnab              | Enables high input sensor limit diagnostics                                                                                                                               | Disable, Enable (default: Enable)                 |
| DiagLowEnab               | Enables low input sensor limit diagnostics                                                                                                                                | Disable, Enable (default: Enable)                 |
| BiasNullEnab              | Enables automatic dc bias nulling                                                                                                                                         | Disable, Enable (default: Enable)                 |
| DiagOCChk                 | Enables open sensor error diagnostic test                                                                                                                                 | Disable, Enable (default: Enable)                 |
| DiagBiasNull              | Enables excessive dc bias diagnostic test                                                                                                                                 | Disable, Enable (default: Enable)                 |
| DiagSigSat                | Enables signal saturation diagnostic test                                                                                                                                 | Disable, Enable (default: Enable)                 |

### IS200SAMB Signal Definitions

| Board Points (Signals) | Description – Point Edit(Enter Signal Connection)               | Direction | Type    |
|------------------------|-----------------------------------------------------------------|-----------|---------|
| L3DIAG_SAMB_R(S or T)  | Board Diagnostic active (non-voted signal)                      | Input     | BIT     |
| LINK_OK_SAMB_R(S or T) | High speed serial link SL1 is communicating with BAPA           | Input     | BIT     |
| ATTN_SAMB              | SAMB has an active alarm                                        | Input     | BIT     |
| Can1_Health            | Combustor can 1 signal health                                   | Input     | BIT     |
| :                      | :                                                               |           |         |
| Can18_Health           | Combustor can 18 signal health                                  | Input     | BIT     |
| Test_Config            | Card is temporarily remotely configured                         | Input     | BIT     |
| Test_Mode              | Signals are from internal test sources, not from terminal board | Input     | BIT     |
| TripCapList            | A capture buffer triggered by TripCapReq is available           | Input     | BIT     |
| UserCapList            | A capture buffer manually requested by a user is available      | Input     | BIT     |
| PambBool_1             | General Electric Proprietary Information                        | Input     | BIT     |
| :                      | :                                                               |           |         |
| PambBool_6             | General Electric Proprietary Information                        | Input     | BIT     |
| PambPt_0               | General Electric Proprietary Information                        | Input     | INTEGER |
| :                      | :                                                               |           |         |
| PambPt_317             | General Electric Proprietary Information                        | Input     | INTEGER |
| Num_Of_Scans           | Scan (block of FFT data) number of this data (1 – 100)          | Input     | INTEGER |
| Num_Avg_Scns           | Number of scans (block of FFT data) averaged (1 – 100)          | Input     | INTEGER |
| Session_Tmr            | Time remaining for remote tuning session                        | Input     | INTEGER |
| TripCapReq             | Request for trip capture buffer collection                      | Output    | BIT     |

# Alarms

## PAMC Specific Alarms

| Alarm ID | Alarm Description                                                            | Possible Cause                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Solution                                                                                                                                                                                         |
|----------|------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 38       | Flashdisk error: Unable to revert to flash configuration after remote access | Permanent configuration data on card is corrupted.                                                                                                                                                                                                                                                                                                                                                                                                               | Download firmware to card or replace UCSA.                                                                                                                                                       |
| 41-58    | Sig {0:F0}: Open Ckt Test Failed Check Wires and Sensor                      | Open circuit detected for terminal board signal Sig x, where x is the identified point.                                                                                                                                                                                                                                                                                                                                                                          | Check wiring and sensor                                                                                                                                                                          |
| 61-78    | Sig {0:F0}: Bias Nulling Error Check InputUse Config                         | DC bias designated for sensor type is outside of range detected for sensor.                                                                                                                                                                                                                                                                                                                                                                                      | Check sensor type in configuration parameter InputUse or check dc bias voltage on signal.                                                                                                        |
| 81-98    | Sig {0:F0}: Input Signal Saturated Check Gain Config                         | Peak input voltage is saturating input.                                                                                                                                                                                                                                                                                                                                                                                                                          | Decrease configuration parameter Gain for designated signal or check for sensor problem.                                                                                                         |
| 101-118  | Sig {0:F0}: Sensor Limit Exceeded                                            | Peak input voltage exceeds limit for selected sensor type.                                                                                                                                                                                                                                                                                                                                                                                                       | Check sensor type in configuration parameter InputUse or check for sensor problem.                                                                                                               |
| 120      | BAPA ADC Reference input calibration failure.                                | BAPA failed calibration test at power up.                                                                                                                                                                                                                                                                                                                                                                                                                        | Replace BAPA.                                                                                                                                                                                    |
| 121-138  | BAPA Chan {0:F0}: ADC calibration failure.                                   | BAPA failed calibration test at power up.                                                                                                                                                                                                                                                                                                                                                                                                                        | Replace BAPA.                                                                                                                                                                                    |
| 139-156  | BAPA Chan {0:F0}: DAC calibration failure.                                   | BAPA failed calibration test at power up.                                                                                                                                                                                                                                                                                                                                                                                                                        | Replace BAPA.                                                                                                                                                                                    |
| 157-174  | BAPA Chan {0:F0}: DC test failure.                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                  |
| 175-192  | BAPA Chan {0:F0}: Analog gain test failure.                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                  |
| 193-210  | BAPA Chan {0:F0}: AC FFT test failure.                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                  |
| 211-228  | BAPA Chan {0:F0}: Anti alias rolloff test failure.                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                  |
| 212      | HSSL Comm link {0:F0} Communication Failure, Code {1:F0}                     | The PAMC/UCSA cannot communicate with remote acquisition hardware (terminal board and BAPA) through the HSSL cable. Code indicates specific failure type. Common codes include:<br>51xxxxxx: Remote acquisition target returning bad id<br>52xxxxxx: Download to BAPA failed<br>53xxxxxx: Link loss detected<br>54xxxxxx: Receive packet error detected<br>55xxxxxx: Transmit packet error (excessive naks)<br>57xxxxxx: No data received from BAPA in 5 seconds | Verify that the BAPA is connected to the appropriate HSSL connector on the UCSA.<br>Check HSSL link cables. If problem persists, replace the UCSA card.<br>Check power on BAPA.<br>Replace BAPA. |

| Alarm ID | Alarm Description                                          | Possible Cause                                                                                 | Solution                                                                                                                                                                                         |
|----------|------------------------------------------------------------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 213      | HSSL Comm link {0:F0} Initialization Failure               | The PAMC/UCSA cannot properly initialize the BAPA.                                             | Verify that the BAPA is connected to the appropriate HSSL connector on the UCSA.<br>Check HSSL link cables. If problem persists, replace the UCSA card.<br>Check power on BAPA.<br>Replace BAPA. |
| 214      | HSSL Comm link {0:F0} Configuration Failure, Code {1:F0}   | PAMC/UCSA interface to the HSSL failed to initialize properly.                                 | Replace UCSA                                                                                                                                                                                     |
| 215      | BAPA plugged into wrong SAMB connector on HSSL Link {0:F0} | SAMB connector that BAPA is plugged into does not agree with connector configured in ToolboxST | BAPA plugged into wrong connector.<br>Serial link plugged into wrong BAPA.<br>Change configured connector in ToolboxST to JA4 or JB4.                                                            |

### ***I/O Pack Alarms***

| Alarm ID | Alarm Description                                           | Possible Cause                                                                                                              | Solution                                                                                                                                                                                                                                    |
|----------|-------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2        | Flash memory CRC failure                                    | Board firmware programming error (board will not go online)                                                                 | Rebuild system and download application and configuration to pack. If problem continues, replace pack.                                                                                                                                      |
| 3        | CRC failure override is active                              | Board firmware programming error (board is allowed to go online)                                                            | Rebuild system and download application and configuration to pack. If problem continues replace pack.                                                                                                                                       |
| 4        | I/O pack in stand-alone mode                                | Invalid command line option                                                                                                 | Rebuild system and download to pack.                                                                                                                                                                                                        |
| 5        | I/O pack in remote I/O mode                                 | Invalid command line option                                                                                                 | Rebuild system and download to pack.                                                                                                                                                                                                        |
| 6        | Special user mode active. Now [ ]                           | Invalid command line option                                                                                                 | Rebuild system and download to pack.                                                                                                                                                                                                        |
| 7        | I/O pack – The I/O pack has gone to the offline state       | Lost communication with controller                                                                                          | Check that controller has not gone off-line. If controller appears OK and other packs are not reporting a problem look for an IONet cable or switch problem.                                                                                |
| 30       | ConfigCompatCode mismatch; Firmware: [ ]                    | A .dll file (ToolboxST support file) has been installed that is incompatible with the firmware loaded on the I/O processor. | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                         |
| 31       | IOCompatCode mismatch; Firmware: [ ]                        | A .dll file (ToolboxST support file) has been installed that is incompatible with the firmware loaded on the I/O processor. | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                         |
| 32-255   | Refer to PAMC-specific alarms                               |                                                                                                                             |                                                                                                                                                                                                                                             |
| 258      | I/O pack Temperature [ ] ° F is out of range [ ] to [ ] ° F | Temperature went outside -20°C to +85 °C (-4° F to +185° F)                                                                 | The environmental controls applied to the cabinet containing the I/O pack should be checked. Pack operation continues correctly beyond these temperature limits but long term operation at elevated temperatures may reduce equipment life. |

| Alarm ID | Alarm Description                                            | Possible Cause                                                                                                  | Solution                                                                                                                                                                                                                                                                                                                       |
|----------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 259      | [ ] frame overruns have occurred                             |                                                                                                                 |                                                                                                                                                                                                                                                                                                                                |
| 260      | [ ] frame number skips have occurred                         |                                                                                                                 |                                                                                                                                                                                                                                                                                                                                |
| 261      | Unable to read configuration file from flash                 | I/O pack does not have correct configuration file stored in flash file system.                                  | Rebuild system and download configuration to pack.                                                                                                                                                                                                                                                                             |
| 262      | Bad configuration file detected                              | The configuration file in the pack is not compatible with the application code that is loaded.                  | Rebuild system and download application and configuration to pack.                                                                                                                                                                                                                                                             |
| 263      | I/O pack configuration – bad name detected                   | Wrong configuration file for I/O pack                                                                           | Rebuild system and download application and configuration to pack.                                                                                                                                                                                                                                                             |
| 264      | I/O pack configuration – bad config compatibility code       | Wrong configuration revision for I/O pack                                                                       | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                            |
| 266      | I/O pack configuration – configuration size mismatch         | The configuration file in the pack does not have the correct size to match the application code that is loaded. | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                            |
| 267      | FPGA – name mismatch detected                                | Wrong configuration for FPGA in I/O pack                                                                        | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                            |
| 268      | FPGA - incompatible revision: Found [ ] Need; [ ]            | Wrong revision of FPGA firmware                                                                                 | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                            |
| 273      | IONet-EGD message – illegal version                          | EGD protocol version incorrect, greater than current version                                                    |                                                                                                                                                                                                                                                                                                                                |
| 279      | Sys - Could not determine platform type from hardware        | Incorrect firmware version or hardware malfunction The firmware could not recognize the host hardware type.     | Ensure that all connectors are aligned properly and fully seated. Check firmware version for compatibility with platform, if OK, replace processor module.                                                                                                                                                                     |
| 280      | Sys - Platform hardware does not match runtime application   | The platform type identified in the application configuration does not match the hardware.                      | Fix platform type in ToolboxST, rebuild and download application.                                                                                                                                                                                                                                                              |
| 281      | Sys - FPGA not programmed due to platform errors             |                                                                                                                 |                                                                                                                                                                                                                                                                                                                                |
| 282      | Sys - Unable to initialize application independent processes | Runtime malfunction. An application-independent firmware process could not be started successfully.             | Reload firmware and application and reboot. If failure persists in controller, remove CompactFlash module and reprogram boot loader using the ToolboxST Download Flash Bootloader option. After reinstalling the flash module and rebooting, reload firmware and application. If this does not work, replace processor module. |

| Alarm ID | Alarm Description                                                           | Possible Cause                                                                                                                                                                                                       | Solution                                                                                                                                                                                                                                                                                                                       |
|----------|-----------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 283      | Sys - Process disconnected illegally.                                       | Runtime or hardware malfunction. A runtime process has crashed.                                                                                                                                                      | Reload firmware and application and reboot. If failure persists in controller, remove CompactFlash module and reprogram boot loader using the ToolboxST Download Flash Bootloader option, After reinstalling the flash module and rebooting, reload firmware and application. If this does not work, replace processor module. |
| 284      | Process fault detected                                                      |                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                |
| 285      | H/W watchdog fault occurred                                                 |                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                |
| 286      |                                                                             |                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                |
| 291      | Frame Sequencer Arm Failure                                                 |                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                |
| 292      | A seq client did not respond to an overrun event prior to the next frame    |                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                |
| 293      | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | I/O pack is waiting to obtain a network address from the controller using DHCP. This could be a network problem, a controller problem, a pack not configured correctly, or an incorrect ID (barcode).                | Check that controller is on line. Confirm that correct terminal board ID is present in ToolboxST. Check IONet (switches, cables).                                                                                                                                                                                              |
| 295      | IOPACK - The FPGA is not generating an I/O interrupt                        | Internal to the I/O pack there is a FPGA that controls I/O hardware. The logic in the FPGA generates an interrupt to the processor requesting that the I/O be serviced. That interrupt is not occurring as expected. | Rebuild system and download to pack. If problem continues, replace pack (there may be a hardware problem with the FPGA).                                                                                                                                                                                                       |
| 301      | IO pack - XML files are missing                                             | I/O pack IO configuration files missing                                                                                                                                                                              | Rebuild system and download application and configuration to pack.                                                                                                                                                                                                                                                             |
| 337      | EGD Output exchange disagreement detected                                   |                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                |
| 339      | IoPack App SSO signals are not being received                               | The controller is not sending system signal outputs to the pack each frame.                                                                                                                                          | Verify that the Appmgr and/or Ionet-EGD has not terminated by checking the Diagnostic - Error Log. Verify that ionet-egd communications is healthy.                                                                                                                                                                            |
| 342      | IoPack App compatibility code mismatch                                      | The compatibility codes from the firmware and toolbox do not agree as seen by the App Process                                                                                                                        | Compress the variables from ToolboxST and download the application code as well as the firmware for the pack.                                                                                                                                                                                                                  |
| 345      | IoPack App static config data CRC mismatch                                  | The static data used by the App Process has been modified and the CRC on that data region is no longer valid.                                                                                                        | If this problem persists, the Dynamic Ram memory on the pack may be suspect. Replace the pack.                                                                                                                                                                                                                                 |
| 346      | Packet loss on network exceeded [ ]                                         | An excessive amount of Ethernet packets have been lost on the ionet Ethernet                                                                                                                                         | Check the network configuration and switches for problems                                                                                                                                                                                                                                                                      |
| 351      | IoPack App Periodic thread [ ] timing overrun                               | A thread that is scheduled at a periodic rate has not completed before the start of the next scheduling period.                                                                                                      |                                                                                                                                                                                                                                                                                                                                |

| Alarm ID | Alarm Description                                               | Possible Cause                                                                                                                                                                      | Solution                                                                                                                                 |
|----------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 357      | Sequencer client out-of-order execution detected                |                                                                                                                                                                                     |                                                                                                                                          |
| 358      | Sequencer client execution underrun detected                    |                                                                                                                                                                                     |                                                                                                                                          |
| 359      | Sequencer client execution overrun detected                     |                                                                                                                                                                                     |                                                                                                                                          |
| 360      | Sequencer frame period out-of-bounds (+/- 15%%) detected        |                                                                                                                                                                                     |                                                                                                                                          |
| 361      | Sequencer frame state timeout out-of-bounds (+/- 15%%) detected |                                                                                                                                                                                     |                                                                                                                                          |
| 362      | Sequencer frame number skip detected                            |                                                                                                                                                                                     |                                                                                                                                          |
| 365      | IO APPMGR - terminated                                          | The application manager process has terminated.                                                                                                                                     | Check the Error diagnostic log for the reason why the segment has terminated.                                                            |
| 366      | IO APPMGR - initialization failure                              | The application manager detected an error during initialization. The most common cause of this problem is that this process could not attach to shared memory from other processes. | Verify that no other processes have terminated.                                                                                          |
| 367      | IO APPMGR - Can not access HSSL Comm link                       | The application manager was not able to open the high speed serial link driver.                                                                                                     | Check HSSL link cables. If problem persists, replace the UCSA card.                                                                      |
| 368      | IO APPMGR - Egd input header size mismatch                      | The controller has sent a communication packet to the Io Pack with the wrong type of message header.                                                                                | Compress the variables from ToolboxST and download the application code.                                                                 |
| 369      | IO APPMGR - Unable to Export Exchange [ ]                       | The IO Pack encountered an error sending data to the controller.                                                                                                                    | Verify that the Ethernet cables and switches are correct and that the IO Pack is defined in the controller                               |
| 370      | IO APPMGR - Unable to Import Exchange [ ]                       | The IO Pack encountered an error receiving data from the controller.                                                                                                                | Verify that the Ethernet cables and switches are correct and that the IO Pack is defined in the controller                               |
| 371      | IO APPMGR - SSI signals are not being updated                   | The application task for the IO pack is not updating the system signal inputs, between updates to the controller.                                                                   | Verify that the application task has not quit by checking the Diagnostic - Error Log under advanced diagnostics.                         |
| 372      | IO APPMGR - static data structure CRC mismatch                  | The controller is not sending system signal outputs to the pack each frame.                                                                                                         | Verify that the Mapper and/or Ionet-EGD has not by checking the Diagnostic - Error Log. Verify that ionet-egd communications is healthy. |
| 373      | IO APPMGR - IO compatibility code mismatch                      | The compatibility codes from the firmware and the ToolboxST configuration do not agree as seen by the Appmgr Process                                                                | Compress the variables from ToolboxST and download the application code as well as the firmware for the pack.                            |
| 445      | Incorrect or Missing Terminal Board on HSSL link 1              | The acquisition card on Link 1 is not connected or does not agree with the ToolboxST configuration.                                                                                 | Verify that the acquisition card is connected to the appropriate HSSL connector on the UCSA.                                             |
| 448      | Bad Board Id Barcode found on HSSL link 1                       | The barcode on the acquisition card connected to link 1 does not agree with those provided in the ToolboxST configuration.                                                          | Verify that the correct acquisition card is connected to the link and that the correct barcode has been entered in ToolboxST.            |
| 451      | Appmgr: Communication Lost on HSSL Link 1                       | The PMVE can no longer communicate with the acquisition card on link 1.                                                                                                             | Verify that the Ethernet cable is connected and that the acquisition card is healthy.                                                    |



| Alarm ID                                    | Alarm Description                      | Possible Cause | Solution |
|---------------------------------------------|----------------------------------------|----------------|----------|
| Sequencer client execution overrun detected | R Controller-Net A: exchange timed out |                |          |
| 1009                                        | S Controller-Net A: exchange timed out |                |          |
| 1010                                        | T Controller-Net A: exchange timed out |                |          |
| 1264                                        | R Controller-Net B: exchange timed out |                |          |
| 1265                                        | S Controller-Net B: exchange timed out |                |          |
| 1266                                        | T Controller-Net B: exchange timed out |                |          |

## ***SAMB Acoustic Monitoring Input***

### ***Functional Description***

The Mark\* VIe Acoustic Monitoring (SAMB) terminal board is a dual terminal board providing 18 inputs for the Acoustic Monitoring System. SAMB provides two terminal points per input channel for a maximum of 18 channels on 36 terminals. It also provides an additional 18 buffered outputs on 36 terminals to connect external instrumentation for monitoring the ac voltage signal that represents the dynamic pressure signals from the combustor. SAMB includes passive electromagnetic interference (EMI) filters to protect against very high frequency noise generated by external sources.

SAMB includes the following features:

- Eighteen signal interface channels for acoustic monitoring, supporting dedicated-dual configuration
- Channels 1 – 9 are configurable to support PCB Piezotronics<sup>®</sup> sensors or charge converter signal amplifier (CCSA) outputs. Sensor power for the PCB sensors is independent of the sensor power for channels 10 – 18.
- Channels 10 – 18 are configurable to support PCB Piezotronics sensors or CCSA outputs. Sensor power for the PCB sensors is independent of the sensor power for channels 1 – 9.
- Eighteen buffered outputs providing ac signal content of the dynamic pressure signals without dc bias voltage
- Thirty-six Euro-style terminal points for the customer inputs
- Thirty-six Euro-style terminal points for the buffered outputs
- EMI protection for all inputs
- EMI filtered inputs fanned to the A and B slots

## Installation

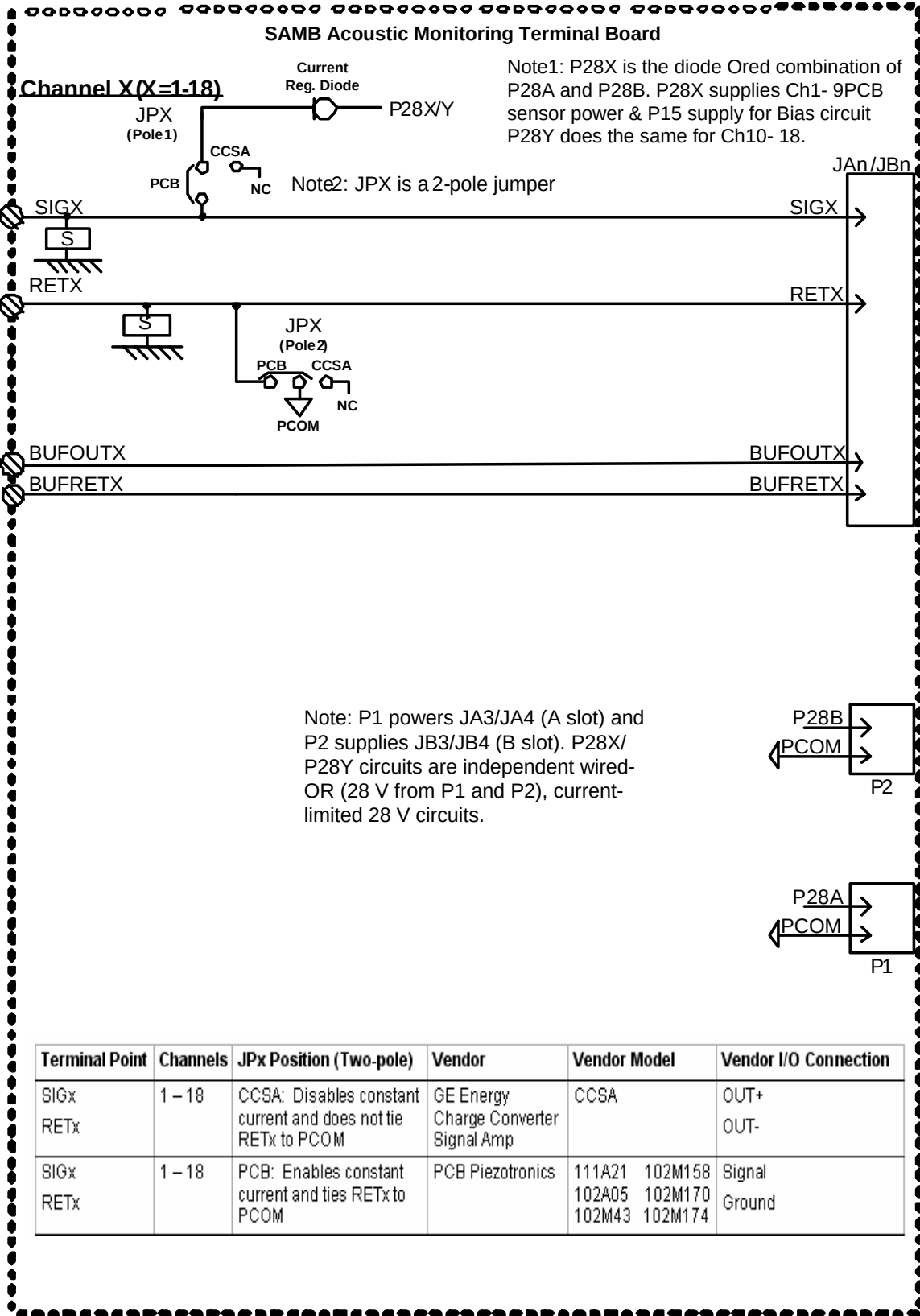
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**Note** A GE field service technician should install the PAMC. Technicians should refer to Support Central website *Acoustic Monitoring Module (PAMC) Installation* in a Mark VIe Control, for complete installation instructions.

The figure, *SAMB Acoustic Monitoring Terminal Board*, shows the functionality of one of the 18 channels supported by SAMB and PAMC. Connect the CCSA or PCB sensors and the buffered outputs to the terminal blocks, as described in the table, *Terminal Point Definitions*.

---

Hardware jumpers connect the constant current source to the SIGx line for the PCB sensors. Each channel has hardware jumper, JPx (where x equals the input number). The jumper should be in the CCSA position if the GE CCSA for Endevco<sup>®</sup> sensors or any other voltage output device is used. The jumper should be in the PCB position if a PCB sensor or any other current output device is used.



SAMB Acoustic Monitoring Terminal Board

*Terminal Variable Definitions*

| Ch. # | Variable | Signal   | Description             | Variable | Signal | Description                      |
|-------|----------|----------|-------------------------|----------|--------|----------------------------------|
| 1     | 1        | BUFOUT1  | Buffered output, signal | 2        | SIG1   | Dynamic pressure voltage, signal |
|       | 3        | BUFRET1  | Buffered output, return | 4        | RET1   | Dynamic pressure voltage, return |
| 2     | 5        | BUFOUT2  | Buffered output, signal | 6        | SIG2   | Dynamic pressure voltage, signal |
|       | 7        | BUFRET2  | Buffered output, return | 8        | RET2   | Dynamic pressure voltage, return |
| 3     | 9        | BUFOUT3  | Buffered output, signal | 10       | SIG3   | Dynamic pressure voltage, signal |
|       | 11       | BUFRET3  | Buffered output, return | 12       | RET3   | Dynamic pressure voltage, return |
| 4     | 13       | BUFOUT4  | Buffered output, signal | 14       | SIG4   | Dynamic pressure voltage, signal |
|       | 15       | BUFRET4  | Buffered output, return | 16       | RET4   | Dynamic pressure voltage, return |
| 5     | 17       | BUFOUT5  | Buffered output, signal | 18       | SIG5   | Dynamic pressure voltage, signal |
|       | 19       | BUFRET5  | Buffered output, return | 20       | RET5   | Dynamic pressure voltage, return |
| 6     | 21       | BUFOUT6  | Buffered output, signal | 22       | SIG6   | Dynamic pressure voltage, signal |
|       | 23       | BUFRET6  | Buffered output, return | 24       | RET6   | Dynamic pressure voltage, return |
| 7     | 25       | BUFOUT7  | Buffered output, signal | 26       | SIG7   | Dynamic pressure voltage, signal |
|       | 27       | BUFRET7  | Buffered output, return | 28       | RET7   | Dynamic pressure voltage, return |
| 8     | 29       | BUFOUT8  | Buffered output, signal | 30       | SIG8   | Dynamic pressure voltage, signal |
|       | 31       | BUFRET8  | Buffered output, return | 32       | RET8   | Dynamic pressure voltage, return |
| 9     | 33       | BUFOUT9  | Buffered output, signal | 34       | SIG9   | Dynamic pressure voltage, signal |
|       | 35       | BUFRET9  | Buffered output, return | 36       | RET9   | Dynamic pressure voltage, return |
| 10    | 37       | BUFOUT10 | Buffered output, signal | 38       | SIG10  | Dynamic pressure voltage, signal |
|       | 39       | BUFRET10 | Buffered output, return | 40       | RET10  | Dynamic pressure voltage, return |
| 11    | 41       | BUFOUT11 | Buffered output, signal | 42       | SIG11  | Dynamic pressure voltage, signal |
|       | 43       | BUFRET11 | Buffered output, return | 44       | RET11  | Dynamic pressure voltage, return |
| 12    | 45       | BUFOUT12 | Buffered output, signal | 46       | SIG12  | Dynamic pressure voltage, signal |
|       | 47       | BUFRET12 | Buffered output, return | 48       | RET12  | Dynamic pressure voltage, return |
| 13    | 49       | BUFOUT13 | Buffered output, signal | 50       | SIG13  | Dynamic pressure voltage, signal |
|       | 51       | BUFRET13 | Buffered output, return | 52       | RET13  | Dynamic pressure voltage, return |
| 14    | 53       | BUFOUT14 | Buffered output, signal | 54       | SIG14  | Dynamic pressure voltage, signal |
|       | 55       | BUFRET14 | Buffered output, return | 56       | RET14  | Dynamic pressure voltage, return |
| 15    | 57       | BUFOUT15 | Buffered output, signal | 58       | SIG15  | Dynamic pressure voltage, signal |
|       | 59       | BUFRET15 | Buffered output, return | 60       | RET15  | Dynamic pressure voltage, return |
| 16    | 61       | BUFOUT16 | Buffered output, signal | 62       | SIG16  | Dynamic pressure voltage, signal |
|       | 63       | BUFRET16 | Buffered output, return | 64       | RET16  | Dynamic pressure voltage, return |
| 17    | 65       | BUFOUT17 | Buffered output, signal | 66       | SIG17  | Dynamic pressure voltage, signal |
|       | 67       | BUFRET17 | Buffered output, return | 68       | RET17  | Dynamic pressure voltage, return |
| 18    | 69       | BUFOUT18 | Buffered output, signal | 70       | SIG18  | Dynamic pressure voltage, signal |
|       | 71       | BUFRET18 | Buffered output, return | 72       | RET18  | Dynamic pressure voltage, return |

## Operation

SAMB inputs an ac voltage signal from the CCSA proportional to the dynamic pressure sensed by the Endevco pressure sensors. SAMB inputs the dynamic pressure directly from PCB pressure sensors as an ac voltage riding on a dc bias voltage. The terminal board provides configuration options to support the hardware listed in the following table:

*SAMB Connections*

| Terminal Point | Channels | JPx Position (Two-pole)                                       | Vendor                                | Vendor Model               |                               | Vendor I/O Connection |
|----------------|----------|---------------------------------------------------------------|---------------------------------------|----------------------------|-------------------------------|-----------------------|
| SIGx<br>RETx   | 1 – 18   | CCSA: Disables constant current and does not tie RETx to PCOM | GE Energy Charge Converter Signal Amp | CCSA                       |                               | OUT+<br>OUT-          |
| SIGx<br>RETx   | 1 – 18   | PCB: Enables constant current and ties RETx to PCOM           | PCB Piezotronics                      | 111A21<br>102A05<br>102M43 | 102M158<br>102M170<br>102M174 | Signal<br>Ground      |

Each channel provides a constant current source that can be connected to SIGx (where x is the channel number) for the PCB sensors. The jumper JPx (where x equals the channel number) is a two-pole jumper that controls the constant current power supply and whether RETx is tied to the power ground, PCOM. When JPx is in the CCSA position, the constant current is disabled and RETx is not tied to PCOM. When JPx is in the PCB position, the constant current is connected to SIGx, providing approximately 3 mA of current to power the PCB sensor. The RETx line is tied to PCOM to provide a return path for the constant current.

A high impedance dc bias allows PAMB to detect an open connection between the charge amplifier (or PCB sensor) and the SAMB terminal board. Each input circuit has +28 V dc bias only.

## Specifications

| Item                        | Specification                                                                    |
|-----------------------------|----------------------------------------------------------------------------------|
| Input channels              | 18 dynamic pressure inputs                                                       |
| Output channels             | 18 buffered outputs                                                              |
| Power inputs                | 2 P28 inputs, each with a 2-pin connector                                        |
| Bias circuit                | P28 on each channel with < 0.2 % dc error                                        |
| Dc output gain              | 1 ±0.5%                                                                          |
| Allowable offset on outputs | 30 mV ±10%                                                                       |
| Output impedance            | 40 Ω ±50%                                                                        |
| Test points                 | 2 with > ±10 V dc range, < 0.5% error tolerance, and = 2.5 mV / count resolution |
| <b>Physical</b>             |                                                                                  |
| Size                        | 14.3 cm high x 23.1 cm wide (5.625 in x 9.1 in)                                  |
| Temperature                 | -30 to 65°C (-22 to 149 °F)                                                      |
| Cooling                     | Free air convection                                                              |
| Humidity                    | 5 to 95% non-condensing                                                          |

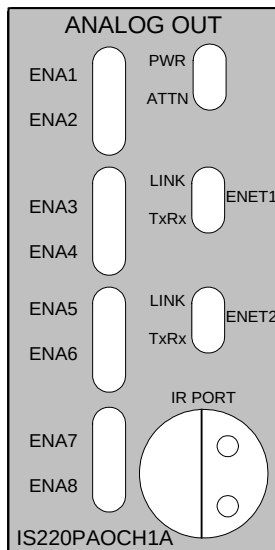
## ***Diagnostics***

The SAMB terminal board has its own ID device, which is interrogated by PAMB. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the JA4 or JB4 connector location. This ID is checked as part of the power-up diagnostics.

# PAOC Analog Output

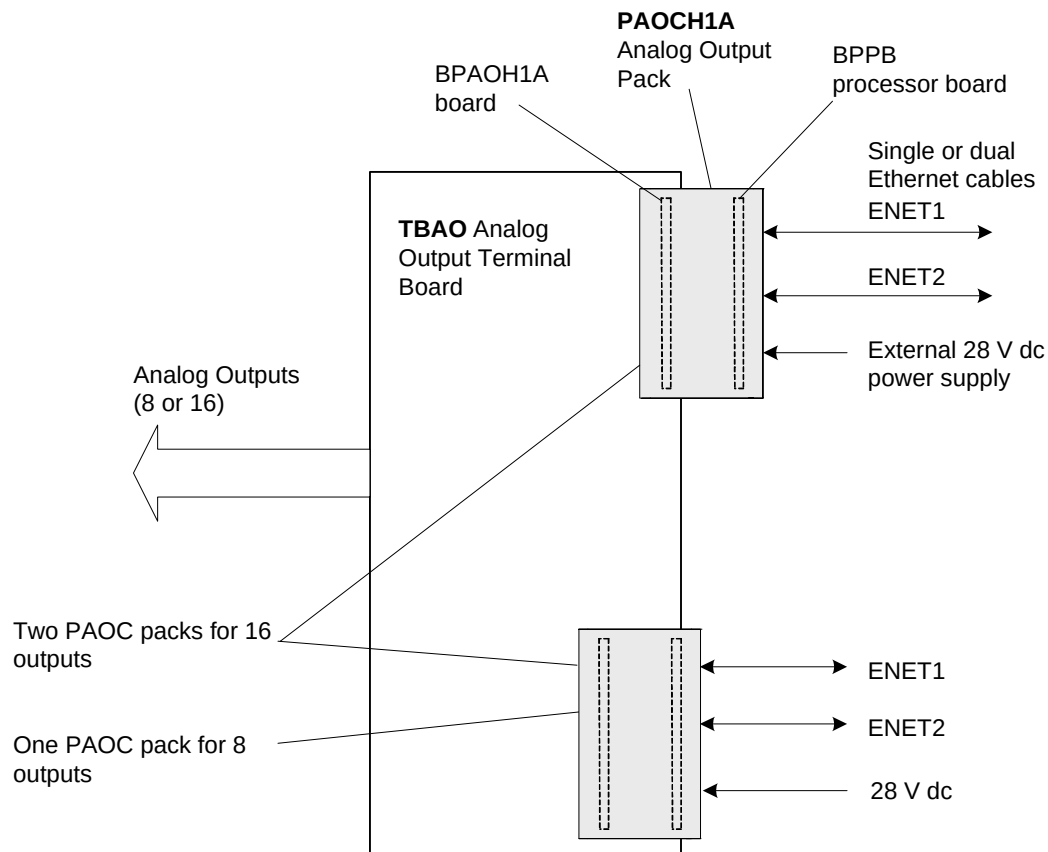
## PAOC Analog Output

### Functional Description



The Analog Output (PAOC) pack provides the electrical interface between one or two I/O Ethernet networks and an analog output terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs and an acquisition board pair specific to the analog output function. The pack is capable of providing up to eight simplex 0-20 mA current loop outputs and includes an analog to digital converter for current feedback from each output.

Input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PAOCH1A is compatible with the analog output terminal board TBAOH1C, and the STAO board, but not the DIN-rail mounted DTAO board. The following table gives details of the compatibility:

| Terminal Board | TBAOH1C     | DTAO      | STAOH1A     |
|----------------|-------------|-----------|-------------|
| Control mode   | Simplex-yes | Dual - no | TMR-no      |
|                | No          | No        | Simplex-yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

While the PAOC will mount on a TBAOH1A or TBAOH1B terminal board, the pack will not realize full accuracy of the analog signals due to circuit differences between the terminal board revisions. For this reason, the PAOC is only compatible with the H1C version of TBAO and will report a board compatibility problem with any of the earlier revisions. No physical damage will result if a PAOC is powered up on an older board in error.

## Installation

### ➤ To install the PAOC pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PAOC I/O pack for simplex or three PAOC I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

---

**Note** The PAOC mounts directly to a Mark VIe terminal board. Simplex terminal boards have a single DC-37 pin connector that receives the PAOC. TMR capable terminal boards have six DC-37 pin connectors, of which only two may be used by PAOC packs, one for the first eight outputs and the other for the second eight outputs. The PAOC is a simplex-only pack.

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# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

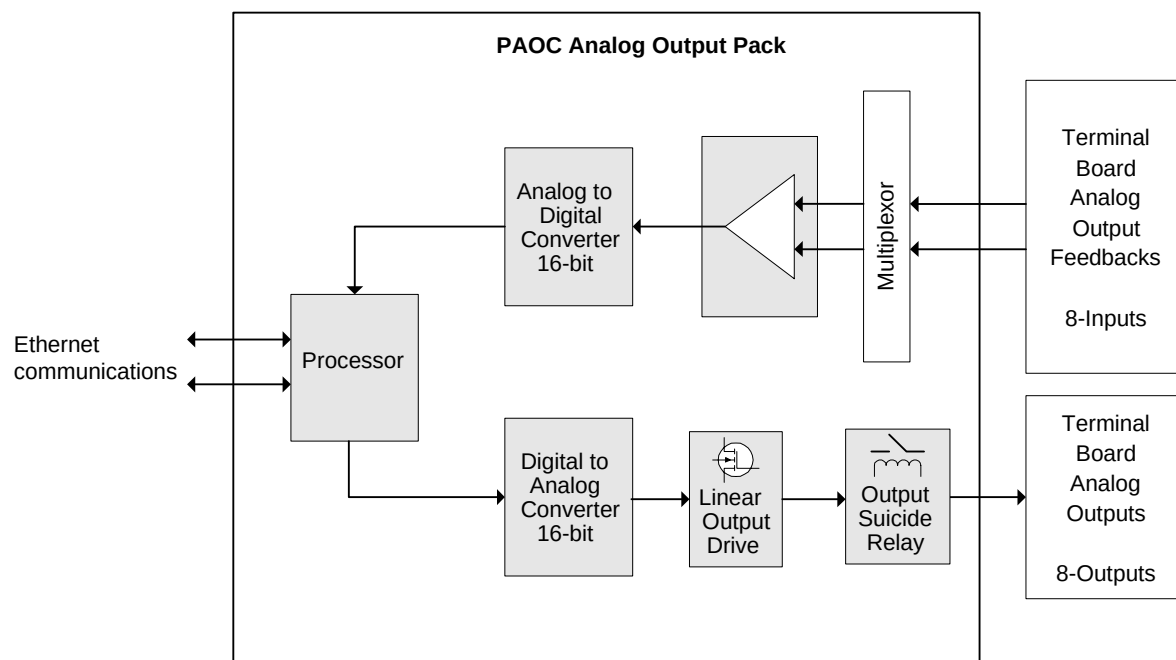
The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

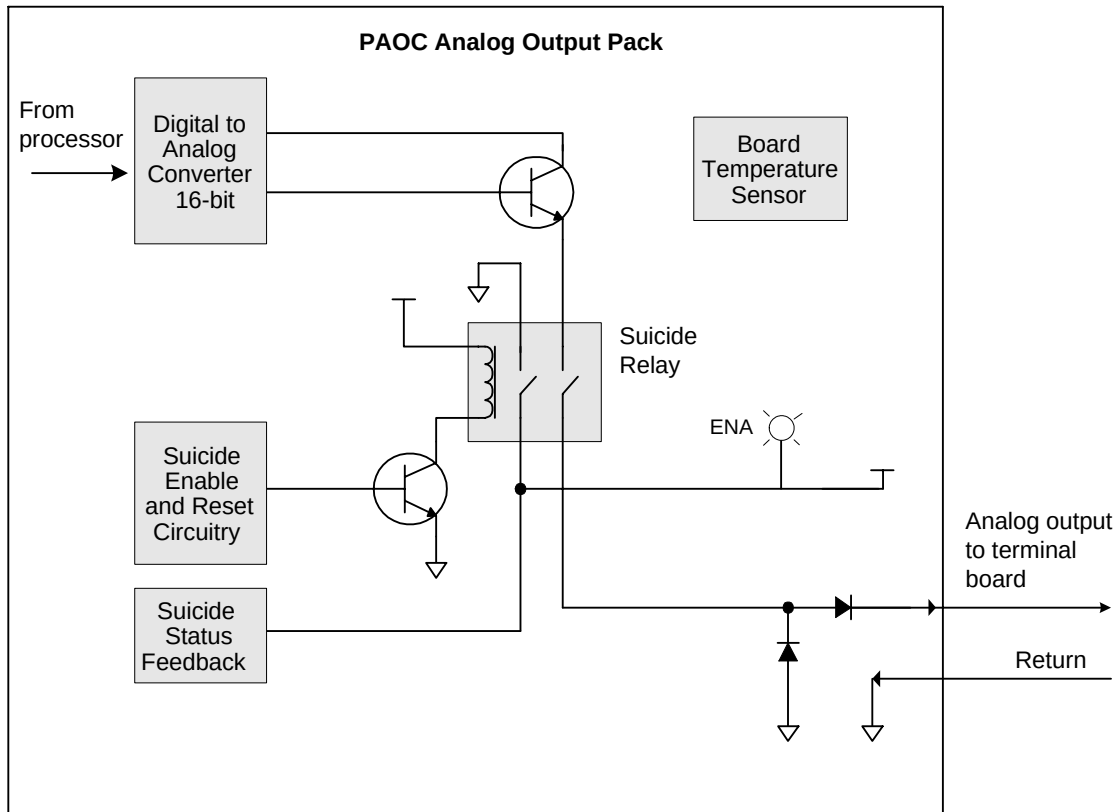
An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## Analog Output Hardware

The PAOC includes eight simplex 0-20 mA analog outputs capable of 18 V compliance. A 16-bit digital-to-analog converter (DAC) commands and drives the output current with an external transistor amplifier. A board temperature sensor is included to warn the control if the pack's internal temperature becomes excessive.

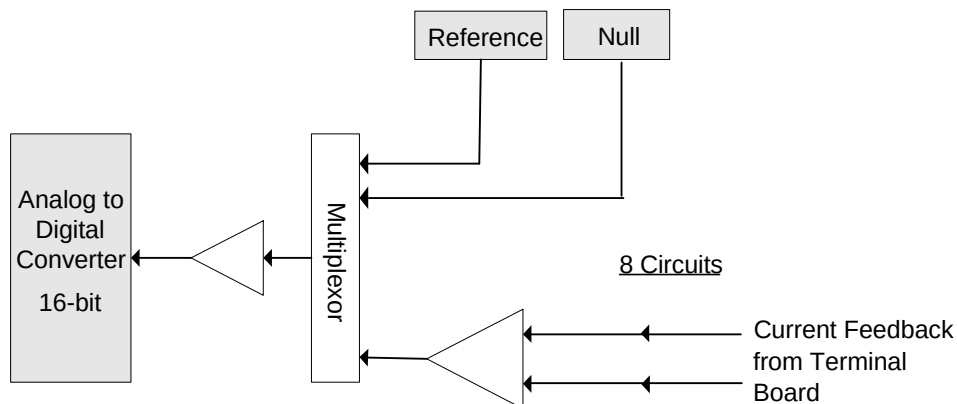


Each analog output circuit also includes a normally open mechanical relay to enable or disable operation of the output. When the disable relay is de-activated, the output opens through the relay, open-circuiting that PAOC's analog output from the customer load that is connected to the terminal board. The mechanical relay's second normally-open contact is used as a status signal to indicate position of the relay with an LED.



### Current Feedback Hardware

The PAOC includes current feedback monitoring for each of the eight simplex 0-20 mA analog outputs. A 50  $\Omega$  resistor on the terminal board and a 16-bit analog to digital converter is used to sense and monitor the output current.



## Thermal De-rating Guidelines

With eight linear, high-compliance analog outputs, the PAOC pack is subject to application limitations depending on its potential ambient environment. I/O packs are specified to have an operating temperature range of -30 to 65°C (-22 to +149 °F), as measured external to the pack.

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**Note** This is the pack external temperature inside the cabinet, not cabinet external temperature.

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Depending on the application, and due to its dense triple board configuration, the PAOC packs ambient environment maximum must be de-rated. The following is a list of output configurations and the appropriate de-rating that must be applied. The minimum output impedance is defined as the minimum series equivalent resistance of the customers load, as seen by the terminal board screws across the output range of 0-20 mA.

Maximum PAOC pack ambient temperature in degrees celsius (degrees fahrenheit) inside cabinet:

|                   |   | Minimum Output Resistance (per output, ohms) |              |              |              |
|-------------------|---|----------------------------------------------|--------------|--------------|--------------|
|                   |   | 0                                            | 250          | 500          | 1000         |
| Number of outputs | 1 | 65° (149 °F)                                 | 65° (149 °F) | 65° (149 °F) | 65° (149 °F) |
|                   | 2 | 60° (140 °F)                                 | 65° (149 °F) | 65° (149 °F) | 65° (149 °F) |
|                   | 3 | 60° (140 °F)                                 | 60° (140 °F) | 60° (140 °F) | 65° (149 °F) |
|                   | 4 | 55° (131 °F)                                 | 60° (140 °F) | 60° (140 °F) | 65° (149 °F) |
|                   | 5 | 55° (131 °F)                                 | 55° (131 °F) | 60° (140 °F) | 60° (140 °F) |
|                   | 6 | 50° (122 °F)                                 | 55° (131 °F) | 55° (131 °F) | 60° (140 °F) |
|                   | 7 | 50° (122 °F)                                 | 50° (122 °F) | 55° (122 °F) | 60° (140 °F) |
|                   | 8 | 45° (104 °F)                                 | 50° (122 °F) | 55° (122 °F) | 55° (122 °F) |

## ID Line

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## Power Management

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly (¼ cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed (¾ cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Connectors

The pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

## Specifications

The following table provides information specific to the PAOC.

| Item                     | Specification                                                                                                                       |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels       | Eight current output channels, single-ended (one side connected to common)                                                          |
| Analog outputs           | 0-20 mA, up to 900 Ω burden (18 V compliance)<br>Response better than 50 rad/sec                                                    |
| Accuracy                 | ±0.5% over -30 to 65°C (-22 to +149 °F) temperature and 0 to 900 Ω load impedance<br>±0.25% typical at 25°C (+77 °F) and 500 Ω load |
| D/A converter resolution | 16-bit resolution                                                                                                                   |
| Frame rate               | 100 Hz on all eight outputs                                                                                                         |
| <b>Physical</b>          |                                                                                                                                     |
| Size                     | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)                                                            |
| Temperature              | -30 to +65°C (-22 to +149 °F)                                                                                                       |
| Technology               | Surface mount                                                                                                                       |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on preset (non-configurable) high and low levels near the end of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. The logic signal, L3DIAG\_xxxx, refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limits.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

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**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

---

| Parameter              | Description                                  | Choices                                  |
|------------------------|----------------------------------------------|------------------------------------------|
| <b>PAOC-Mod_Config</b> |                                              |                                          |
| <b>AnalogOut1</b>      | First of eight analog outputs - Board Point  | Point Edit (Output FLOAT)                |
| Output_MA              | Output mA selection                          | Unused, 0-20 mA, 0-200 mA                |
| Low_MA                 | Output mA at low value                       | 0 to 200 mA                              |
| Low_Value              | Output in engineering units at low mA        | -3.4082e + 038 to 3.4028e + 038          |
| High_MA                | Output mA at high value                      | 0 to 200 mA                              |
| High_Value             | Output value in engineering units at high mA | -3.4082e + 038 to 3.4028e + 038          |
| D/A_ErrLimit           | DA error threshold in percent                | 0 to 100 %                               |
| Suicide_Enab           | Suicide enable for faulty output             | Enable, disable                          |
| Output_State           | State of the outputs when off-line           | PwrDownMode, HoldLastVal, Output_Value   |
| Output_Value           | Pre-determined value for the outputs         |                                          |
| DitherAmpl             | Dither in % current of scaled output mA      | 0 to 10                                  |
| Dither_Freq            | Dither rate in Hertz                         | Unused, 12.5, 25.0<br>33.33, 50.0, 100.0 |

| Parameter           | Description                          | Choices   |       |
|---------------------|--------------------------------------|-----------|-------|
| IS220PAOC PointDefs | Description                          | Direction | Type  |
| L3DIAG_PAOC         | I/O diagnostic indication            | Input     | BIT   |
| LINK_OK_PAOC        | I/O link okay indication             | Input     | BIT   |
| ATTN_PAOC           | I/O attention indication             | Input     | BIT   |
| IOPackTmp           | I/O pack temperature                 | Input     | FLOAT |
| OutSuicide1         | Status of suicide relay for output 1 | Input     | BIT   |
| :                   | :                                    | Input     | BIT   |
| Out1MA              | Measure output current in mA         | Input     | FLOAT |
| :                   | :                                    | Input     | FLOAT |

## Alarms

### PAOC Specific Alarms

The following alarms are specific to the PAOC I/O pack.

| Alarm ID | Alarm Description                                                               | Possible Cause                                                                                                                                                        | Solution                                                                                                                                                                                                                                        |
|----------|---------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32-41    | Analog Input {0:F0} unhealthy                                                   |                                                                                                                                                                       |                                                                                                                                                                                                                                                 |
| 46-53    | Output {0:F0} Feedback current varies from reference current                    | <p>&lt;b&gt;D/A_ErrLimit&lt;/b&gt; is not configured properly (set too low).</p> <p>Analog output is not connected properly.</p> <p>Board failure (D/A converter)</p> | <p>Verify &lt;b&gt;D/A_ErrLimit&lt;/b&gt; settings.</p> <p>Verify analog output connections.</p> <p>Replace I/O pack.</p>                                                                                                                       |
| 54-61    | Output {0:F0} Feedback current is excessive                                     |                                                                                                                                                                       |                                                                                                                                                                                                                                                 |
| 62-69    | Output {0:F0} Suicide relay non-functional                                      | Board failure (Relay or driver)                                                                                                                                       | Replace I/O pack.                                                                                                                                                                                                                               |
| 70-77    | Output {0:F0} Suicide Active                                                    |                                                                                                                                                                       |                                                                                                                                                                                                                                                 |
| 78       | Acquisition Board Temperature {0:F1} deg F exceeds the max limit ({1:F1} deg F) | The internal temperature on the PAOC has exceeded the maximum temperature limit of 185 deg F (85 deg C).                                                              | The environmental controls applied to the cabinet containing the I/O pack should be checked. Pack operation will continue correctly beyond these temperature limits but long term operation at elevated temperatures may reduce equipment life. |
| 79       | P15V PowerSupply Not OK                                                         | Board failure (D/A converter or power supply)                                                                                                                         | Replace I/O pack.                                                                                                                                                                                                                               |
| 80       | N15V PowerSupply Not OK                                                         | Board failure (D/A converter or power supply)                                                                                                                         | Replace I/O pack.                                                                                                                                                                                                                               |
| 96       | ConfigCompatCode mismatch                                                       | A tre file has been installed that is incompatible with the PAOC firmware. Either the tre file or firmware must change. Contact the factory.                          |                                                                                                                                                                                                                                                 |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need: [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |



| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

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## ***TBAO Analog Output***

### ***Functional Description***

The Analog Output (TBAO) terminal board supports 16 analog outputs with a current range of 0-20 mA. Current outputs are generated by the I/O processor, which can be local (Mark\* VIe control) or remote (Mark VI control). The outputs have noise suppression circuitry to protect against surge and high-frequency noise. TBAO has two barrier-type terminal blocks for customer wiring and six D-type cable connectors.

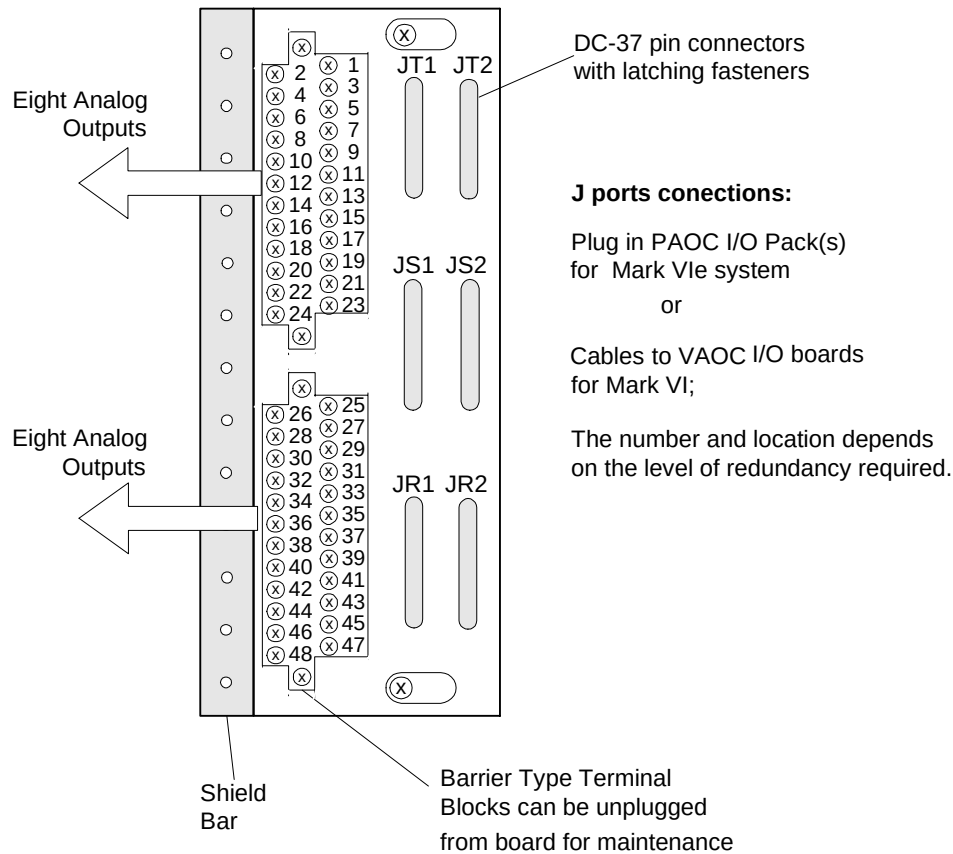
### ***Mark VI Systems***

In Mark VI systems, TBAO works with VAOC processor and supports simplex and TMR applications. Cables with molded plugs connect TBAO to the VME rack where the VAOC board is located. In TMR systems, TBAO is cabled to three VOAC boards.

## Mark VIe Systems

In Mark VIe systems, TBAO works with the PAOC I/O pack and supports simplex applications only. The I/O packs plug into the D-type connectors and communicate over Ethernet with the controller.

Refer to *GEI-100577 Mark VIe Analog Input* for board compatibility.



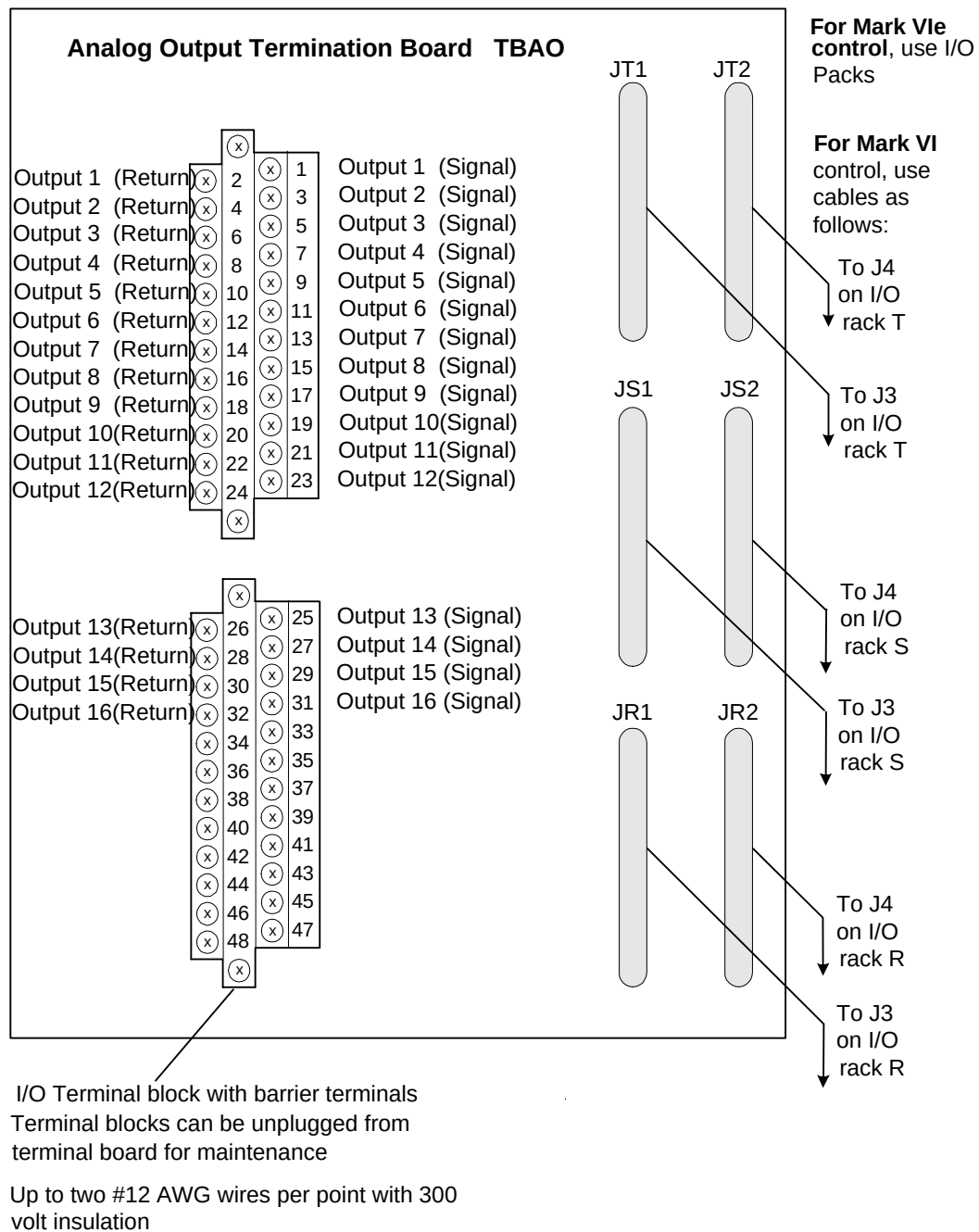
*TBAO Analog Output Terminal Board*

## Installation

Attach TBAO to a vertical mounting plate. Connect the wires for the 16 analog outputs directly to the two I/O terminal blocks mounted on the left of the board. Each point can accept two 3.0 mm (#12AWG) wires with 300 V insulation per point using spade or ring type lugs. Each block is held down with two screws and has 24 terminals. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block. Make cable connections to TBAO follows:

- In Mark VI systems, connect cables with molded plugs to the D-type connectors on the TBAO and to the VME rack where the VAOC processor is located. Use two cables for simplex or six cables for TMR.
- In Mark VIe systems, plug the PAOC I/O packs directly into selected D-type connectors. Special side mounting brackets support the packs.

The following figure shows details of TBAO wiring and cabling.

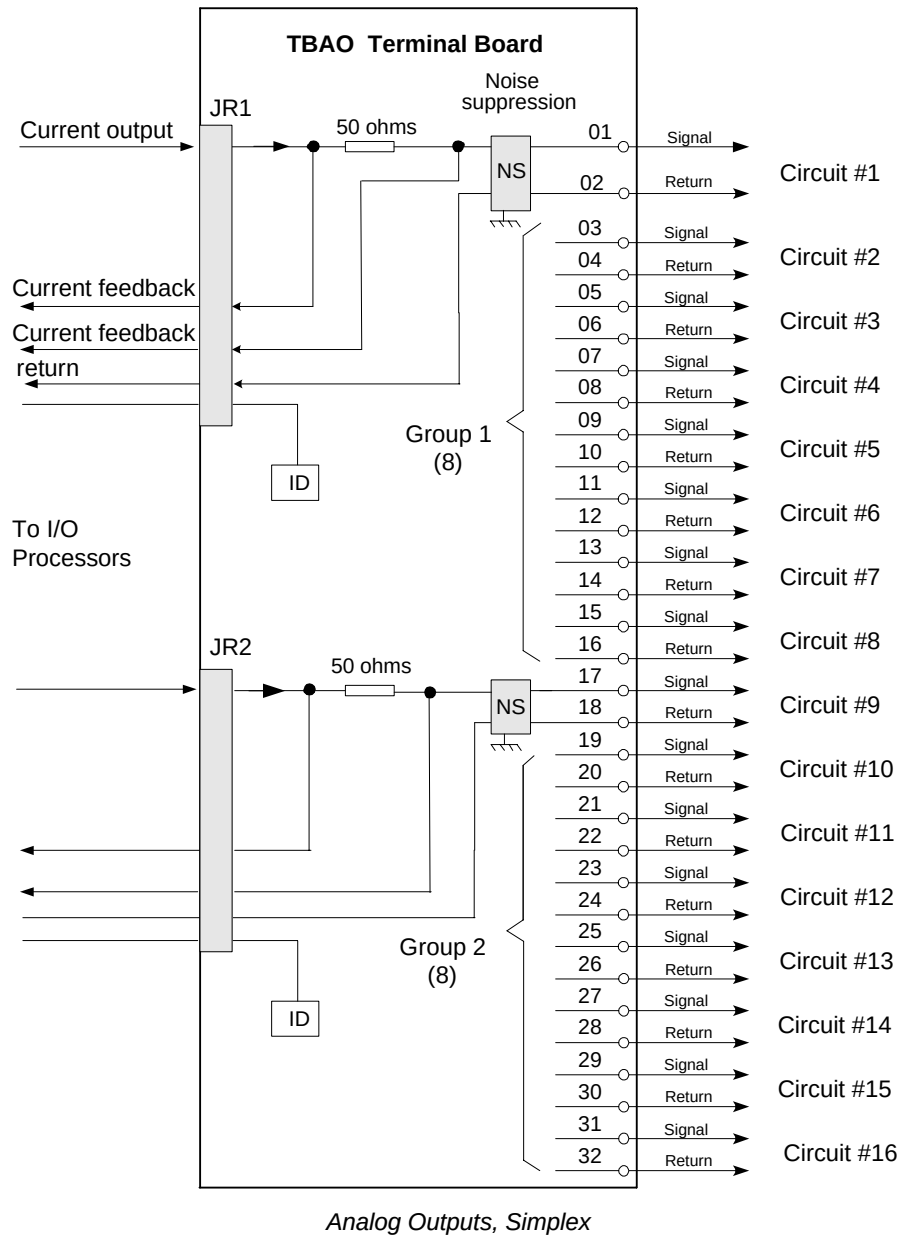


*TBAO Terminal Board Wiring*

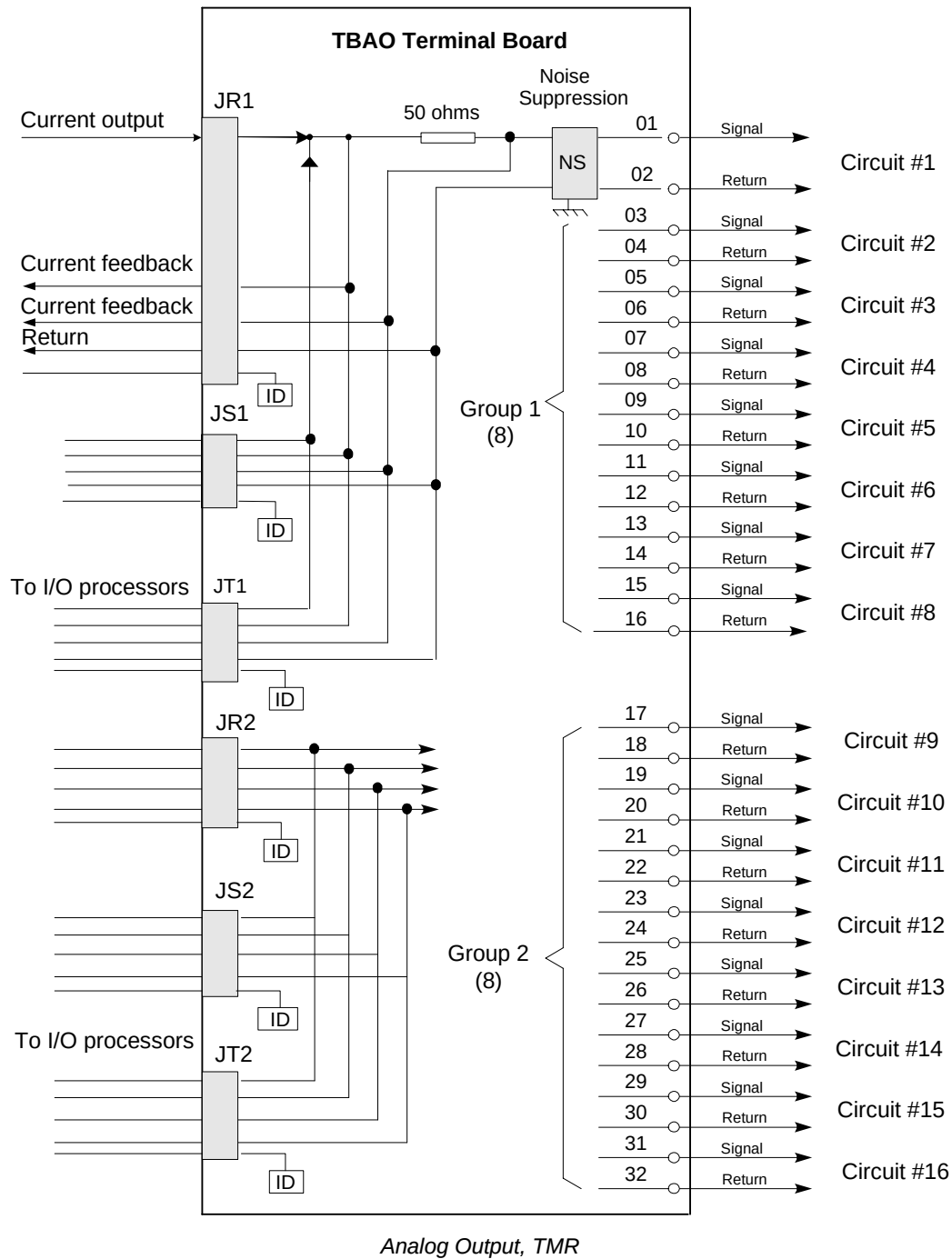
## Operation

TBAO supports 16 analog control outputs. Driven devices should not exceed a resistance of 500  $\Omega$  (900  $\Omega$  if using I/O packs) and can be located up to 300 m (984 ft) from the turbine control cabinet. The VAOC or PAOC contains the D/A converter and drivers that generate the controlled currents. The output current is measured by the voltage drop across a resistor on the terminal board.

Filters reduce high-frequency noise and suppress surge on each output near the point of signal exit. The following figure shows TBAO in a simplex system.



In a TMR system, each analog current output is fed by the sum of the currents from the three I/O processors, as shown in the drawing below. The total output current is measured with a series resistor that feeds a voltage back to each I/O processor. The resulting output is the voted middle value (median) of the three currents.



## Specifications

| Item                     | Specification                                                                                                      |
|--------------------------|--------------------------------------------------------------------------------------------------------------------|
| Number of channels       | 16 current output channels, single-ended (one side connected to common)                                            |
| Analog output current    | 0-20 mA                                                                                                            |
| Customer load resistance | Up to 500 $\Omega$ burden with VOACH1B and TBAOH1B and 900 $\Omega$ burden (18 V compliance) with PAOC and TBAOH1C |
| <b>Physical</b>          |                                                                                                                    |
| Size                     | 10.16 cm wide x 33.02 cm high (4.0 in x 13.0 in)                                                                   |
| Temperature              | -30 to +65°C (-22 to +149 °F)                                                                                      |

## Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

There are no jumpers or hardware settings on the board.

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## STAO Simplex Analog Output

### Functional Description

The Simplex Analog Output (STAO) terminal board is a compact analog output terminal board, designed for DIN-rail or flat mounting. STAO has eight 0-20 mA analog outputs driven by the PAOC I/O pack. The on-board circuits and noise suppression are the same as those on TBAO terminal board. High-density Euro-block type terminal blocks are mounted on the board for wiring to the customer's devices. An on-board ID chip identifies the board to the I/O processor for system diagnostic purposes.

### Mark VIe Systems

In Mark\* VIe systems, the PAOC I/O pack works with the STAO. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet. Only simplex systems are supported.

Refer to *GEI-100577 Mark VIe Analog Output* for board compatibility.

## Installation

The STAO plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN-rail. Optionally, the STAO plus insulator mount on a sheet metal assembly that then bolts directly to a cabinet. Driven devices should not exceed a resistance of 900  $\Omega$  and can be located up to 300 m (984 ft) from the turbine control cabinet. Two types of Euro-block terminal blocks are available:

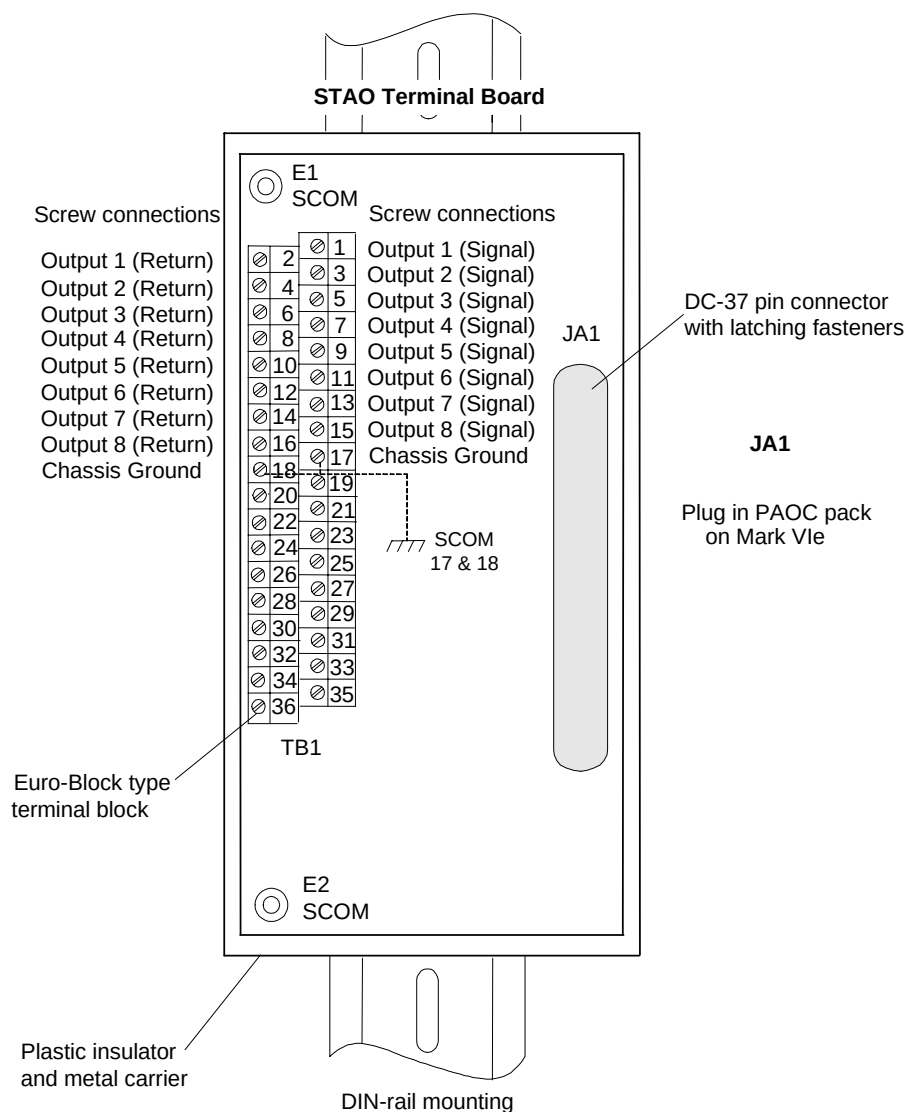
- STAOH1 has a permanently mounted terminal block with 36 terminals.
- STAOH2 has a right angle header accepting a range of commercially available pluggable terminal blocks, for a total of 36 terminals.

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**Note** There is no shield terminal strip with this design.

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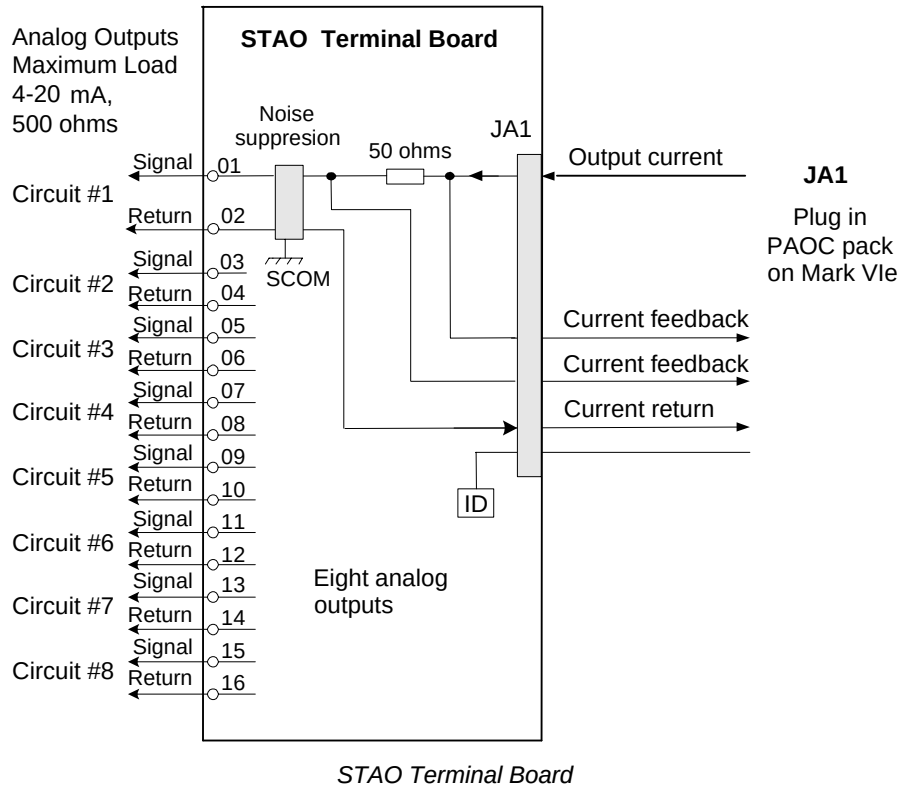
The eight analog outputs are wired directly to the terminal block as shown in the following figure. There are two screws for the SCOM connection. Typically #18 AWG wires (shielded twisted pair) are used. I/O cable shield terminal uses an external mounting bracket supplied by GE or the customer. E1 and E2 are mounting holes for the chassis ground screw connection (SCOM). DIN-type terminal boards can be stacked vertically on the DIN-rail to conserve cabinet space.



STAO Wiring and Cabling

## Operation

STAO supports eight analog control current outputs. On each output, the voltage drop across the local loop current sense resistor is measured and the signal is fed back to the I/O processor that controls the current. Filters reduce high-frequency noise and suppress surge on each output near the point of signal exit. The I/O processor contains the D/A converter and drivers that generate the controlled currents.



## Specifications

| Item                     | Specification                                                              |
|--------------------------|----------------------------------------------------------------------------|
| Number of channels       | Eight current output channels, single-ended (one side connected to common) |
| Analog output current    | 0-20 mA                                                                    |
| Customer load resistance | Up to 900 $\Omega$ burden with PAOC pack                                   |
| <b>Physical</b>          |                                                                            |
| Size                     | 15.9 cm high x 10.2 cm wide (6.25 in x 4.0 in)                             |
| Temperature              | -30 to 65°C (-22 to +149 °F)                                               |
| Technology               | Surface mount                                                              |



## ***Diagnostics***

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no jumpers or hardware settings on the board.

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## ***Notes***

# PCAA Core Analog Module

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## PCAA Core Analog Module

### Functional Description

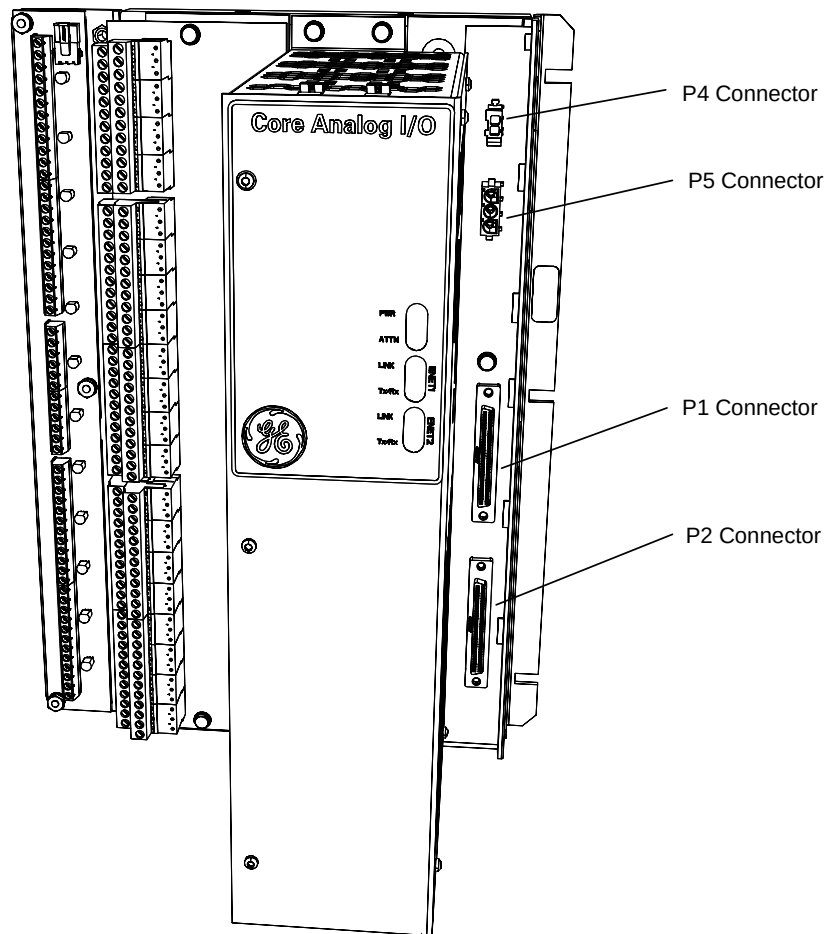
The Core Analog (PCAA) module and associated Core Analog (TCAS and TCAT) terminal board provide a large portion of the analog signal I/O required to operate a gas turbine. PCAA and TCAT provide thermocouple inputs, 4-20 mA current loop I/O, seismic inputs, Linear Variable Differential Transformer (LVDT) excitation and inputs, pulse rate inputs, and servo coil outputs. PCAA may be applied in simplex, dual, and TMR systems. A single TCAT terminal board fans signal inputs to one, two, or three connected PCAA modules. The shield ground and 24 V field power terminals on an adjacent JGPA board supplement the terminals on PCAA and TCAT.

PCAA contains a processor board common to all Mark\* VIe distributed I/O, two application I/O boards, and a terminal board. The complete module is regarded as the least replaceable unit and there is no support provided to diagnose or replace the individual boards making up the module.

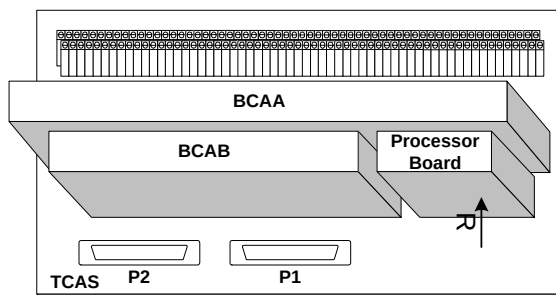
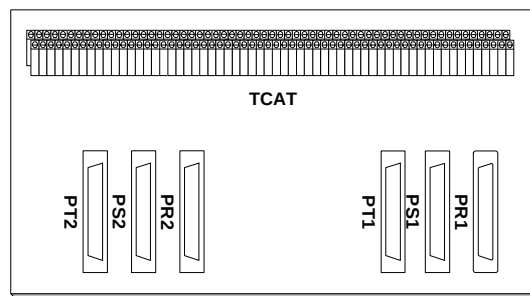
Input to the module is through dual RJ45 Ethernet connectors and 28 V dc power connector P5. Field device I/O is through 120 euro-style box terminals on the module edge. Power for a JGPA board is through connector P4. Module connection to TCAT is through two 68-pin cables on connectors P1 and P2.

The signals on PCAA are separated into two groups. Signal inputs that may be fanned from a single input into a single, dual, or TMR PCAA modules are routed through the TCAT terminal board. Signals that are dedicated to a single PCAA module are wired to the terminals on PCAA. This creates the signal split shown in the following table. It is possible to use PCAA without TCAT if the fanned inputs are not required.

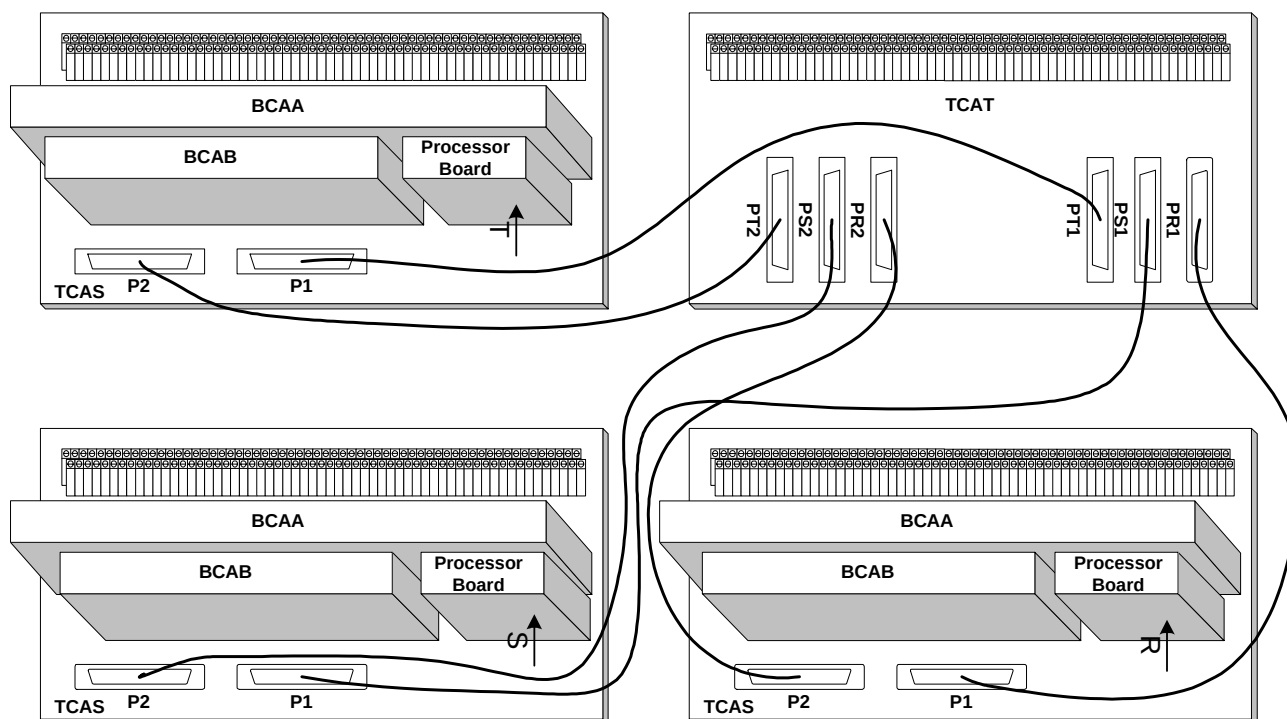
| PCAA Terminals |                                 |               | TCAT Terminals |                                                  |               |
|----------------|---------------------------------|---------------|----------------|--------------------------------------------------|---------------|
| # Signals      | Signal Type                     | Screws/Signal | # Signals      | Signal Type                                      | Screws/Signal |
| 25             | Thermocouples                   | 2             | 12             | Fanned seismic inputs                            | 2             |
| 10             | Analog 4-20 mA inputs           | 2             | 24             | Fanned analog 4-20 mA inputs                     | 2             |
| 2              | Analog 4-20 mA or $\pm 10$ V in | 2             | 12             | 24 V output power @ 25 mA                        | 1             |
| 2              | Analog 4-20 mA outputs          | 2             | 3              | Voting 4-20 mA outputs                           | 2             |
| 1              | $\pm 12$ V power output         | 2             | 12             | Fanned LVDT Feedback                             | 2             |
| 6              | LVDT Excitation outputs         | 2             | 2              | Fanned Mag. Pulse Rate Inputs (servo flow meter) | 2             |
| 6              | Servo coil driver outputs       | 3             | 1              | Common connection                                | 1             |
| 1              | Servo suicide relay input       | 2             |                |                                                  |               |
| 2              | TTL pulse inputs+power          | 4             |                |                                                  |               |



PCAA Core Analog



PCAA-TCAT Connection Diagram - Simplex (PCAA cover omitted to show board relationship)



PCAA-TCAT Connection Diagram - TMR (PCAA cover omitted to show board relationship)

## Compatibility

The PCAA module is fully compatible with all other Mark VIe I/O packs and controllers. PCAA supports the frame rates, redundancy, and networking as shown in the following table.

| PCAA Quantity | IONet Connections | Frame Rate | TCAT Connections | Comments                                            |
|---------------|-------------------|------------|------------------|-----------------------------------------------------|
| Simplex       | One or Two        | 40 ms      | Zero or One      | TCAT optional on simplex configurations             |
| Simplex       | One               | 10 ms      | Zero or One      | Only one IONet at 10 msec frame rates               |
| TMR           | One               | 40 ms      | One              | TMR configurations only support one IONet per PCAA. |
| TMR           | One               | 10 ms      | One              |                                                     |

## ***Installation***

### **➤ To install the PCAA module**

- 1** Securely mount the PCAA module.
- 2** Connect the JGPA power connection to the P4 connector on PCAA.
- 3** Connect the PCAA module to an optional associated TCAT terminal board using two 68-pin cables on connectors P1 and P2. Connectors on TCAT are paired by a network connection. PR1 and PR2 go to a PCAA connected to the R controller network, PS1 and PS2 go to a PCAA connected to the S controller, and PT1 and PT2 go to a PCAA connected to the T controller. It is important to fully seat the cable mounting screws, finger-tight only, into PCAA and TCAT to ensure proper cable grounding. Failure to secure the cables may result in an inability of PCAA to read the electronic ID on TCAT and may reduce the quality of other signals.

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**Note** When removing 68-pin cables, ensure that the hex posts in the board-mounted connectors do not turn when backing out the cable thumbscrews.

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- 4** Plug in one or two Ethernet cables depending on the system configuration. When a single IONet connection is used, the module operates correctly over either port. If dual connections are used, standard practice is to hook ENET1 to the network associated with the R controller. However, the PCAA is not sensitive to Ethernet connections, and negotiates proper operation over either port. If TMR PCAA modules are present, the network connection should match with the connection made to TCAT. For example, the PCAA module with R IONet connection should have cables that go to the TCAT PR1 and PR2 connectors.
- 5** Check grounding of the JGPA shield wire terminals. In most applications, JGPA shield ground terminals are electrically tied to the sheet metal the board is mounted on. The mounting then supplies the ground path for the terminals. In some applications, it is required to define a shield ground that is independent of the mounting sheet metal. For these applications, the JGPA is mounted using hardware that isolates the board from the sheet metal. In these applications, it is important to provide a suitable ground wire between one or more JGPA terminals and the required shield ground potential.
- 6** Apply power to the module through the P5 connector and check the power and Ethernet status indicator lights.
- 7** Configure the PCAA module as necessary.

## Wiring

The PCAA module features 120 pluggable Euro-style box terminals. A JGPA board mounts adjacent to the PCAA module and uses Euro-style box terminals to provide forty eight shield termination points (green) plus twelve 24 V dc output terminals (orange) for 4-20 mA transmitters. The Euro-style box terminals on TCAT accept conductors with the following characteristics:

| Conductor Type                                                                    | Minimum              | Maximum             |
|-----------------------------------------------------------------------------------|----------------------|---------------------|
| Conductor cross section solid                                                     | 0.2 mm <sup>2</sup>  | NA                  |
| Conductor cross section solid                                                     | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded                                                  | 0.2 mm <sup>2</sup>  | NA                  |
| Conductor cross section stranded                                                  | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded, with ferrule without plastic sleeve             | 0.25 mm <sup>2</sup> | NA                  |
| Conductor cross section stranded, with ferrule without plastic sleeve             | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded, with ferrule with plastic sleeve                | 0.25 mm <sup>2</sup> | NA                  |
| Conductor cross section stranded, with ferrule with plastic sleeve                | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section AWG/kcmil                                                 | 24 AWG               | NA                  |
| Conductor cross section AWG/kcmil                                                 | NA                   | 12 AWG              |
| 2 conductors with same cross section, solid                                       | 0.2 mm <sup>2</sup>  | NA                  |
| 2 conductors with same cross section, solid                                       | NA                   | 1 mm <sup>2</sup>   |
| 2 conductors with same cross section, stranded                                    | 0.2 mm <sup>2</sup>  | NA                  |
| 2 conductors with same cross section, stranded                                    | NA                   | 1.5 mm <sup>2</sup> |
| 2 conductors with same cross section, stranded, ferrules without plastic sleeve   | 0.25 mm <sup>2</sup> | NA                  |
| 2 conductors with same cross section, stranded, ferrules without plastic sleeve   | NA                   | 1 mm <sup>2</sup>   |
| 2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve | 0.5 mm <sup>2</sup>  | NA                  |
| 2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve | NA                   | 1.5 mm <sup>2</sup> |

The following table lists the terminal assignments for the PCAA module.

**TCAS Screw Terminal Assignments**

|    | <b>Name</b> | <b>Function</b> |    | <b>Name</b> | <b>Function</b>          |
|----|-------------|-----------------|----|-------------|--------------------------|
| 1  | TC1H        | Thermocouple1   | 41 | TC21H       | Thermocouple21           |
| 2  | TC1L        |                 | 42 | TC21L       |                          |
| 3  | TC2H        | Thermocouple2   | 43 | TC22H       | Thermocouple22           |
| 4  | TC2L        |                 | 44 | TC22L       |                          |
| 5  | TC3H        | Thermocouple3   | 45 | TC23H       | Thermocouple23           |
| 6  | TC3L        |                 | 46 | TC23L       |                          |
| 7  | TC4H        | Thermocouple4   | 47 | TC24H       | Thermocouple24           |
| 8  | TC4L        |                 | 48 | TC24L       |                          |
| 9  | TC5H        | Thermocouple5   | 49 | TC25H       | Thermocouple25           |
| 10 | TC5L        |                 | 50 | TC25L       |                          |
| 11 | TC6H        | Thermocouple6   | 51 | TFH1        | TTLpulserate input #1    |
| 12 | TC6L        |                 | 52 | TFL1        |                          |
| 13 | TC7H        | Thermocouple7   | 53 | TFPWR1      |                          |
| 14 | TC7L        |                 | 54 | TFL1        |                          |
| 15 | TC8H        | Thermocouple8   | 55 | TFH2        | TTLpulserate input #2    |
| 16 | TC8L        |                 | 56 | TFL2        |                          |
| 17 | TC9H        | Thermocouple9   | 57 | TFPWR2      |                          |
| 18 | TC9L        |                 | 58 | TFL2        |                          |
| 19 | TC10H       | Thermocouple10  | 59 | ASIH1       | Analog 4-20 mA input #1  |
| 20 | TC10L       |                 | 60 | ASIL1       |                          |
| 21 | TC11H       | Thermocouple11  | 61 | ASIH2       | Analog 4-20 mA input #2  |
| 22 | TC11L       |                 | 62 | ASIL2       |                          |
| 23 | TC12H       | Thermocouple12  | 63 | ASIH3       | Analog 4-20 mA input #3  |
| 24 | TC12L       |                 | 64 | ASIL3       |                          |
| 25 | TC13H       | Thermocouple13  | 65 | ASIH4       | Analog 4-20 mA input #4  |
| 26 | TC13L       |                 | 66 | ASIL4       |                          |
| 27 | TC14H       | Thermocouple14  | 67 | ASIH5       | Analog 4-20 mA input #5  |
| 28 | TC14L       |                 | 68 | ASIL5       |                          |
| 29 | TC15H       | Thermocouple15  | 69 | ASIH6       | Analog 4-20 mA input #6  |
| 30 | TC15L       |                 | 70 | ASIL6       |                          |
| 31 | TC16H       | Thermocouple16  | 71 | APWRP12     | ±12 V power output       |
| 32 | TC16L       |                 | 72 | APWRN12     |                          |
| 33 | TC17H       | Thermocouple17  | 73 | ASIH7       | Analog 4-20 mA input #7  |
| 34 | TC17L       |                 | 74 | ASIL7       |                          |
| 35 | TC18H       | Thermocouple18  | 75 | ASIH8       | Analog 4-20 mA input #8  |
| 36 | TC18L       |                 | 76 | ASIL8       |                          |
| 37 | TC19H       | Thermocouple19  | 77 | ASIH9       | Analog 4-20 mA input #9  |
| 38 | TC19L       |                 | 78 | ASIL9       |                          |
| 39 | TC20H       | Thermocouple20  | 79 | ASIH10      | Analog 4-20 mA input #10 |
| 40 | TC20L       |                 | 80 | ASIL10      |                          |

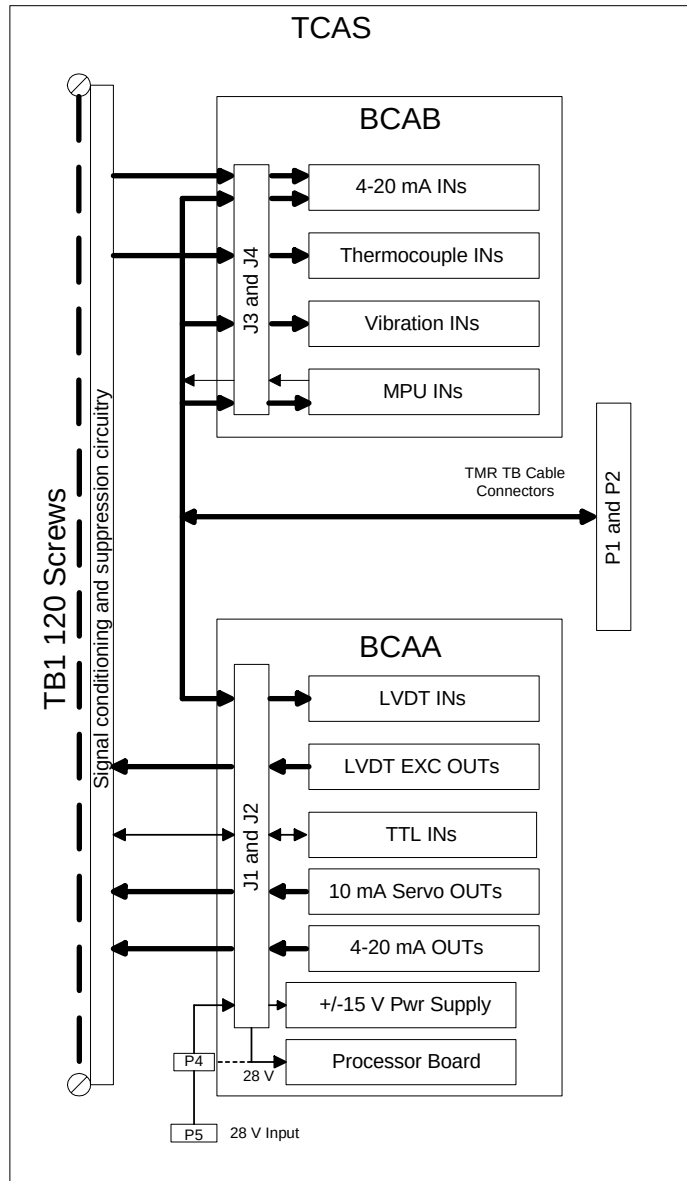


|     | Name   | Function                                                    |     | Name     | Function                                                    |
|-----|--------|-------------------------------------------------------------|-----|----------|-------------------------------------------------------------|
| 81  | ASIH11 | Analog 4-20 mA $\pm$ 10 V input #11                         | 101 | SVO5L    | Servo Output #5 & #6.<br>Note Odd-Even Terminal<br>Grouping |
| 82  | ASIL11 |                                                             | 102 | SVO6L    |                                                             |
| 83  | ASIH12 | Analog 4-20 mA $\pm$ 10 V input #12                         | 103 | SVO5H    |                                                             |
| 84  | ASIL12 |                                                             | 104 | SVO6H    |                                                             |
| 85  | ASOH1  | Analog 4-20 mA Output #1                                    | 105 | SVO5X    |                                                             |
| 86  | ASOL1  |                                                             | 106 | SVO6X    |                                                             |
| 87  | ASOH2  | Analog 4-20 mA Output #2                                    | 107 | SVRL1    | Servo Suicide Relay Input                                   |
| 88  | ASOL2  |                                                             | 108 | SVRL2    |                                                             |
| 89  | SVO1L  | Servo Output #1 & #2.<br>Note Odd-Even Terminal<br>Grouping | 109 | LVDTEXH1 | LVDT Excitation Output #1                                   |
| 90  | SVO2L  |                                                             | 110 | LVDTEXL1 |                                                             |
| 91  | SVO1H  |                                                             | 111 | LVDTEXH2 | LVDT Excitation Output #2                                   |
| 92  | SVO2H  |                                                             | 112 | LVDTEXL2 |                                                             |
| 93  | SVO1X  |                                                             | 113 | LVDTEXH3 | LVDT Excitation Output #3                                   |
| 94  | SVO2X  |                                                             | 114 | LVDTEXL3 |                                                             |
| 95  | SVO3L  | Servo Output #3 & #4.<br>Note Odd-Even Terminal<br>Grouping | 115 | LVDTEXH4 | LVDT Excitation Output #4                                   |
| 96  | SVO4L  |                                                             | 116 | LVDTEXL4 |                                                             |
| 97  | SVO3H  |                                                             | 117 | LVDTEXH5 | LVDT Excitation Output #5                                   |
| 98  | SVO4H  |                                                             | 118 | LVDTEXL5 |                                                             |
| 99  | SVO3X  |                                                             | 119 | LVDTEXH6 | LVDT Excitation Output #6                                   |
| 100 | SVO4X  |                                                             | 120 | LVDTEXL6 |                                                             |

## Operation

### Module Overview

The PCAA module consists of four separate circuit boards in a single physical assembly. The module is regarded as the least replaceable unit because of the difficulty of isolating a failure to a single board. The module is not designed for replacement of individual boards.



*PCAA Board Relationship Diagram*

### TCAS Terminal Board

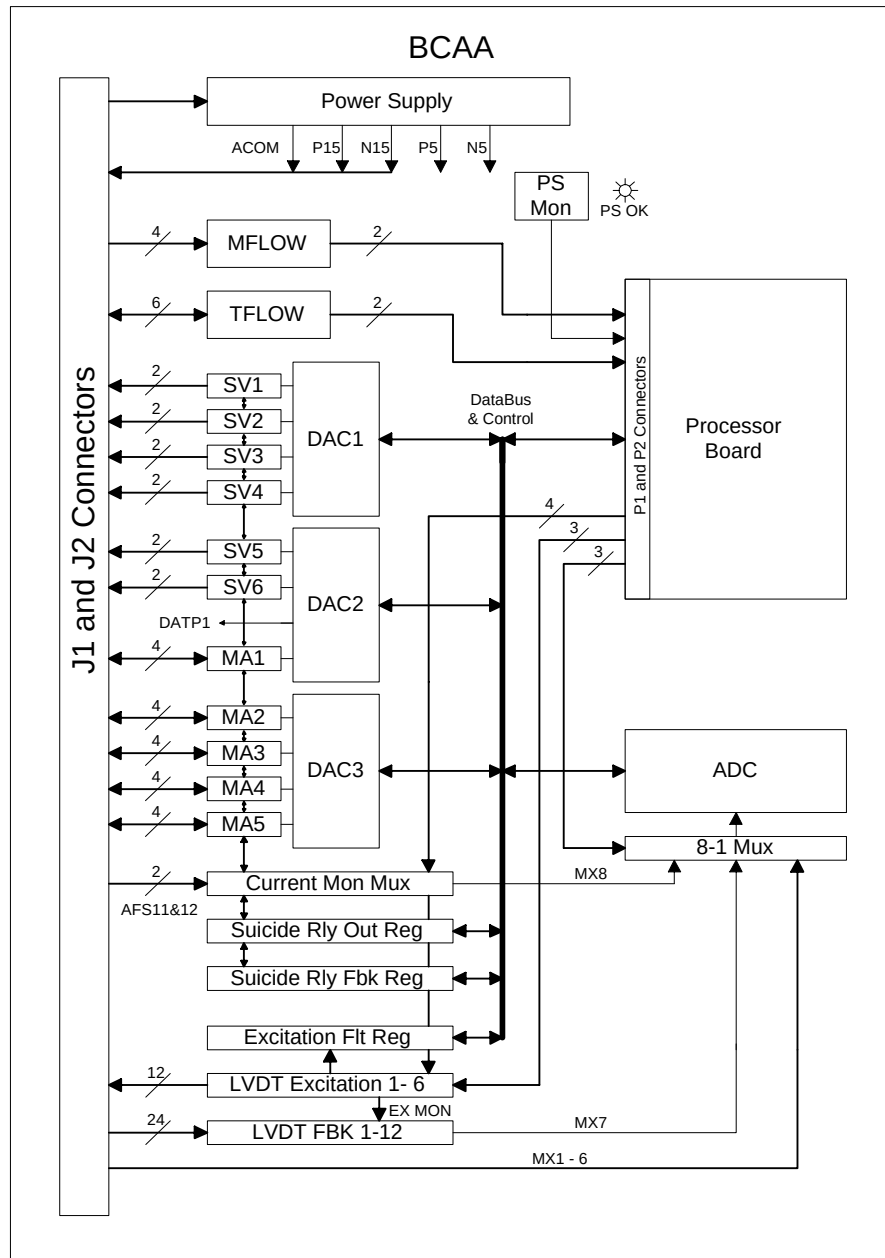
The IS200TCAS terminal board provides the customer terminals and signal routing into the BCAA and BCAB boards. TCAS accepts bulk 28 V control power through the P5 connector. It then provides the power through connector P4 to a JGPA board in the input cable shield termination location. TCAS provides the P1 and P2 68 pin connectors for IS200TCAT terminal board cables. Internal to the module the TCAS terminal board routes signals to connectors for the BCAA and BCAB analog processing boards.

## BCAA and BCAB Analog Processing Boards

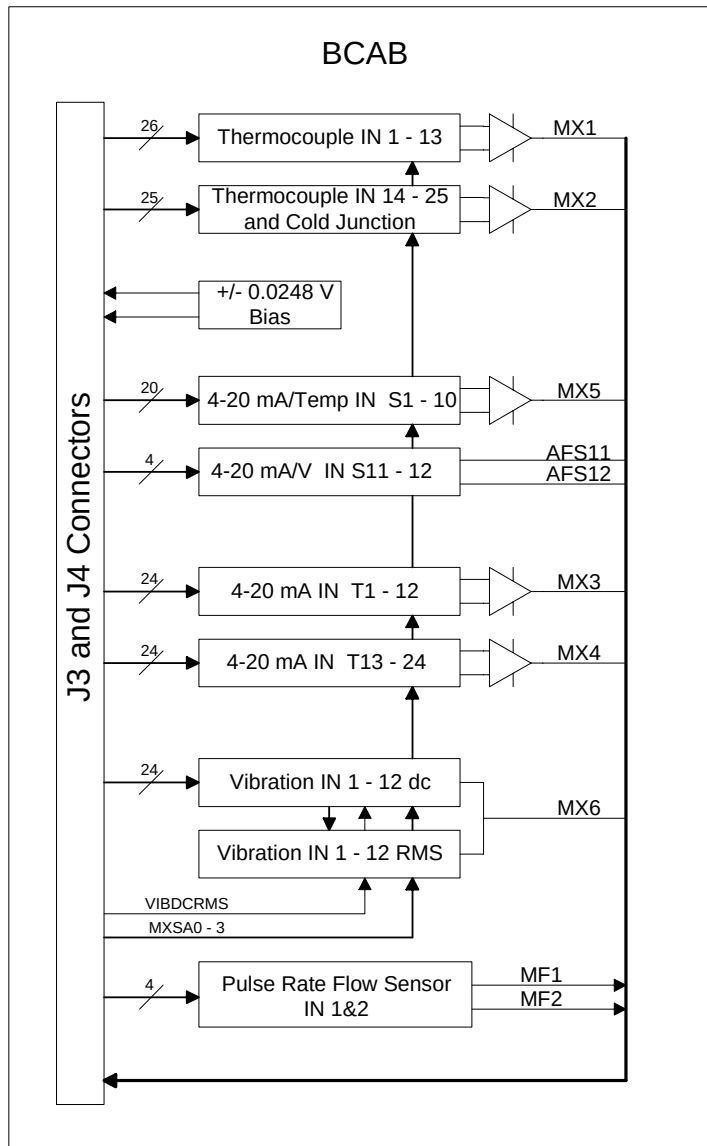
Inside the module cover the BCAA and BCAB boards provide power, analog signal conditioning, and analog/digital conversion.

BCAA is the main printed circuit board in the PCAA module. This board provides the main  $\pm 15$  V power and the majority of the digital and analog interface to the processor board. In addition, this board provides the signal conditioning required to interface 12 LVDT sensors, five 4-20mA and six servo outputs, and two TTL flow sensors to the processor board.

The BCAB interface board provides the signal conditioning required to interface the thermocouples, 4-20 mA inputs, pulse rate flow sensors and vibration inputs to the control electronics.



BCAA Block Diagram



*BCAB Block Diagram*

### **Processor**

The processor board in the module is common to all Mark VIe I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Local ambient temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network does not result in any disturbance to the I/O pack operation, and the failure is indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

### ***ID Line***

The four boards that make up the PCAA module contain electronic ID parts that are read during power initialization. A similar part associated with each cable connection on the TCAT terminal board allows the processor to confirm correct matching of all board revisions plus processor firmware and report board revision status to the system level control.

### ***Power Management***

The PCAA includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a power disturbance in the module from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows module status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the module.
- LED solid on - a critical fault is present that prevents the module from operating. Critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - a diagnostic alarm condition is present in the module such as incorrect TCAT terminal board cables or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the module is not online
- LED flashing slowly (2 cycle) - the module has received a request to flash the LED to draw attention to the module. This is used during factory test or as an aid to confirm physical location against ToolboxST\* settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the module is transmitting or receiving data over the port.

## Connectors

- Connectors P1 and P2 provide cable connections to a TCAT terminal board.
- An RJ45 Ethernet connector named ENET1 on the module side is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the module side is the redundant or secondary system interface.
- A 3-pin power connector P5 on the module is the input point for 28 V dc power for the module and terminal boards.
- A power connector P4 on the module provides 28 V dc power to a JGPA board located for wire shield termination.

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**Note** The module operates from a power source that is applied directly to the module P5 connector, not through the normal power connector located on the processor board.

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## Signal Response

The PCAA module is designed to run at frame rates of 40 and 10 ms. For each signal type an accuracy specification is listed that includes all effects such as aging, temperature, power supply input variation, and product variation. For each signal type a typical accuracy at 25°C with mean and standard deviation is also listed. This typical accuracy is similar to the accuracy that can be expected in normal operation while the specified accuracy is an absolute worst case limit on the signal accuracy.

## Thermocouples

PCAA supports the following thermocouple types and temperature ranges:

| Type | Range °F     | Range °C       |
|------|--------------|----------------|
| E    | -60 to +1150 | -51 to +621    |
| J    | -60 to +1500 | -51 to +816    |
| K    | -60 to +2000 | -51 to +1093   |
| T    | -60 to +750  | -51 to +399    |
| S    | 0 to 3200    | -17.78 to 1760 |

A single cold junction is provided with each PCAA module. The module accepts a controller backup cold junction value, CJBackup, in the event a problem is detected with the local sensor. The PCAA may be configured to use a controller provided remote cold junction value, CJRemote. All thermocouple inputs are biased with a dc voltage that will drive the temperature signal full scale negative in the event of an open wire. Accuracy exceeds  $\pm 0.1\%$  of full scale over the full specified operating temperature of PCAA. Typical measured mean accuracy at 25°C is  $\pm 0.01\%$  with a standard deviation of 0.016%. Primary source of temperature drift for thermocouple inputs is a precision calibration reference rated at 0.0008%/°C worst case.

### 4-20 mA Inputs

PCAA meets the specification of  $\pm 0.25\%$  for 4-20 mA inputs,  $\pm 0.5\%$  for voltage inputs over the full PCAA operating temperature range. Typical measured mean current input accuracy at 25°C is  $\pm 0.05\%$  with a standard deviation of 0.016%. Primary source of temperature drift for analog inputs is a precision calibration reference rated at 0.0008%/°C worst case. All inputs have a jumper to select grounded or floating measurements. When the Open/GND jumper is in the Open position the input accepts a maximum of 7 volts common mode relative to the PCAA ground. As a group it is possible to specify an upper and lower current level for a valid input. Each input may then be individually configured to produce a diagnostic when current is outside the specified limits.

Analog inputs 11 and 12 may also be configured as voltage inputs. In support of sensors on legacy systems a single  $\pm 12$  V power supply output is provided on PCAA with rating of 50 mA.

### 4-20 mA

Typical measured mean accuracy at 25°C is  $\pm 0.1\%$  with standard deviation of 0.11%. The two outputs on PCAA behave as typical simplex analog outputs. The three outputs on TCAT, when driven from triple PCAA modules, exhibit full fault tolerance. An output failure on one of the three PCAA modules results in a very short disturbance to the output with full recovery to the commanded value. All five analog outputs are provided with independent read-back of the output current and an output relay. If incorrect operation of the output is detected, the relay is automatically opened to protect the connected device against excessive output current. All analog output circuits have greater than 18 V output drive capability.

## Seismic Inputs

TCAT seismic inputs are biased with a small dc current for open wire detection. Inputs go through a high-pass filter at 4 Hz and low pass filter at 600 Hz. The filtered signal goes through an RMS conversion followed by a 1 Hz filter. The result is sampled and used to perform a calculation to determine inches per second peak vibration. In parallel with the primary signal path, the inputs are monitored for the presence of dc voltage to drive the annunciation of a failed or open sensor. PCAA meets accuracy of  $\pm 2\%$  over the full PCAA operating temperature range. Typical measured mean seismic input accuracy at 25°C is  $\pm 0.02\%$  with standard deviation of 0.25%.

## LVDT

Each of six excitation outputs provides a 7 Vrms, 3.2 kHz sine wave and is capable of driving 60 mA. Input sampling takes place at 100 Hz. PCAA meets LVDT input voltage accuracy of  $\pm 1\%$  over the full range of operating temperature and load impedances. Typical measured mean accuracy at 25°C is  $\pm 0.07\%$  with standard deviation of 0.05%. Position feedback accuracy in the PCAA is dominated by initial calibration quality and any drift experienced in the circuits after calibration. In PCAA, drift is determined by the precision voltage reference used for internal circuit calibration, rated for 0.0008%/°C worst case temperature drift and almost no measurable aging.

## Servos

### Servos

Servo output features in the PCAA Module :

#### PCAA

Six output drivers capable of full scale output of 10 mA.

Regulators run at 100 Hz

Servo output accuracy  $\pm 3.5\%$

Two of six outputs controlled by optional input signal that removes output drivers and biases output closed

PCAA regulator types supported include the following.

#### PCAA

| Reg Type   | Description                                                                                                                                                   |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Position   | Set RegGain = 0 and adjust the current regulator command, ServoCurrentRef through the system output, Reg#_NullCor.                                            |
| LiquidFuel | FlowInput1 = FlowRate1-4 FlowInput2 = Unused                                                                                                                  |
| LiquidFuel | FlowInput1 = FlowRate1-4 and FlowInput2 = FlowRate1-4.<br>Input is the maximum of the two values.                                                             |
| Position   | PositionInput1 = Position 1 selected from LVDT1 through LVDT12 and PositionInput2 = Unused and PositionInput3 = Unused.<br>Not supported                      |
| Position   | PositionInput1 = Position 1 selected from LVDT1 through LVDT12 and PositionInput2 = Position 2 selected from LVDT1 through LVDT12 and PositionInput3 = Unused |



## PCAA

| Reg Type                | Description                                                                                                                                                                                           |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Position                | PositionInput1 = Position 1 selected from LVDT1 through LVDT12 and PositionInput2 = Position 2 selected from LVDT1 through LVDT12 and PositionInput3 = Position 3 selected from LVDT1 through LVDT12. |
| SpeedRatio              | Outer P2 pressure loop regulating the maximum of two P2 pressure feedbacks feeding the reference to the inner position loop deriving its feedback from the maximum of two LVDTs.                      |
| LiquidFuel<br>wPosition | Outer flow rate loop regulating the maximum of two flow rate feedbacks providing the reference to the inner position loop deriving its feedback from the maximum of two LVDTs.                        |

PCAA implements four regulator types. The Speed Ratio Valve (SRV) regulator in the PCAA is an enhanced version of the SRV control in the Mark VI product. The PCAA provides support for both the outer P2 pressure loop and the inner position loop. The PCAA can run both loops at 100 Hz compared to 200 Hz for the PSVO's inner position loop and 25 Hz for the controller's outer P2 loop.

Output current range is fixed at 10 mA. PCAA meets a servo output accuracy of  $\pm 3.5\%$  of full scale over the full range of operating temperature and load impedance. Typical measured mean accuracy at 25°C is  $\pm 0.5\%$  with standard deviation of 0.07%.

To allow continuous movement of the servo system to avoid sticking, PCAA features adjustable amplitude dither with frequency selected to be 50 Hz, 25 Hz, 16.67 Hz, 12.5 Hz, and 8.13 Hz.

The first two servo outputs are equipped with an output shut down relay. Terminals 107 and 108 must be disconnected for servo 1 and 2 to be enabled. If terminals 107 and 108 are shorted together, the servo driver is disconnected from the output terminals and a passive circuit biases the servo closed. This feature is used when it is required to include servo action in a control protective response. The TREG K4CL relay is often used for this purpose in simplex systems. If protective action is not needed on these servos, a wire jumper should be provided between terminals 107 and 108. Servos three through six are not affected by the shut down relay action.

LVDT signal conditioning on the PCAA uses the measured value of excitation voltage to correct for excitation changes. One PCAA module may be providing excitation on an LVDT that is being read by all three PCAA modules in a TMR set. Application blockware must be provided to pass the excitation voltage monitor inputs, ServoExcitMonitor\_R, ServoExcitMonitor\_S, ServoExcitMonitor\_T to the ExcMon\_fromR and ExcMon\_fromS outputs through the Move block function.

## Position Valve Servo System

The Position Valve Servo system is used to control the Gas Control Valves (GCV) on the fuel skids of heavy-duty gas turbines and the Inlet Guide Vanes (IGV) on the compressor of the heavy-duties. Refer to the diagram *Position Valve Servo System*.

GCV or guide vane position is fed back to the digital position regulator in the PCAA using LVDT sensors. The TCAS terminal board provides the six LVDT excitation signal pairs: LVDTEXH1\_R/LVDTEXL1\_R through LVDTEXH6\_R/LVDTEXL6\_R. These excitation outputs are connected to the primary-side of the LVDT position sensor. The primary-side signal is a 3.2 kHz sine wave excitation with a 7.07 V RMS amplitude. The LVDT secondary-side signal amplitude is proportional to the position change in the valve. The LVDT secondary-side is connected to one of the twelve TCAT terminal board LVDT input signal pairs: LVDT1H/LVDT1L through LVDT12H/LVDT12L. The TCAT terminal board is used to fan the LVDT signal pair to the TMR PCAA set: PCAA (R), PCAA (S) and PCAA (T) through cabling. The BCAA acquisition board provides signal conditioning to convert the RMS voltage from the secondary-side of the LVDT to a dc equivalent signal read by the processor through analog-to-digital (A/D) converters.

The PCAA firmware can run up to six independent digital servo regulators. Each loop is performed at a 100 Hz sample rate. Details of the Position digital regulator are covered in the next section. The digital regulator output, ServoCurrentRef is written to a digital-to-analog (D/A) converter. The negated output of the D/A is the current command for the analog current regulator.

The BCAA acquisition board has six analog current regulators, one per digital servo regulator. All six analog current regulators are rated for 10 mA only. Each current output provides an internal suicide protection relay controlled by the PCAA firmware. Each of the six servo outputs supports either three-coil servos or two-coil servos and each provides a jumper on the TCAS terminal board to configure the output.

The jumper is placed in the TMR position for the 3-coil servo and placed in the opposite position for the 2-coil servo. For example, for the 3-coil servo using Servo output 1:

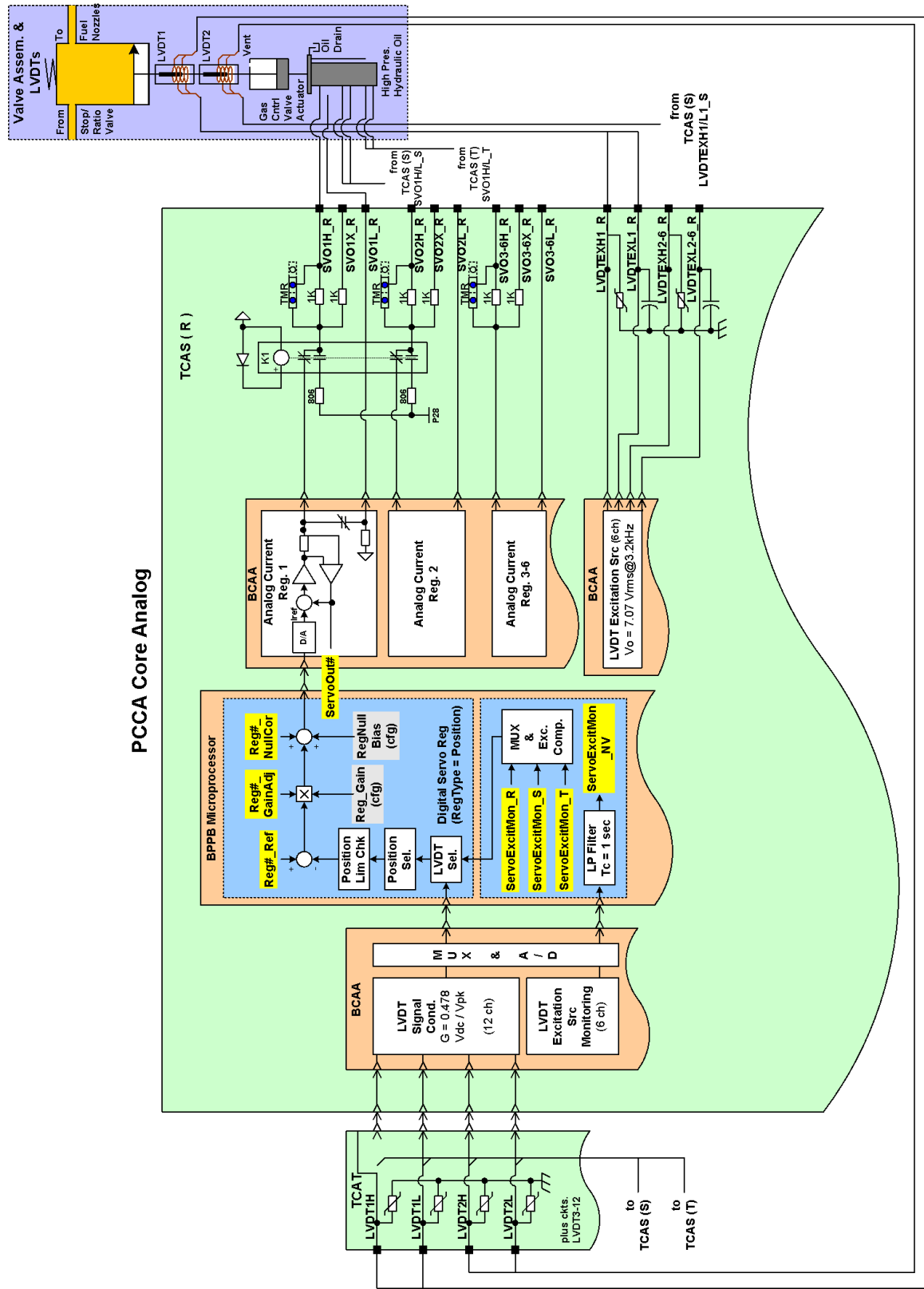
PCAA SVO1H\_R/SVO1L\_R outputs are connected to coil 1, TCAS JP15\_R is placed in 1-2\_TMR

PCAA SVO1H\_R/SVO1L\_R outputs are connected to coil 2, TCAS JP15\_S is placed in 1-2\_TMR

PCAA SVO1H\_R/SVO1L\_R outputs are connected to coil 3, TCAS JP15\_T is placed in 1-2\_TMR

For the simplex 2-coil servo connection, PCAA\_R SV01H/L outputs are connected to coil 1 and SV01X\_R/SVO1L\_R outputs are connected to coil 2. TCAS JP15\_R is placed in 2-3\_Simplex (non-TMR position).

Servo outputs 1 and 2 also provide a means to externally suicide the outputs through the TCAS inputs SVRL1/2. For the Mark VIe, the PPRO provides an external contact connected across SVRL1 and SVRL2. If the contact closes, the K1 relay is energized and the servo output is isolated from the digital regulator control, providing a direct connection through a current limiting resistor (15mA fixed output), as long as the K1 relay is energized.



Position Valve Servo System

## Digital Servo Regulator\_Position

The digital Position regulator is a proportional regulator generating a servo current command proportional to the error signal, the difference between the position reference from the controller and the valve position feedback. Refer to the diagram *Digital Servo Regulator\_Position*.

Three feedback options are supported: Single position feedback, dual position feedbacks or three position feedbacks.

- Setting *PositionInput1* equal to one of the twelve LVDT inputs can configure the single position feedback option.
- The dual feedback option is selected when the configuration parameters, *PositionInput1* and *PositionInput2* are assigned to different LVDT inputs.
- The three feedback option is enabled by setting each of the following configuration parameters to a unique LVDT input: *PositionInput1*, *PositionInput2* and *PositionInput3*.

Each of the position inputs enabled run through a Position Calculation function that converts the dc volts signal representing RMS volts to a valve position in percent where 0% represents fully closed and 100% represents a fully open valve.

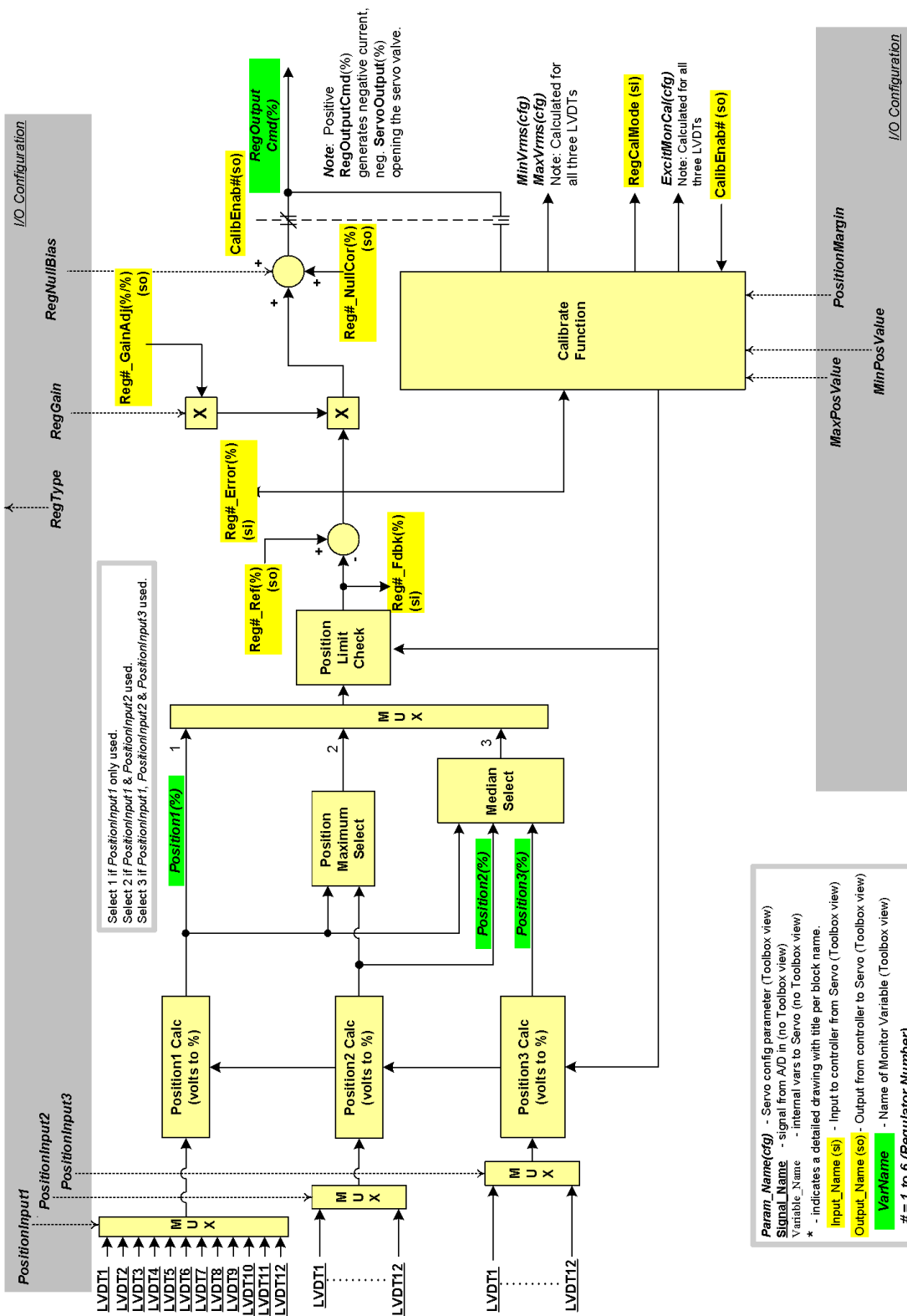
The Position Limit function's input is the following based on the configuration:

- Equal to the Position Calculation output for a single position feedback.
- Equal to the maximum select from two Position Calculation outputs for the dual position input configuration.
- Equal to the median select for the three position input configuration. The Position Limit function checks the feedback range of *Reg#\_Fdbk*. The range defined in percent over nominal is configurable using the parameter, *Fdbk\_Suicide*. The suicide only works if it is enabled by *EnabPosFbkSuic*.

In the next figure, the proportional regulator error, is equal to the position reference command from the controller, *Reg#Ref* minus the position feedback, *Reg#\_Fdbk*. Proportional regulator error is multiplied by a composite gain defined by the multiplication of the configuration parameter, *RegGain* and the controller output, *Reg#\_GainAdj*. The product of the gain and position error defines a current in percent. The amount of current required to negate the spring force used to close the valve if the servo fails is compensated by the configuration parameter, *RegNullBias*. The controller system output, *Reg#\_NullCor* is used to correct the null bias value when one of the TMR servos is suicided. The resultant output from the proportional position regulator is a current command in percent with the Monitor variable name, *ServoCurrentRef*.

After the initial configuration setting is made for the position loop, the user calibrates the position valve feedbacks. This is done by using ToolboxST to select the LVDT calibration mode and setting the controller output *CalibEnab#* equal to TRUE. In the calibration mode, the user can use the servo output in the open-loop mode to force the valve to the fully closed position and also to the fully open position. During the calibration mode, the PCAA assigns the RMS voltage that represents the open and closed position to the configuration parameters for each LVDT that is used: *MinVrms* and *MaxVrms*. The user selects *Calibrate and Save* to store the LVDT Excitation output voltage is read and stored in the LVDT configurable parameter *ExcitMonCal*. The excitation voltage is used to compensate for excitation voltage changes during runtime. The user must also verify that the LVDT parameter *ExcitSelect* comes from the proper Excitation voltage source (R,S, or T).

### Digital Servo Regulator - Position



### Digital Servo Regulator - Position

## Speed Ratio Valve Servo System

The Speed Ratio Valve Servo system is used to control the main fuel-feed Speed Ratio Valve (SRV) whose output feeds the GCVs on the fuel skids of the heavy-duty gas turbines. The SRV control is a multi-loop servo. The P2 pressure provides the outer loop feedback and the valve position provides the inner loop control. Refer to the diagram *Speed Ratio Valve Servo System*.

The outer loop SRV pressure is fed back to the digital pressure loop in the PCAA using pressure sensors. These pressure sensors have 4-20 mA outputs that are connected to one of the TCAS terminal board dedicated SRV analog inputs: ASIH11\_R / ASIL11\_R and/or ASIH12\_R / ASIL12\_R.

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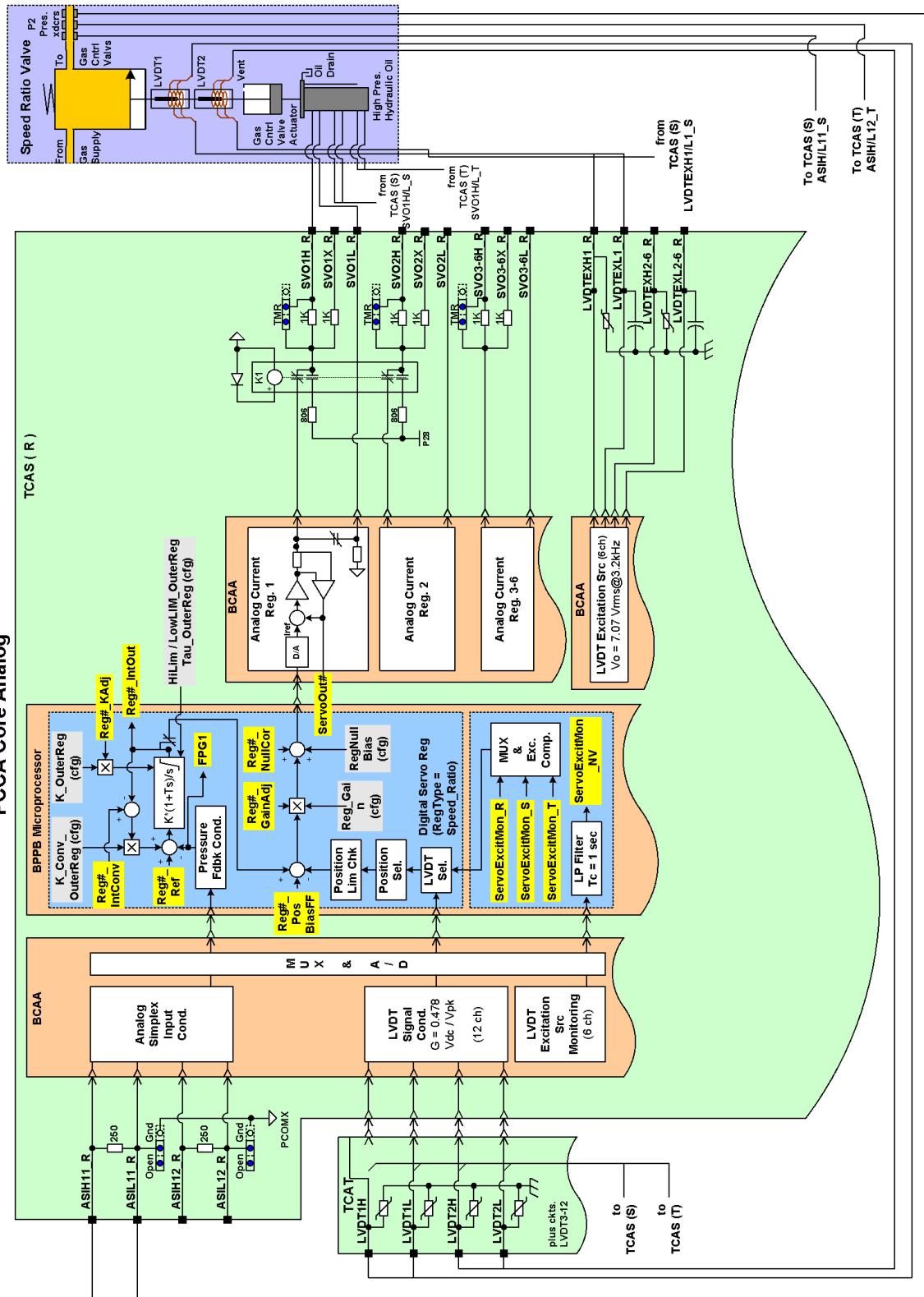
**Note** The pressure inputs are not fanned, and redundant pressure inputs are connected to separate PCAA modules when the SRV is configured as TMR.

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The inner loop P2 valve position is fed back to the digital position loop in the PCAA using LVDT sensors. The LVDT secondary-side is connected to one of the twelve TCAT terminal board LVDT input signal pairs: LVDT1H/LVDT1L through LVDT12H/LVDT12L. The TCAT terminal board is used to fan the LVDT signal pair to the TMR PCAA set: PCAA (R), PCAA (S) and PCAA (T) through cabling. The BCAA acquisition board provides signal conditioning to convert the RMS voltage from the secondary-side of the LVDT to a dc equivalent signal read by the processor through analog-to-digital (A/D) converters.

The PCAA firmware uses one of the six independent digital servo regulators. The SRV loop is run at a 100 Hz sample rate. Details of the Speed Ratio Valve digital regulator are covered in the next section. The digital regulator output, ServoCurrentRef is written to a digital-to-analog (D/A) converter. The output of the D/A is the current command for the analog current regulator.

# PCAA Core Analog



Speed Ratio Valve Servo System

## Digital Servo Regulator – Speed Ratio

The digital Speed Ratio Valve regulator is a proportional plus integral (PI) outer regulator with an inner proportional position regulator generating a servo current command. The SRV output is based on a multi-loop control using the P2 pressure feedback for the outer loop and the valve position for the inner loop feedback. Refer to the diagram *Digital Servo Regulator - Speed Ratio*.

The outer P2 pressure loop derives its pressure feedback from either a single pressure input or the maximum select of two pressure inputs. For a single pressure input, the configuration parameter *PressureInput1* is assigned to either AnalogInput11 or 12. For a dual pressure input, *PressureInput1* is assigned to AnalogInput11 or 12 and *PressureInput2* is assigned to AnalogInput11 or 12. The Pressure Limit Check checks the range of the maximum select or the single feedback depending on the configuration. If the pressure feedback, Reg#\_Pressure is less than *PresFdbkLoLim* or Reg#\_Pressure is greater than *PresFdbkHiLim* then the pressure loop is assumed to be open loop and the SRV servo out will suicide if the *EnabPressureFbkSuic* parameter is set to Enable.

The SRV pressure error, Reg#Ref minus Reg#Pressure has an integrator convergence error added to it. The objective of the convergence error is to keep the PI controller between PCAA (R), PCAA (S) and PCAA (T) together. The PI output for (R, S and T), Reg#\_IntOut is read by the controller. The average error, Reg#\_IntConv is calculated from the three inputs. Each SRV regulator for R, S and T takes the average, subtracts its own PI output value from this, multiplies it by a gain value, *K\_Conv\_OuterReg* to come up with the convergence error to move the integrator for PI R, S and T together. The PI proportional gain, *K\_OuterReg* and the integral time constant, *Tau\_OuterReg* provide the PI adjustments. The clamping is controlled by the parameters: *HiLim\_OuterReg* and *LowLim\_OuterReg*. The PI outer loop output, Reg#\_IntOut is the position command for the inner position loop.

The inner position loop supports two feedback options: Single position feedback and the maximum select of two position feedbacks. Setting PositionInput1 equal to one of the twelve LVDT inputs can configure the single position feedback option. The maximum select of two position feedbacks is selected when the configuration parameters, *PositionInput1* and *PositionInput2* are assigned to different LVDT inputs.

Each of the position inputs enabled run through a Position Calculation function that converts the dc volts signal representing RMS volts to a valve position in percent where 0% represents fully closed and 100% represents a fully open valve.

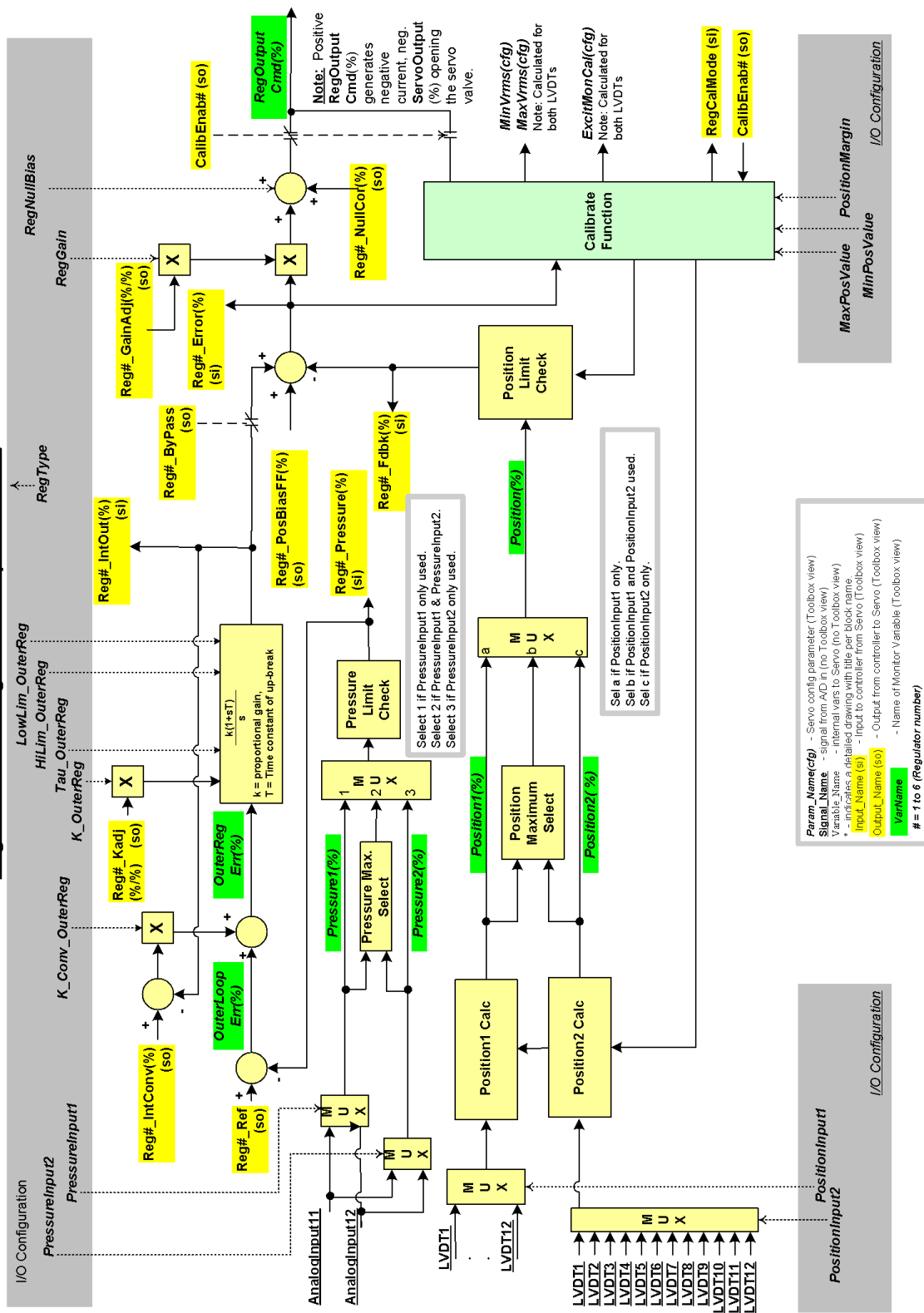
The Position Limit function's input is the following based on the configuration: equal to the Position Calculation output for a single position feedback or equal to the maximum select from two Position Calculation outputs for the dual position input configuration. The Position Limit function checks the feedback range of Reg#\_Fdbk. The range defined in percent over nominal is configurable using the parameter, *Fdbk\_Suicide*.

The proportional regulator error, Reg#\_Error is equal to the position reference command from the controller, Reg#Ref minus the position feedback, Reg#\_Fdbk. Reg#\_Error is multiplied by a composite gain defined by the multiplication of the configuration parameter, RegGain and the controller output, Reg#\_GainAdj. The product of the gain and position error defines a current in percent. The amount of current required to negate the spring force used to close the valve if the servo fails is compensated by the configuration parameter, RegNullBias. The controller system output, Reg#\_NullCor is used to correct the null bias value when one of the TMR servos suicides for some reason. The resultant output from the proportional position regulator is a current command in percent with the Monitor variable name, ServoCurrentRef.



After the initial configuration setting is made for the position loop, the user calibrates the position valve feedbacks. This is done by using ToolboxST to select the LVDT calibration mode and setting the controller output *CalibEnab#* equal to TRUE. In the calibration mode, the user can use the servo output in the open-loop mode to force the valve to the fully closed position and also to the fully open position. During the calibration mode, the PCAA assigns the RMS voltage that represents the open and closed position to the configuration parameters: *MinVrms* and *MaxVrms*. The user selects *Calibrate and Save* to store the LVDT Excitation output voltage in the LVDT configurable parameter *ExcitMonCal*. The excitation voltage is used to compensate for excitation voltage changes during runtime. The user must also verify that the LVDT parameter *ExcitSelect* comes from the proper Excitation voltage source (R, S or T).

## Digital Servo Regulator - Speed Ratio



Digital Servo Regulator - Speed Ratio

## Liquid Fuel Valve Servo System

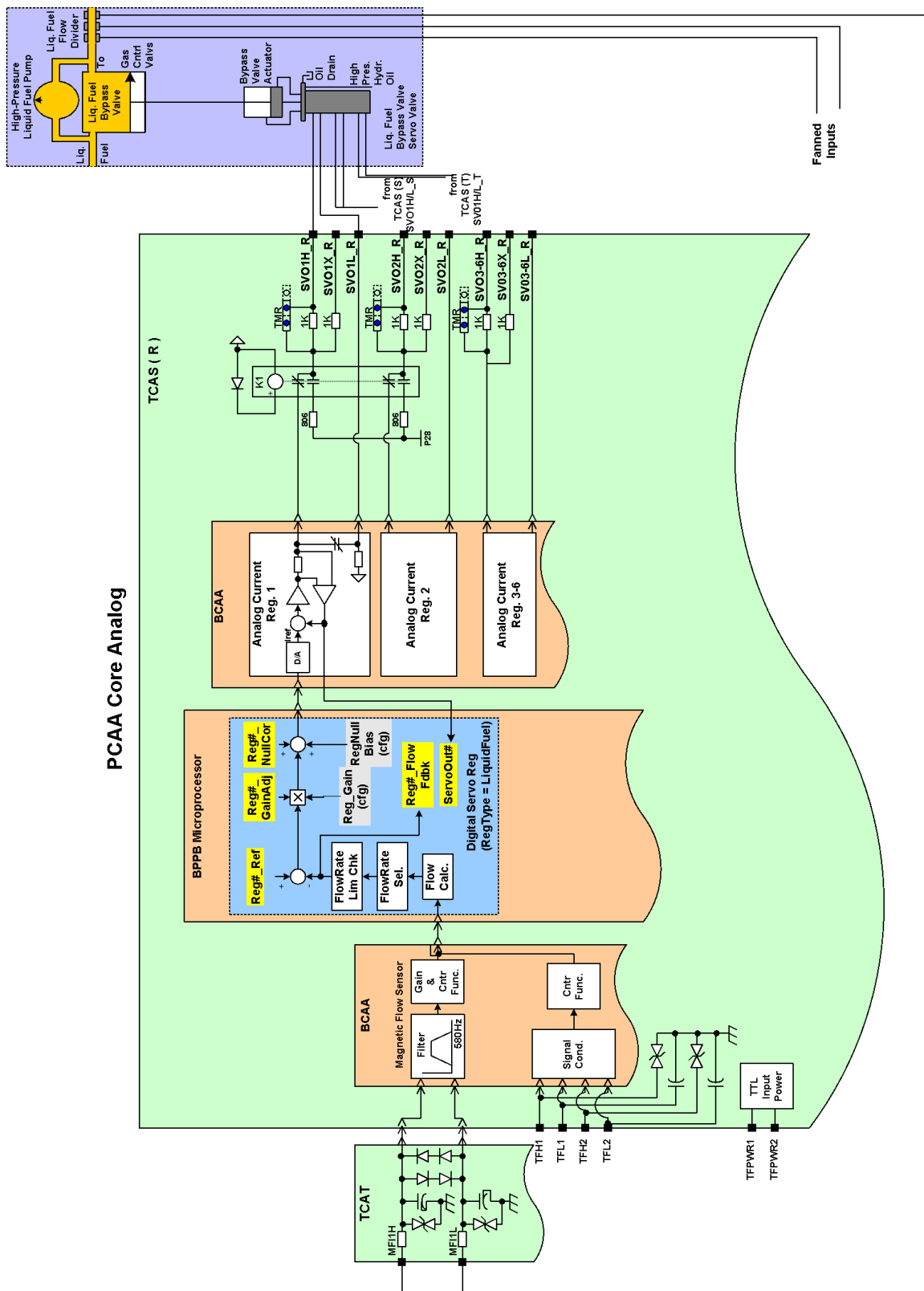
The Liquid Fuel Servo system is used with gas turbines using the liquid fuel option. Refer to the diagram *Liquid Fuel Valve Servo System*.

The flow rate is fed back to the digital flow rate regulator in the PCAA using Liquid Fuel flow meter with magnetic pickup outputs. The flow meter output is connected to one of the two TCAT terminal board magnetic flow sensor input signal pairs: MFI1H/MFI1L through MFI2H/MFI2L or two TCAS terminal board TTL flow sensor input signals: TFH1/L1 through TFH2/L2. The TCAT terminal board is used to fan the magnetic input signal pair to the TMR PCAA set: PCAA (R), PCAA (S) and PCAA (T) through cabling. The BCAA acquisition card provides signal conditioning to convert the variable frequency, variable amplitude input to a digital pulse. The digital pulse from the magnetic flow sensor signal conditioning or the TTL sensor conditioning feeds a counter used to determine the frequency of the pulse train from the flow meter.

The processor board uses one of the six independent digital servo regulators. The Liquid Fuel servo regulator is sampled at a 100 Hz rate. Details of the Liquid Fuel digital regulator are covered in the next section. The digital regulator output, ServoCurrentRef is written to a digital-to-analog (D/A) converter. The output of the D/A is the current command for the analog current regulator.

The BCAA acquisition board has six analog current regulators, one per digital servo regulator. All six analog current regulators are rated for 10 mA only. Each current output provides an internal suicide protection relay controlled by the processor board software. Each of the six servo outputs supports either three-coil servos or two-coil servos and each provides a jumper on the TCAS terminal board to configure the output. The jumper is placed in the *TMR* position for the 3-coil servo and placed in the *Open* position for the 2-coil servo. For the 3-coil servo using Servo output 1, PCAA SVO1H\_R/SVO1L\_R outputs are connected to coil 1, PCAA (S) SV01H/L outputs are connected to coil 2 and PCAA (T) SV01H/L outputs are connected to coil 3. For the simplex 2-coil servo connection, PCAA SVO1H\_R/DVO1L\_R outputs are connected to coil 1 and SV01X/L outputs are connected to coil 2.

Servo outputs 1 and 2 also provide a means to externally suicide the outputs through the TCAS inputs SVRL1/2. For the Mark VIe, the PPRO provides an external contact connected across SVRL1 and SVRL2. If the contact closes, the K1 relay is energized and the servo output is isolated from the digital regulator control, providing a direct connection through a current limiting resistor (15 mA fixed output), as long as the K1 relay is energized.



Liquid Fuel Valve Servo System

## Digital Servo Regulator - Liquid Fuel

The Digital Liquid Fuel regulator is a proportional regulator generating a servo current command proportional to the error signal, the difference between the Liquid Fuel flow rate reference from the controller and the flow rate feedback. Refer to the diagram *Digital Servo Regulator - Liquid Fuel*.

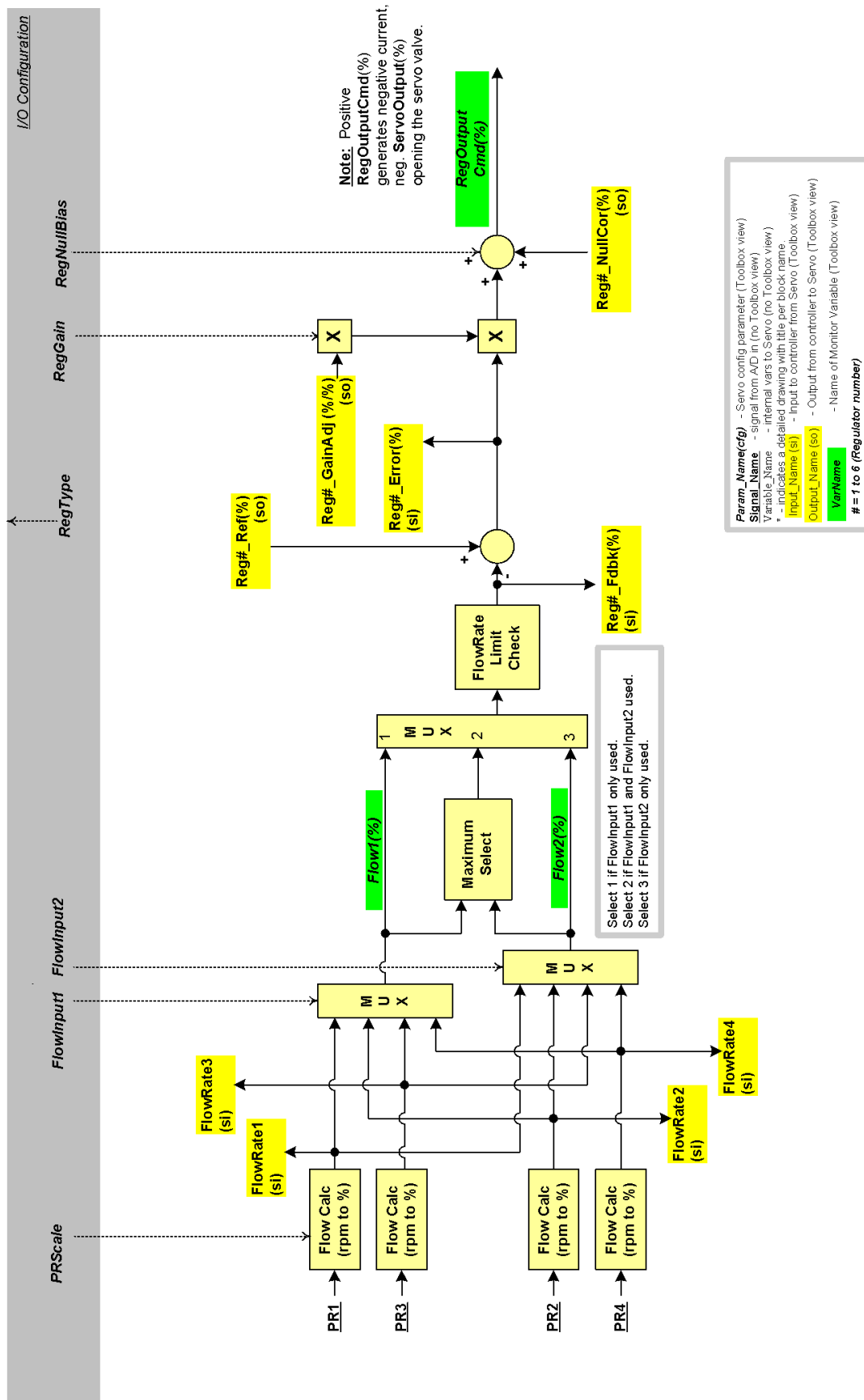
Two flow rate feedback options are supported: Single flow rate feedback or the dual flow rate option. Setting FlowInput1 equal to one of the four flow rate inputs configures the single flow rate option. The dual feedback option is selected when the configuration parameters, *FlowInput1* and *FlowInput2* are assigned to different flow inputs. Unlike the LVDT calibration available for the position inputs, there is no ToolboxST calibration function for the flow inputs.

Each of the enabled flow rate inputs runs through a Flow Rate Calculation function that converts the revolutions per minute frequency to a flow rate percentage where 0% represents no flow and 100% represents a rated flow.

The Flow Rate Limit Check's input is the following based on the configuration: equal to the flow rate output for a single feedback or equal to the maximum select from two flow rates. The Flow Rate Limit Check looks for the flow rate feedback, Reg#\_Fdbk to be out of range. The range is defined using configurable minimum and maximum flow limits in percent of nominal. There is also a configurable delay that must be exceeded before a diagnostic alarm is generated. If the flow feedback exceeds either flow limit for the defined delay the servo will suicide, if enabled.

The proportional regulator error, Reg#\_Error is equal to the flow rate reference command from the controller, Reg#Ref minus the flow rate feedback, Reg#\_Fdbk. Reg#\_Error is multiplied by the composite gain defined by the multiplication of the configuration parameter, *RegGain* and the controller output, Reg#\_GainAdj. The product of the gain and flow rate error defines a current in percent. The amount of current required to negate the spring force used to close the valve if the servo fails is compensated by the configuration parameter, RegNullBias. The controller system output, Reg#\_NullCor is used to correct the null bias value when one of the TMR servos suicides for some reason. The resultant output from the proportional position regulator is a current command in percent with the Monitor variable name, ServoCurrentRef.

## Digital Servo Regulator - LiquidFuel



Digital Servo Regulator - Liquid Fuel

## Liquid Fuel Valve with Position Feedback Servo System

The Liquid Fuel Valve with Position Feedback Servo system is used with gas turbines using the liquid fuel option. The Liquid Fuel Valve with Position Feedback is the multi-loop control system. The fuel flow rate is the feedback for the outer loop and the valve position is the inner loop feedback. Refer to the diagram *Liquid Fuel Valve with Position Feedback Servo System*.

The flow rate is fed back to the digital flow rate regulator in the PCAA using Liquid Fuel flow meter with magnetic pickup outputs. The flow meter output is connected to one of the two TCAT terminal board magnetic flow sensor input signal pairs: MFI1H/MFI1L through MFI2H/MFI2L or one of the PCAA TTL flow sensor input signal pairs. The TCAT terminal board is used to fan the magnetic input signal pair to the TMR PCAA set: PCAA ( R), PCAA (S) and PCAA (T) through cabling. The BCAA acquisition card provides signal conditioning to convert the variable frequency, variable amplitude input to a digital pulse. The digital pulse feeds a counter used to determine the frequency of the pulse train from the flow meter.

The inner loop valve position is fed back to the digital position loop in the PCAA using Linear Variable Differential Transformer (LVDT) sensors. The TCAS terminal board provides the six LVDT excitation signal pairs: LVDTEXH1\_R/LVDTEXL1\_R through LVDTEXH6\_R/LVDL6\_R. The primary-side signal is a 3.2 kHz sine wave excitation with a 7.07 V RMS amplitude. The LVDT secondary-side is connected to one of the twelve TCAT terminal board LVDT input signal pairs: LVDT1H/LSVT1L through LVDT12H/LVDT12L. The TCAT terminal board is used to fan the LVDT signal pair to the TMR PCAA set: PCAA ( R), PCAA (S) and PCAA (T) through cabling. The BCAA acquisition board provides signal conditioning to convert the RMS voltage from the secondary-side of the LVDT to a dc equivalent signal read by the processor through analog-to-digital (A/D) converters.

The processor board will use one of the six independent digital servo regulators. The Liquid Fuel Valve with Position Feedback servo regulator is sampled at a 100 Hz rate. Details of the Liquid Fuel Valve with Position Feedback digital regulator are covered in the next section. The digital regulator output, ServoCurrentRef is written to a digital-to-analog (D/A) converter. The output of the D/A is the current command for the analog current regulator.

The BCAA acquisition board has six analog current regulators with a 10 mA rating. Each current output provides an internal suicide protection relay controlled by the BPPB software. Each of the six servo outputs supports either three-coil servos or two-coil servos and each provides a jumper on the TCAS terminal board to configure the output. The jumper is placed in the *TMR* position for the 3-coil servo and placed in the *Open* position for the 2-coil servo.

Servo outputs 1 and 2 also provide a means to externally suicide the outputs via the TCAS inputs SVRL1/2. For the Mark VIe the PPRO provides an external contact connected across SVRL1 and SVRL2. If the contact closes, the K1 relay is energized and the servo output is isolated from the digital regulator control, providing a direct connection through a current limiting resistor (15mA fixed output), as long as the K1 relay is energized.





## Digital Servo Regulator – Liquid Fuel with Position

The Digital Liquid Fuel with Position regulator is a proportional plus integral (PI) outer flow rate regulator with an inner proportional position regulator generating a servo current command. The Liquid Fuel with Position output is based on a multi-loop control using the liquid fuel flow rate feedback for the outer loop and the valve position for the inner loop feedback. Refer to the diagram *Digital Servo Regulator - Liquid Fuel with Position*.

The outer flow rate loop derives its feedback from either a single flow rate input or the maximum select of two flow rate inputs. For a single flow rate input, the configuration parameter *FlowInput1* is assigned to *FlowRate1* through *FlowRate4*. For the maximum select of two flow rates, the configuration parameter, *FlowInput1* is equal to one of four flow rate feedbacks and *FlowInput2* is equal to a different one of the four flow feedbacks. The Flow Rate Limit Check checks the range of the maximum select or the single feedback depending on the configuration. If the flow rate feedback, *Reg#\_FlowFdbk* is less than *FlowFdbkLoLim* or *Reg#\_PressureFlowFdbk* is greater than *FlowFdbkHiLim* then the flow loop is assumed to be open loop and the SRV servo out will suicide.

The flow rate error, *Reg#Ref* minus *Reg#FlowFdbk* has an integrator convergence error added to it. The objective of the convergence error is to keep the PI controller between PCAA (R), PCAA (S) and PCAA (T) together. The PI output for (R, S and T), *Reg#\_IntOut* is read by the controller. The median selected value, *Reg#\_IntConv* is calculated from the three inputs. Each LFBV regulator for R, S and T takes the average, subtracts its own PI output value from this, multiplies it by a gain value, *K\_Conv\_OuterReg* to come up with the convergence error to move the integrator for PI R, S and T together. The PI proportional gain, *K\_OuterReg* and the integral time constant, *Tau\_OuterReg* provide the PI adjustments. The clamping is controlled by the parameters: *HiLim\_OuterReg* and *LowLim\_OuterReg*. The PI outer loop output, *Reg#\_IntOut* is the position command for the inner position loop.

The inner position loop supports two feedback options: Single position feedback and the maximum select of two position feedbacks. Setting *PositionInput1* equal to one of the twelve LVDT inputs can configure the single position feedback option. The maximum select of two position feedbacks is selected when the configuration parameters, *PositionInput1* and *PositionInput2* are assigned to different LVDT inputs.

Each of the enabled position inputs run through a Position Calculation function that converts the dc volts signal representing RMS volts to a valve position in percent where 0% represents fully closed and 100% represents a fully open valve.

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**Note** The valve percent representation can also be configured for the opposite where 100% is equivalent to fully closed.

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The Position Limit function's input is the following based on the configuration: equal to the Position Calculation output for a single position feedback or equal to the maximum select from two Position Calculation outputs for the dual position input configuration. The Position Limit function checks the feedback range of *Reg#\_Fdbk*. The range defined in percent over nominal is configurable using the parameter, *Fdbk\_Suicide*; if enabled.

The proportional regulator error,  $\text{Reg\#\_Error}$  is equal to the position reference command from the controller,  $\text{Reg\#Ref}$  minus the position feedback,  $\text{Reg\#\_Fdbk}$ .  $\text{Reg\#\_Error}$  is multiplied by a composite gain defined by the multiplication of the configuration parameter,  $\text{RegGain}$  and the controller output,  $\text{Reg\#\_GainAdj}$ . The product of the gain and position error defines a current in percent. The amount of current required to negate the spring force used to close the valve if the servo fails is compensated by the configuration parameter,  $\text{RegNullBias}$ . The controller system output,  $\text{Reg\#\_NullCor}$  is used to correct the null bias value when one of the TMR servos suicides for some reason. The resultant output from the proportional position regulator is a current command in percent with the Monitor variable name,  $\text{ServoCurrentRef}$ .

After the initial configuration setting is made for the position loop, the user calibrates the position valve feedbacks. This is done by using ToolboxST to select the LVDT calibration mode and setting the controller output  $\text{CalibEnab\#}$  equal to TRUE. In the calibration mode, the user can use the servo output in the open-loop mode to force the valve to the fully closed position and also to the fully open position. During the calibration mode, the PCAA assigns the RMS voltage that represents the open and closed position to the configuration parameters:  $\text{MinVrms}$  and  $\text{MaxVrms}$ . The user selects *Calibrate and Save* to store the LVDT Excitation output voltage in the LVDT configurable parameter  $\text{ExcitMonCal}$ . The excitation voltage is used to compensate for excitation voltage changes during run time. The user must also verify that the LVDT parameter  $\text{ExcitSelect}$  comes from the proper Excitation voltage source (R, S, or T)

[illegible]

### Digital Servo Regulator - LiqFuel\_wPos

## Pulse Inputs

Mark VIe has shaft speed inputs on PTUR and PPRO and flow inputs on PSVO. PCAA is intended for use with PTUR and PPRO so PCAA does not include shaft speed inputs. PCAA includes two TTL (5v active) pulse rate inputs with output power. TCAT has two fanned magnetic pulse rate inputs. All inputs are for flow measurements associated with servo regulation and work up to 20,000 Hz. Pulse input accuracy is greater than  $\pm 0.05\%$  of full scale input.

## Specifications

The following table provides information specific to the PCAA module with the included TCAS terminal board.

| Item                          | Location    | Specification                                                                                                                                                                                                                               |
|-------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of Inputs              | PCAA        | 25 thermocouple inputs<br>Ten 4-20 mA inputs<br>Two 4-20 mA or $\pm 10$ V configurable inputs<br>Two active pulse rate inputs<br>One servo coil suicide relay input affecting the first two servo outputs                                   |
| Number of Outputs             | PCAA        | Six servo coil driver outputs<br>Two 4-20 mA outputs<br>One $\pm 12$ V dc power output<br>Six LVDT excitation outputs                                                                                                                       |
|                               | JGPA        | Twelve 24 V power outputs for 4-20 mA transmitters                                                                                                                                                                                          |
| <b>Signal Accuracy</b>        |             |                                                                                                                                                                                                                                             |
| Thermocouple inputs           | PCAA        | $\pm 0.10\%$ including all sources of error<br>$\pm 0.06\%$ typical at 25°C                                                                                                                                                                 |
| Analog 4-20 mA inputs         | PCAA & TCAT | $\pm 0.25\%$ including all sources of error<br>$\pm 0.10\%$ typical at 25°C                                                                                                                                                                 |
| Analog 0-10 V dc inputs       | PCAA        | $\pm 0.50\%$ including all sources of error<br>$\pm 0.20\%$ typical at 25°C                                                                                                                                                                 |
| Seismic inputs                | TCAT        | $\pm 2.00\%$ including all sources of error<br>$\pm 0.90\%$ typical at 25°C                                                                                                                                                                 |
| LVDT input                    | TCAT        | $\pm 1.00\%$ including all sources of error<br>$\pm 0.25\%$ typical at 25°C                                                                                                                                                                 |
| LVDT excitation monitor input | PCAA        | $\pm 1.00\%$ including all sources of error<br>$\pm 0.55\%$ typical at 25°C                                                                                                                                                                 |
| LVDT excitation output        | PCAA        | 7 V ac RMS $\pm 5.00\%$ including all error sources, $\pm 3.00\%$ typical at 25°C<br>3.2 kHz output sine wave frequency.<br>60 mA output drive current capability.<br>(LVDT position calculation uses monitor value, not excitation output) |
| Servo driver output           | PCAA        | $\pm 3.50\%$ including all sources of error<br>$\pm 0.70\%$ typical at 25°C                                                                                                                                                                 |
| Analog 4-20 mA output         | PCAA & TCAT | $\pm 0.75\%$ including all sources of error<br>$\pm 0.43\%$ typical at 25°C                                                                                                                                                                 |
| 24 V Power output             | JGPA & TCAT | 24 V dc $\pm 0.5\%$ over current ranges of 0 to 25 mA.                                                                                                                                                                                      |
| <b>Other Specifications</b>   |             |                                                                                                                                                                                                                                             |
| Power supply input voltage    |             | 28 V dc $\pm 5\%$                                                                                                                                                                                                                           |

## Physical

|             |      |                                              |
|-------------|------|----------------------------------------------|
| Size        | PCAA | 33.02 cm high x 17.8 cm wide (13 in x 7 in)  |
| Technology  | ALL  | Surface-mount                                |
| Temperature | ALL  | Operating: -30°C to 65°C (-22 °F to +149 °F) |

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## Diagnostics

The module performs the following self-diagnostic tests:

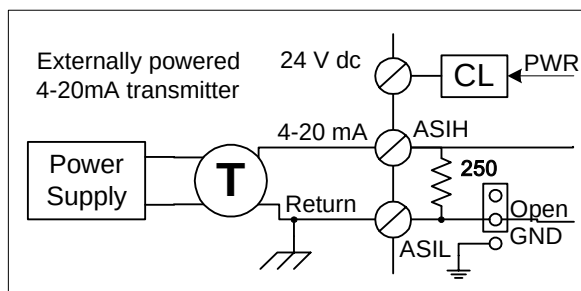
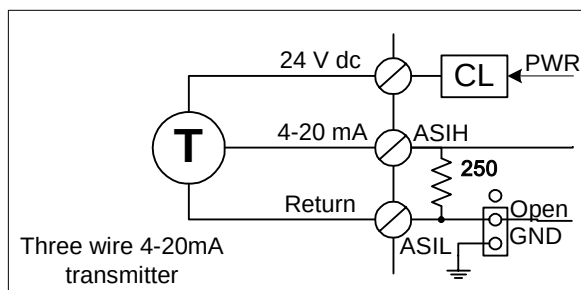
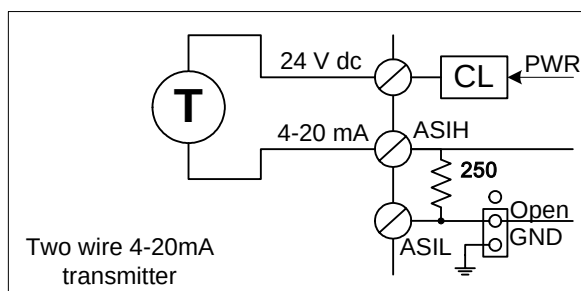
- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- As a group, the 4-20 mA analog inputs have a specified high and low current range for a valid signal. If a signal falls outside the specified range, the signal health is declared to be bad.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values, and are used to confirm the health of the analog to digital converter circuits. If the reference value does not fall within a defined range, an alarm is generated to indicate a potential problem with signal accuracy.
- Analog output current is sensed on the terminal board using a small burden resistor. The pack conditions this signal and compares it to the commanded current to confirm the health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.
- Thermocouple circuits are biased with a small dc current. If a thermocouple circuit opens, the temperature signal goes to a full-scale negative reading.
- Seismic input circuits are biased with a small dc current. If a seismic sensor circuit opens, an alarm is generated and the signal health is set to indicate a problem.

Details of the individual diagnostics are available from the ToolboxST. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy. Additional diagnostic information may be found in the module alarm listing.

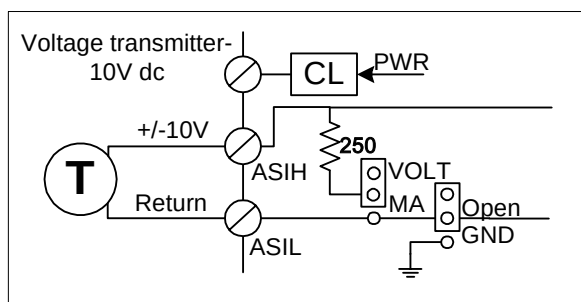
## Configuration

### Analog Input

The PCAA is able to interface to several different types of 4-20 mA transmitters. Each input has a jumper next to the terminals that is used to determine if the return terminal is grounded or floating. The default position of the jumper is floating or open. The JGPA board provides twelve 24 V dc terminals, one for each 4-20 mA transmitter input.



The last two 4-20 mA inputs on PCAA feature an additional jumper that removes the 250 Ω burden resistor for  $\pm 10$  V dc input applications. When the jumper is in the MA position, the input behaves the same as the first ten inputs. When the jumper is in the VOLT position the burden resistor is removed and the input acts as a voltage input.



| Jumper | Pos 1-2 | Pos 2-3 | Notes        |
|--------|---------|---------|--------------|
| JP1    | OPEN    | GND     | Analog In 1  |
| JP2    | OPEN    | GND     | Analog In 2  |
| JP3    | OPEN    | GND     | Analog In 3  |
| JP4    | OPEN    | GND     | Analog In 4  |
| JP5    | OPEN    | GND     | Analog In 5  |
| JP6    | OPEN    | GND     | Analog In 6  |
| JP7    | OPEN    | GND     | Analog In 7  |
| JP8    | OPEN    | GND     | Analog In 8  |
| JP9    | OPEN    | GND     | Analog In 9  |
| JP10   | OPEN    | GND     | Analog In 10 |
| JP11   | OPEN    | GND     | Analog In 11 |
| JP12   | OPEN    | GND     | Analog In 12 |
| JP13   | MA      | VOLT    | Analog In 11 |
| JP14   | MA      | VOLT    | Analog In 12 |

#### *Analog Input Jumper Summary*

### **Servo Output**

Correct position selection for servo configuration jumpers are listed under each servo regulator type.

| Jumper | Pos 1-2 | Pos 2-3 | Notes                |
|--------|---------|---------|----------------------|
| JP15   | TMR     | Simplex | Servo1 output select |
| JP16   | TMR     | Simplex | Servo2 output select |
| JP17   | TMR     | Simplex | Servo3 output select |
| JP18   | TMR     | Simplex | Servo4 output select |
| JP19   | TMR     | Simplex | Servo5 output select |
| JP20   | TMR     | Simplex | Servo6 output select |

### **Alarms**

#### **PCAA Module Alarms**

| Alarm ID | Alarm Description                                     | Possible Cause                                                   | Solution                                                                                                                                                     |
|----------|-------------------------------------------------------|------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2        | Flash memory CRC failure                              | Board firmware programming error (board will not go online)      | Rebuild system and download application and configuration to pack. If problem continues replace pack.                                                        |
| 3        | CRC failure override is active                        | Board firmware programming error (board is allowed to go online) | Rebuild system and download application and configuration to pack. If problem continues replace pack.                                                        |
| 4        | I/O pack in stand alone mode                          | Invalid command line option                                      | Rebuild system and download to pack.                                                                                                                         |
| 5        | I/O pack in remote I/O mode                           | Invalid command line option                                      | Rebuild system and download to pack.                                                                                                                         |
| 6        | Special user mode active. Now [ ]                     | Invalid command line option                                      | Rebuild system and download to pack.                                                                                                                         |
| 7        | I/O pack – The I/O pack has gone to the Offline state | Lost communication with controller                               | Check that controller has not gone off-line. If controller appears OK and other packs are not reporting a problem look for an IONet cable or switch problem. |

| Alarm ID | Alarm Description                                           | Possible Cause                                                                                                                                                                         | Solution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|-------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16       | System limit checking is disabled                           | System checking was disabled by configuration                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 30       | ConfigCompatCode mismatch; Firmware: [ ]                    | A .dll file (ToolboxST support file) has been installed that is incompatible with the firmware loaded on the I/O processor.                                                            | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 31       | IOCompatCode mismatch; Firmware: [ ]                        | A .dll file (ToolboxST support file) has been installed that is incompatible with the firmware loaded on the I/O processor.                                                            | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 32       | Unallowed VarIOCompatCode Change                            | A .dll file (ToolboxST support file) has been installed that is incompatible with the firmware loaded on the I/O processor.                                                            | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 33-67    | Thermocouple [ ] Unhealthy                                  | Thermocouple [ ] input to the analog to digital converter exceeded the converter limits OR exceeded the specified range of operation for the selected type of thermocouple input.      | The solution may be one of the following<br>-Check field wiring including shields. Check installation of PCAA on terminal board. Problem is usually not a PCAA or terminal board failure if other thermocouples are working correctly.<br>-The board has detected a thermocouple open and has applied a bias to the circuit driving it to a large negative number, or the TC is not connected, or a condition such as stray voltage or noise caused the input to exceed -63 mV.<br>-The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the cold junction compensation is wrong, or the thermocouple wiring is open. |
| 68       | Cold Junction Unhealthy, Using Backup                       | The local cold junction signal from the TCAT terminal board is out of range. The normal range is -30°C to 65°C (-22 °F to 145 °F).                                                     | If hardware is in the normal temperature range, then possible hardware failure of cold junction sensor on the TCAS board. Replace module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 69-80    | Analog Input (Simplex) [ ] unhealthy                        | TCAS Analog Input reading outside of limits. Check hardware for valid connections: Excitation to transducer, bad transducer, terminal board jumper settings, or open or short-circuit. | Check field wiring including shields. Problem is usually not a PCAA or terminal board failure if other Analog Inputs are working correctly. Check PCAA ground select jumper for the input. Check that Inputs are in Operable range (3.0-21.5 mA, ±5.25 V, ±10.5 V). Verify parameter settings for Min_MA_Input and Max_MA_Input.                                                                                                                                                                                                                                                                                                                                                              |
| 81-104   | Analog Input (Voted) [ ] unhealthy                          | TCAT Analog Input reading outside of limits. Check hardware for valid connections: Excitation to transducer, bad transducer, or open or short-circuit                                  | Check field wiring including shields. Problem is usually not a PCAA or terminal board failure if other Analog Inputs are working correctly. Check ground select jumper for the input. Ensure TCAT - PCAA cables are fully seated in connectors. Check that Inputs are in Operable range (3.0-21.5 mA) Verify parameter settings for Min_MA_Input and Max_MA_Input.                                                                                                                                                                                                                                                                                                                            |
| 105-116  | Vibration Input for Seismic (Velocity) Sensor [ ] unhealthy | Bad transducer, or open or short-circuit OR Incorrect configuration for sensor resistance (Ohms)                                                                                       | Check field wiring including shields. Problem is usually not a PCAA or terminal board failure if other vibration inputs are working correctly. Verify that the configured sensor resistance matches with resistance of actual sensor connected.                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 117-122  | LVDT Excitation [ ] Failed                                  | Excitation ground fault                                                                                                                                                                | Check field wiring including shields for LVDT Excitation Output. Problem is usually not a PCAA or terminal board failure if other LVDT Excitation Outputs are working correctly. Hardware failure, Replace hardware                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |



| Alarm ID | Alarm Description                                           | Possible Cause                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Solution                                                                                                                                                                                                                                                                                                                  |
|----------|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 123-134  | LVDT [ ] Servo Excitation Ratio Out of Range                | Incorrect Configuration parameter (ExcitMonCal), or terminal board failure                                                                                                                                                                                                                                                                                                                                                                                                    | ExcitMonCal is set during Servo regulator calibration and is a nominal Excitation value. If actual LVDT excitation goes out of range ( $\pm 10\%$ of ExcitMonCal), this alarm is generated. Check configuration parameter for proper value, recalibrate servo or replace the PCAA Module.                                 |
| 135-146  | LVDT [ ] Vrms Out of Hardware Limit                         | Excitation to LVDT, bad transducer, or open or short-circuit OR LVDT [ ] input to the analog to digital converter exceeded the converter limits. LVDT scaling configuration (MinVrms, MaxVrms) has not been calibrated.                                                                                                                                                                                                                                                       | Check field wiring including shields and LVDT Excitation. Problem is usually not a PCAA or terminal board failure if other LVDT inputs are working correctly. Calibrate servo regulator with the proper LVDT. Verify the configuration limits, MinVrms and MaxVrms.                                                       |
| 147-148  | Monitor [ ] Invalid Servo Configuration                     | Invalid set of configuration for selected type of regulator.                                                                                                                                                                                                                                                                                                                                                                                                                  | Check and correct the configuration parameters for selected type of regulator. Verify that Monitor regulator type matches Regulator type of selected servo.                                                                                                                                                               |
| 149      | More than One Servo Requested for Calibration               | Only one servo can be calibrated at given time, more than one request of servo calibration requested by user.                                                                                                                                                                                                                                                                                                                                                                 | Check variables <i>CalibEnab#</i> in the 'Variables' Tab & make sure that only One <i>CalibEnab#</i> for only One Servo is Set to 'True' at a given time.                                                                                                                                                                 |
| 150      | Calibration: Selected LVDT Max / Min Pos Limit Out of Range | Used to insure that all selected LVDTs are scaled to the same units. MaxPosValue or MinPosValue for Selected LVDT configured in 'PositionInput#1' in the Regulator Configuration is Out of range, i.e $\pm 50\%$ , encountered during calibration.                                                                                                                                                                                                                            | Check the Regulator Configuration for Parameter <i>PositionInput#1</i> for the particular Servo. Check the 'MaxPosValue' & 'MinPosValue' for LVDT# Selected input in <i>PositionInput#1</i> . The MaxPosValue for LVDT Input should be between 50% to 150%. The MinPosValue for LVDT Input should be between -50% to 50%. |
| 151-154  | FlowRate [ ] Input unhealthy                                | Possible broken wire on flow rate input. Diagnostic is generated when pulse rate was above 100 Hz, but then suddenly drops to 0.                                                                                                                                                                                                                                                                                                                                              | Check field wiring including shields. Problem is usually not a PCAA or terminal board failure if other Flow Rate Inputs are working correctly. Hardware failure, Replace hardware                                                                                                                                         |
| 155-160  | Servo [ ] Disabled: Configuration error                     | Any of the following may cause this error<br>-Servo Position input connected to unused LVDT<br>-Incorrect Position input configuration<br>-Servo Flow input connected to unused PR<br>-Incorrect Flow input configuration<br>-Servo Pressure input connected to unused Analog Input<br>-Incorrect Pressure input configuration                                                                                                                                                | Check and correct the configuration parameters for selected type of regulator. Check Inputs are connected to used sensor inputs in configuration.                                                                                                                                                                         |
| 161-166  | Servo [ ] Output Suicide Active                             | 1) Invalid/Incorrect Configuration:<br>-Any of the following may cause this error<br>-Servo Position input connected to unused LVDT<br>-Incorrect Position input configuration<br>-Servo Flow input connected to unused PR<br>-Incorrect Flow input configuration<br>-Servo Pressure input connected to unused Analog Input<br>-Incorrect Pressure input configuration,<br>2) Regulator Feedback out of range,<br>3) Servo Current feedback differs from Servo Current Output | Check and correct the configuration parameters for selected type of regulator. Check Inputs are connected to used sensor inputs in configuration.                                                                                                                                                                         |

| Alarm ID | Alarm Description                                           | Possible Cause                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Solution                                                                                                                                                                                                                             |
|----------|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 167-173  | Ref [ ] Reference Voltage out of limits                     | <p>The reference voltage for the analog inputs is more than <math>\pm 5\%</math> from the expected value. Indicates a reference, multiplexor, or A/D converter hardware problem.</p> <p>Ref 1,2 affect Thermocouples</p> <p>Ref 3,4 affect TCAT analog inputs</p> <p>Ref 5 affects TCAS analog inputs (1-10)</p> <p>Ref 6 affects vibration inputs</p> <p>Ref 7 affects LVDTs, Excitation monitor, analog inputs 11 &amp; 12, servo current feedbacks, analog output feedbacks.</p> | Check PCAA ground quality through mounting bolts. Cycle power on PCAA. Replace PCAA.                                                                                                                                                 |
| 174-180  | Null [ ] Null Voltage out of limits                         | <p>The Null voltage for the analog inputs is more than 5% from the expected value. Indicates a reference, multiplexor, or A/D converter hardware problem.</p> <p>Null 1,2 affect Thermocouples</p> <p>Null 3,4 affect TCAT analog inputs</p> <p>Null 5 affects TCAS analog inputs (1-10)</p> <p>Null 6 affects vibration inputs</p> <p>Null 7 affects LVDTs, Excitation monitor, analog inputs 11 &amp; 12, servo current feedbacks, analog output feedbacks.</p>                   | Check PCAA ground quality through mounting bolts. Cycle power on PCAA. Replace PCAA.                                                                                                                                                 |
| 181-183  | Analog Output [ ] Individual current unhealthy              | Bad transducer, or open or short-circuit                                                                                                                                                                                                                                                                                                                                                                                                                                            | Check field wiring including shields. Problem is usually not a PCAA or terminal board failure if other Analog outputs are working correctly.                                                                                         |
| 184-188  | Analog Output [ ] Total current unhealthy                   | Bad transducer, or open or short-circuit                                                                                                                                                                                                                                                                                                                                                                                                                                            | Check field wiring including shields. Check for indication of analog output suicide relay operation. Check PCAA- TCAT cables. Problem is usually not a PCAA or terminal board failure if other Analog outputs are working correctly. |
| 189-190  | Analog Output (Simplex)<br>[ ] 20 mA suicide active         | PCAA unable to control analog output current. Output removed by opening relay contacts. May be caused by excessive field wiring or connected device problems interfering with current, or terminal board failure.                                                                                                                                                                                                                                                                   | Check field wiring and status of connected device. Hardware failure, Replace PCAA TCAS Terminal board.                                                                                                                               |
| 190-193  | Analog Output (Voted) [ ] 20 mA suicide active              | PCAA unable to control analog output current. Output removed by opening relay contacts. May be caused by excessive field wiring or connected device problems interfering with current, or terminal board failure.                                                                                                                                                                                                                                                                   | Check field wiring and status of connected device. Ensure TCAT-PCAA cables are fully seated in connectors. Replace PCAA module. Replace TCAT terminal board.                                                                         |
| 194-195  | Analog Output (Simplex)<br>[ ] Suicide relay non-functional | The relay in series with the analog output has contact feedback. Suicide relay feedback does not match command.                                                                                                                                                                                                                                                                                                                                                                     | Hardware failure, Replace PCAA module.                                                                                                                                                                                               |
| 196-198  | Analog Output (Voted) [ ] Suicide relay non-functional      | The relay in series with the analog output has contact feedback. Suicide relay feedback does not match command.                                                                                                                                                                                                                                                                                                                                                                     | Hardware failure, Replace PCAA module.                                                                                                                                                                                               |

| Alarm ID | Alarm Description                                                 | Possible Cause                                                                                                                                                                                                                                                                                                              | Solution                                                                                                                                                                                                                                                                                      |
|----------|-------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 199-204  | Servo [ ] Position Feedback out of range                          | LVDT position feedback is outside of the specified range.                                                                                                                                                                                                                                                                   | Check the LVDT configuration settings, calibration, field wiring. Ensure that TCAT-PCAA cables are fully seated.                                                                                                                                                                              |
| 205-210  | Servo [ ] Pressure Feedback out of range                          | The pressure feedback used in a servo regulator is outside of the specified range.                                                                                                                                                                                                                                          | Check the source of the pressure signal including the sensor, field wiring, and configuration. Verify terminal board jumper settings for analog inputs.                                                                                                                                       |
| 211-216  | Servo [ ] Flow Feedback out of range                              | The flow feedback used in a servo regulator is outside of the specified range.                                                                                                                                                                                                                                              | If active pulse rate flow sensor- check power to device, field wiring, the sensor, and configuration. If magnetic pulse rate flow sensor, check device, field wiring, input configuration, and TCAT-PCAA cables.                                                                              |
| 217      | TCAT Configuration & Hardware Mismatch                            | TCAT configured in toolbox but Terminal Board not Connected or TCAT Not configured in toolbox but Terminal Board Connected. This diagnostic is only generated on power-up.                                                                                                                                                  | Verify that TCAT selection in Toolbox configuration matches actual hardware. Verify that P1 & P2 cable connections are not swapped. Verify TCAT Terminal Board P1 & P2 Cable connections are screwed down and all terminal boards are properly grounded. Perform a power down reset to clear. |
| 218      | TCAT Connector P1 & P2 Types Mismatch                             | The Type (Like R/R or S/S or T/T) of P1 & P2 connections between TCAT & TCAS do not match. The Valid Combinations are:<br><br>P1(TCAS)-PR1(TCAT) & P2(TCAS)-PR2(TCAT), P1(TCAS)-PS1(TCAT), P2(TCAS)-PS2(TCAT),<br><br>P1(TCAS)-PT1(TCAT), P2(TCAS)-PT2(TCAT).                                                               | Check Toolbox Configuration & TCAT Terminal Board P1 & P2 Cable connections between TCAS & TCAT. Check if there is no type (R/R,S/S,T/T) mismatch                                                                                                                                             |
| 221      | Calibration Mode Enabled                                          | One of the <strong>CalibEnab#</strong> outputs is set to <strong>True</strong> .                                                                                                                                                                                                                                            | Set <strong>CalibEnab#</strong> to <strong>False</strong> . This alarm is active to annunciate that the card is in a special mode where servo suicide protection has been disabled and the user needs to take special precautions in this mode.                                               |
| 256      | I/O pack [ ] V Power supply voltage is low                        | I/O pack input power is required to be within the range 28 V $\pm$ 5%. Input voltage has dropped below 18 V. I/O pack operation will be compromised or may stop completely.                                                                                                                                                 | If PPDA is available to monitor control cabinet power check that I/O pack for active alarms. Check I/O pack power within the control cabinet starting with power supplies and working toward the affected I/O pack.                                                                           |
| 257      | I/O pack [ ] V power supply voltage is low                        | I/O pack input power is required to be within the range 28V $\pm$ 5%. Input voltage has dropped below 26.5 V. In most cases normal pack operation will continue below this voltage but field devices that require 24 V from the terminal board may begin to experience reduced voltage operation with undetermined results. | If PPDA is available to monitor control cabinet power check that I/O pack for active alarms. Check I/O pack power within the control cabinet starting with power supplies and working toward the affected I/O pack.                                                                           |
| 258      | I/O pack Temperature<br>[ ] ° F is out of range<br>[ ] to [ ] ° F | Temperature went outside - 20°C to +85°C (-4 °F to +185 °F)                                                                                                                                                                                                                                                                 | The environmental controls applied to the cabinet containing the I/O pack should be checked. Pack operation will continue correctly beyond these temperature limits but long-term operation at elevated temperatures may reduce equipment life.                                               |
| 261      | Unable to read configuration file from flash                      | I/O pack does not have correct configuration file stored in flash file system.                                                                                                                                                                                                                                              | Rebuild system and download configuration to pack.                                                                                                                                                                                                                                            |
| 262      | Bad configuration file detected                                   | The configuration file in the pack is not compatible with the application code that is loaded.                                                                                                                                                                                                                              | Rebuild system and download application and configuration to pack.                                                                                                                                                                                                                            |

| Alarm ID | Alarm Description                                            | Possible Cause                                                                                                  | Solution                                                                                                                                                                                                                                                                                                                        |
|----------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 263      | I/O pack configuration – bad name detected                   | Wrong configuration file for I/O pack                                                                           | Rebuild system and download application and configuration to pack.                                                                                                                                                                                                                                                              |
| 264      | I/O pack configuration – bad config compatibility code       | Wrong configuration revision for I/O pack                                                                       | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                             |
| 265      | I/O pack mapper – EGD header size mismatch                   | Controller EGD revision code not supported                                                                      | 0                                                                                                                                                                                                                                                                                                                               |
| 266      | I/O pack configuration – configuration size mismatch         | The configuration file in the pack does not have the correct size to match the application code that is loaded. | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                             |
| 267      | FPGA – name mismatch detected                                | Wrong configuration for FPGA in I/O pack                                                                        | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                             |
| 268      | FPGA - incompatible revision: Found [ ]; Need[ ].            | Wrong revision of FPGA firmware                                                                                 | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                             |
| 269      | I/O pack mapper – initialization failure                     | Mapper process was not able to start                                                                            |                                                                                                                                                                                                                                                                                                                                 |
| 270      | I/O pack mapper – mapper terminated                          | Mapper process stopped, no communication                                                                        |                                                                                                                                                                                                                                                                                                                                 |
| 271      | I/O pack mapper – unable to Export Exchange [ ]              | EGD not being sent to Controller                                                                                |                                                                                                                                                                                                                                                                                                                                 |
| 272      | I/O pack mapper – Unable to Import Exchange [ ]              | Not receiving EGD information from Controller                                                                   |                                                                                                                                                                                                                                                                                                                                 |
| 273      | IONet-EGD message – Illegal version                          | EGD protocol version incorrect, greater than current version                                                    |                                                                                                                                                                                                                                                                                                                                 |
| 279      | Sys - Could not determine platform type from hardware        | Incorrect firmware version or hardware malfunction. The firmware could not recognize the host hardware type.    | Ensure all connectors are aligned properly and fully seated. Check firmware version for compatibility with platform, if OK, replace processor module.                                                                                                                                                                           |
| 280      | Sys - Platform hardware does not match runtime application   | The platform type identified in the application configuration does not match the actual hardware.               | Fix platform type in ToolboxST, rebuild and download application.                                                                                                                                                                                                                                                               |
| 281      | Sys - FPGA not programmed due to platform errors             |                                                                                                                 |                                                                                                                                                                                                                                                                                                                                 |
| 282      | Sys - Unable to initialize application independent processes | Runtime malfunction. An application-independent firmware process could not be started successfully.             | Reload firmware and application and reboot. For Controller, if failure persists remove CompactFlash module and reprogram boot loader using ToolboxST Download Flash Bootloader pick, then, after reinstalling the flash module and rebooting, reload firmware and application. If this does not work, replace processor module. |
| 283      | Sys - Process disconnected illegally.                        | Runtime or hardware malfunction. A runtime process has crashed.                                                 | Reload firmware and application and reboot. For controller if failure persists remove CompactFlash module and reprogram boot loader using ToolboxST Download Flash Bootloader pick, then, after reinstalling the flash module and rebooting, reload firmware and application. If this does not work, replace processor module.  |

| Alarm ID | Alarm Description                                                           | Possible Cause                                                                                                                                                                                                       | Solution                                                                                                                     |
|----------|-----------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| 293      | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | I/O pack is waiting to obtain a network address from the controller using DHCP. This could be a network problem, a controller problem, or pack not configured correctly, or incorrect ID (barcode).                  | Check that controller is on line. Confirm correct terminal board ID is present in ToolboxST. Check IONet (switches, cables). |
| 295      | IOPACK - The FPGA is not generating an I/O interrupt                        | Internal to the I/O pack there is a FPGA that controls I/O hardware. The logic in the FPGA generates an interrupt to the processor requesting that the I/O be serviced. That interrupt is not occurring as expected. | Rebuild system and download to pack. If problem continues replace pack as there may be a hardware problem with the FPGA.     |
| 300      | Application Code Load Failure                                               | Invalid application configuration, firmware or hardware malfunction.                                                                                                                                                 | Rebuild and download application to all processors; reload firmware and application; replace processor module.               |
| 301      | IO pack - XML files are missing                                             | I/O pack IO configuration files missing                                                                                                                                                                              | Rebuild system and download application and configuration to pack.                                                           |
| 314      | Controller pid [ ], exch [ ] timed out, IONet [ ].                          | I/O pack outputs not received from controller                                                                                                                                                                        |                                                                                                                              |
| 315      | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                                                                          |                                                                                                                              |
| 316      | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                                                                                      |                                                                                                                              |
| 317      | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with minor signature different than expected                                                                                                                                      |                                                                                                                              |
| 318      | Controller pid [ ], exch [ ] cfg timestamp mismatch, IONet [ ]              | I/O pack outputs exchange received with configuration timestamp different than expected                                                                                                                              |                                                                                                                              |
| 1008     | R Controller-Net A: exchange timed out                                      |                                                                                                                                                                                                                      |                                                                                                                              |
| 1009     | S Controller-Net A: exchange timed out                                      |                                                                                                                                                                                                                      |                                                                                                                              |
| 1010     | T Controller-Net A: exchange timed out                                      |                                                                                                                                                                                                                      |                                                                                                                              |
| 1264     | R Controller-Net B: exchange timed out                                      |                                                                                                                                                                                                                      |                                                                                                                              |
| 1265     | S Controller-Net B: exchange timed out                                      |                                                                                                                                                                                                                      |                                                                                                                              |
| 1266     | T Controller-Net B: exchange timed out                                      |                                                                                                                                                                                                                      |                                                                                                                              |

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# ***TCAT Core Analog Terminal Board***

## ***Functional Description***

The Core Analog (TCAT) terminal board provides additional I/O terminals for the PCAA module. It handles input signals that are fanned to one or three PCAA modules. Inputs include twelve seismic, twelve LVDT, twenty four 4-20 mA, and two magnetic pulse rate inputs. An individual 24 V dc power source is included for all twenty four 4-20 mA inputs with half on TCAT and half on an adjacent JGPA board. TCAT outputs consist of three 4-20 mA voted signals.

Field wire terminal points are provided by 120 pluggable Euro-style box terminals. Terminal grouping is a set of 48 terminals, a set of 24, and a second set of 48. A JGPA board adjacent to the TCAT field terminals provides twelve additional 24 V dc outputs for 4-20 mA devices as well as shield wire terminals. Power to JGPA is supplied by TCAT connector P3 or P4 and is the diode-or of power from the connected PCAA modules.

Pairs of 68 pin cables provide connection between TCAT and one or more PCAA modules. PR1 and PR2 go to a PCAA connected to the R IONet. PS1 and PS2 go to a PCAA connected to the S IONet. PT1 and PT2 go to a PCAA connected to the T IONet. TCAT provides an electronic ID on each cable connection. Cables are always used in pairs and PCAA uses the electronic ID to confirm that correct TCAT cables are in place.



## Installation

TCAT with an underlying insulating plastic carrier mounts to a metal back base. Screws are located at the top and bottom of the field terminals with a third screw approximately in the center of the board.

## Wiring

The TCAT terminal board features 120 pluggable Euro-style box terminals. A JGPA board mounts adjacent to the TCAT terminal board and uses Euro-style box terminals to provide forty eight shield termination points plus twelve 24 V dc output terminals for 4-20 mA transmitters. The Euro-style box terminals on TCAT accept conductors with the following characteristics:

| Conductor Type                                                                    | Minimum              | Maximum             |
|-----------------------------------------------------------------------------------|----------------------|---------------------|
| Conductor cross section solid                                                     | 0.2 mm <sup>2</sup>  | NA                  |
| Conductor cross section solid                                                     | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded                                                  | 0.2 mm <sup>2</sup>  | NA                  |
| Conductor cross section stranded                                                  | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded, with ferrule without plastic sleeve             | 0.25 mm <sup>2</sup> | NA                  |
| Conductor cross section stranded, with ferrule without plastic sleeve             | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded, with ferrule with plastic sleeve                | 0.25 mm <sup>2</sup> | NA                  |
| Conductor cross section stranded, with ferrule with plastic sleeve                | NA                   | 2.5 mm <sup>2</sup> |
| Conductor cross section AWG/kcmil                                                 | 24 AWG               | NA                  |
| Conductor cross section AWG/kcmil                                                 | NA                   | 12 AWG              |
| 2 conductors with same cross section, solid                                       | 0.2 mm <sup>2</sup>  | NA                  |
| 2 conductors with same cross section, solid                                       | NA                   | 1 mm <sup>2</sup>   |
| 2 conductors with same cross section, stranded                                    | 0.2 mm <sup>2</sup>  | NA                  |
| 2 conductors with same cross section, stranded                                    | NA                   | 1.5 mm <sup>2</sup> |
| 2 conductors with same cross section, stranded, ferrules without plastic sleeve   | 0.25 mm <sup>2</sup> | NA                  |
| 2 conductors with same cross section, stranded, ferrules without plastic sleeve   | NA                   | 1 mm <sup>2</sup>   |
| 2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve | 0.5 mm <sup>2</sup>  | NA                  |
| 2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve | NA                   | 1.5 mm <sup>2</sup> |

*TCAT Terminal Conductor Size Range*



The following table lists the terminal assignments for the TCAT terminal board

**TCAT Screw Terminal Assignments**

|    | <b>Name</b> | <b>Function</b>          |    | <b>Name</b> | <b>Function</b>    |
|----|-------------|--------------------------|----|-------------|--------------------|
| 1  | AFT1H       | Analog Fanned #1         | 41 | AFT14H      | Analog Fanned # 14 |
| 2  | AFT1L       |                          | 42 | AFT14L      |                    |
| 3  | AFT2H       | Analog Fanned #2         | 43 | AFT15H      | Analog Fanned # 15 |
| 4  | AFT2L       |                          | 44 | AFT15L      |                    |
| 5  | AFT3H       | Analog Fanned # 3        | 45 | AFT16H      | Analog Fanned # 16 |
| 6  | AFT3L       |                          | 46 | AFT16L      |                    |
| 7  | AFT4H       | Analog Fanned # 4        | 47 | AFT17H      | Analog Fanned # 17 |
| 8  | AFT4L       |                          | 48 | AFT17L      |                    |
| 9  | AFT5H       | Analog Fanned # 5        | 49 | AFT18H      | Analog Fanned # 18 |
| 10 | AFT5L       |                          | 50 | AFT18L      |                    |
| 11 | AFT6H       | Analog Fanned # 6        | 51 | AFT19H      | Analog Fanned # 19 |
| 12 | AFT6L       |                          | 52 | AFT19L      |                    |
| 13 | AFT7H       | Analog Fanned # 7        | 53 | AFT20H      | Analog Fanned # 20 |
| 14 | AFT7L       |                          | 54 | AFT20L      |                    |
| 15 | AFT8H       | Analog Fanned # 8        | 55 | AFT21H      | Analog Fanned # 21 |
| 16 | AFT8L       |                          | 56 | AFT21L      |                    |
| 17 | AFT9H       | Analog Fanned # 9        | 57 | AFT22H      | Analog Fanned # 22 |
| 18 | AFT9L       |                          | 58 | AFT22L      |                    |
| 19 | AFT10H      | Analog Fanned # 10       | 59 | AFT23H      | Analog Fanned # 23 |
| 20 | AFT10L      |                          | 60 | AFT23L      |                    |
| 21 | AFT11H      | Analog Fanned # 11       | 61 | AFT24H      | Analog Fanned # 24 |
| 22 | AFT11L      |                          | 62 | AFT24L      |                    |
| 23 | AFT12H      | Analog Fanned # 12       | 63 | VFIH1       | Seismic Input # 1  |
| 24 | AFT12L      |                          | 64 | VFIL1       |                    |
| 25 | APWR13      | 24 V power<br>no connect | 65 | VFIH2       | Seismic Input # 2  |
| 26 |             |                          | 66 | VFIL2       |                    |
| 27 | APWR14      |                          | 67 | VFIH3       | Seismic Input # 3  |
| 28 | APWR15      |                          | 68 | VFIL3       |                    |
| 29 | APWR16      |                          | 69 | VFIH4       | Seismic Input # 4  |
| 30 | APWR17      |                          | 70 | VFIL4       |                    |
| 31 | APWR18      |                          | 71 | VFIH5       | Seismic Input # 5  |
| 32 | APWR19      |                          | 72 | VFIL5       |                    |
| 33 | APWR20      |                          | 73 | VFIH6       | Seismic Input # 6  |
| 34 | APWR21      |                          | 74 | VFIL6       |                    |
| 35 | APWR22      |                          | 75 | VFIH7       | Seismic Input # 7  |
| 36 | APWR23      |                          | 76 | VFIL7       |                    |
| 37 | APWR24      |                          | 77 | VFIH8       | Seismic Input # 8  |
| 38 | PCOM        | Common                   | 78 | VFI8L       |                    |
| 39 | AFT13H      | Analog Fanned # 13       | 79 | VFI9H       | Seismic Input # 9  |
| 40 | AFT13L      |                          | 80 | VFI9L       |                    |

**TCAT Screw Terminal Assignments**

|     | <b>Name</b> | <b>Function</b>       |     | <b>Name</b> | <b>Function</b> |
|-----|-------------|-----------------------|-----|-------------|-----------------|
| 81  | VFIH10      | Seismic Input # 10    | 101 | LVDT6H      | LVDT Input # 6  |
| 82  | VFIL10      |                       | 102 | LVDT6L      |                 |
| 83  | VFIH11      | Seismic Input # 11    | 103 | LVDT7H      | LVDT Input # 7  |
| 84  | VFIL11      |                       | 104 | LVDT7L      |                 |
| 85  | VFIH12      | Seismic Input # 12    | 105 | LVDT8H      | LVDT Input # 8  |
| 86  | VFIL12      |                       | 106 | LVDT8L      |                 |
| 87  | MFI1H       | Mag pickup flow input | 107 | LVDT9H      | LVDT Input # 9  |
| 88  | MFI1L       |                       | 108 | LVDT9L      |                 |
| 89  | MFI2H       | Mag pickup flow input | 109 | LVDT10H     | LVDT Input # 10 |
| 90  | MFI2L       |                       | 110 | LVDT10L     |                 |
| 91  | LVDT1H      | LVDT Input # 1        | 111 | LVDT11H     | LVDT Input # 11 |
| 92  | LVDT1L      |                       | 112 | LVDT11L     |                 |
| 93  | LVDT2H      | LVDT Input # 2        | 113 | LVDT12H     | LVDT Input # 12 |
| 94  | LVDT2L      |                       | 114 | LVDT12L     |                 |
| 95  | LVDT3H      | LVDT Input # 3        | 115 | ATOH3       | TMR 4-20 mA     |
| 96  | LVDT3L      |                       | 116 | ATOL3       |                 |
| 97  | LVDT4H      | LVDT Input # 4        | 117 | ATOH4       | TMR 4-20 mA     |
| 98  | LVDT4L      |                       | 118 | ATOL4       |                 |
| 99  | LVDT5H      | LVDT Input # 5        | 119 | ATOH5       | TMR 4-20 mA     |
| 100 | LVDT5L      |                       | 120 | ATOL5       |                 |

## Operation

TCAT provides fanning of input signals to one or more PCAA modules. This is done with high reliability passive circuits to ensure reliability in redundant applications.

TCAT accepts 28 V dc power from connected PCAA modules. It then does a diode-or of the power sources to obtain redundant power input for the 24 V dc outputs. Each 24 V output on TCAT is provided with an individual voltage regulator that includes thermal shutdown for branch circuit protection.

**Note** An over current condition on one 24 V dc output will result in only that output being shut down. When the overload is removed the terminal will return to 24 V dc.

TCAT accepts  $\pm 15$  V dc power from connected PCAA modules. It then does a diode-or of the power sources to obtain redundant power. The  $\pm 15$  V dc power is then used internally to voltage bias the seismic inputs.

## ***Specifications***

Please refer to the signal specifications listed in the PCAA documentation for details of the signals on TCAT.

| <b>Item</b>          | <b>Specification</b>                                                                                                                                                  |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs     | Twenty-four 4-20 mA signals.<br>Twelve seismic signals.<br>Twelve LVDT windings.<br>Two magnetic pulse rate flow signals.                                             |
| Number of outputs    | Three 4-20 mA hardware voted analog outputs.<br>Twelve 24 V dc outputs with 25 mA capability.<br>Twelve 24 V dc additional outputs on JGPA with 25 mA capability.     |
| Power supply voltage | 28 V dc $\pm 5\%$ from one or more PCAA modules.<br>$\pm 15$ V dc from one or more PCAA modules.<br>(both supplies routed through the cabling between PCAA and TCAT). |
| Pulse rate input     | Minimum signal for proper measurement at 2 Hz is 33 mVpk, and at 12 kHz is 827 mVpk.                                                                                  |
| <b>Physical</b>      |                                                                                                                                                                       |
| Size                 | 33.02 cm high x 17.8 cm wide (13 in x 7 in)                                                                                                                           |
| Technology           | Surface-mount                                                                                                                                                         |
| Temperature          | Operating: -30°C to 65°C (-22 °F to +149 °F)                                                                                                                          |

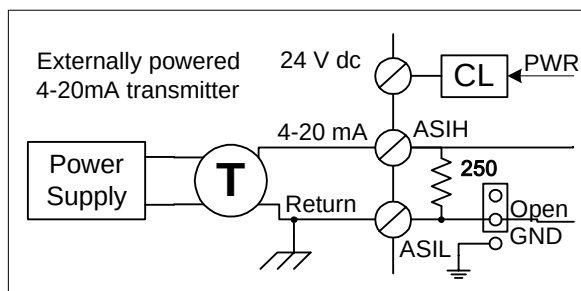
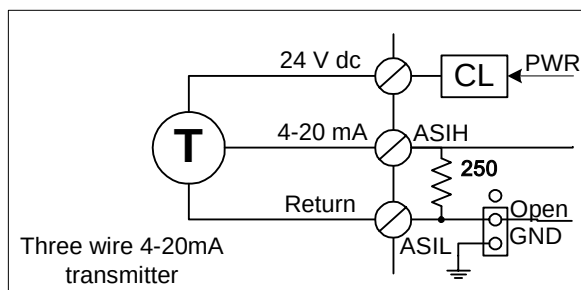
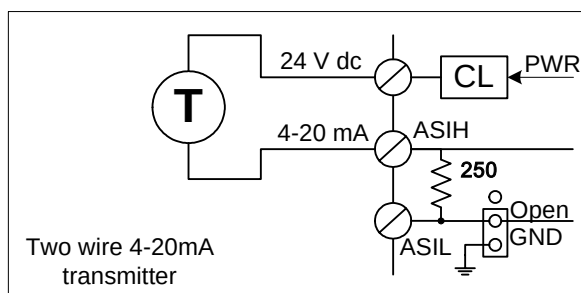
## ***Diagnostics***

All diagnostics associated with TCAT are performed in PCAA and documented for that module.

## Configuration

### Analog Input

The TCAT is able to interface with several different types of 4-20 mA transmitters. Each input has a jumper next to the terminals that is used to determine if the return terminal is grounded or floating. The default position of the jumper is floating or open. The combination of TCAT + JGPA provides twenty-four 24 V dc terminals, one for each 4-20 mA transmitter input.



## JGPA Ground and Power Board

### Functional Description

The PCAA core analog module and TCAT terminal board each provide twelve 4-20 mA inputs that are not provided with 24 V power for field devices. The Ground and Power (JGPA) board is a long narrow board that mounts adjacent to PCAA where shield wires are terminated. JGPA provides shield wire terminal points that may be tied directly to the underlying functional earth sheet metal or wired to a preferred grounding point. In this respect it is very similar to the JGND board offered as an option with other Mark VIe terminal boards. JGPA also provides twelve individually regulated and protected 24 V field device power outputs. Each output is sufficient to power a single 4-20 mA field device.

JGPA receives power from PCAA or TCAT through a 28 V power feed on connector P1. Power passes through twelve regulators and is available on TB3 screws 1-12. TB3 uses terminals colored orange to set them apart from the terminals provided for shield wire termination. Shield terminals are on TB1 and TB2 using twenty-four conventional green euro-style box terminals for each.

## ***Installation***

JGPA is installed adjacent to the terminals on PCAA and TCAT. Power is provided to JGPA through a cable from P1 to PCAA or TCAT. JGPA mounts on a sheet metal bracket that is at ground potential. When mounted with conductive hardware the ground path for JGPA shield wires is through the mounting bracket. If alternate shield wire grounding is desired the JGPA may be mounted with non-conductive washers and hardware. With isolated mounting, ground is defined by one or more wires from JGPA shield ground terminals to the desired ground location.

The terminals on JGPA have the following conductor capacities.

| <b>Conductor Type</b>                                                             | <b>Minimum</b>       | <b>Maximum</b>      |
|-----------------------------------------------------------------------------------|----------------------|---------------------|
| Conductor cross section solid                                                     | 0.2 mm <sup>2</sup>  |                     |
| Conductor cross section solid                                                     |                      | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded                                                  | 0.2 mm <sup>2</sup>  |                     |
| Conductor cross section stranded                                                  |                      | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded, with ferrule without plastic sleeve             | 0.25 mm <sup>2</sup> |                     |
| Conductor cross section stranded, with ferrule without plastic sleeve             |                      | 2.5 mm <sup>2</sup> |
| Conductor cross section stranded, with ferrule with plastic sleeve                | 0.25 mm <sup>2</sup> |                     |
| Conductor cross section stranded, with ferrule with plastic sleeve                |                      | 2.5 mm <sup>2</sup> |
| Conductor cross section AWG/kcmil                                                 | 24 AWG               |                     |
| Conductor cross section AWG/kcmil                                                 |                      | 12 AWG              |
| 2 conductors with same cross section, solid                                       | 0.2 mm <sup>2</sup>  |                     |
| 2 conductors with same cross section, solid                                       |                      | 1 mm <sup>2</sup>   |
| 2 conductors with same cross section, stranded                                    | 0.2 mm <sup>2</sup>  |                     |
| 2 conductors with same cross section, stranded                                    |                      | 1.5 mm <sup>2</sup> |
| 2 conductors with same cross section, stranded, ferrules without plastic sleeve   | 0.25 mm <sup>2</sup> |                     |
| 2 conductors with same cross section, stranded, ferrules without plastic sleeve   |                      | 1 mm <sup>2</sup>   |
| 2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve | 0.5 mm <sup>2</sup>  |                     |
| 2 conductors with same cross section, stranded, TWIN ferrules with plastic sleeve |                      | 1.5 mm <sup>2</sup> |

## ***Operation***

JGPA provides regulated 24 V dc power to the twelve terminals of TB3.

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**Note** An over current condition on one 24 V dc output results in only that output being shut down. When the overload is removed, the terminal returns to 24 V dc.

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## ***Specifications***

| <b>Item</b>             | <b>Specification</b>                                                                                   |
|-------------------------|--------------------------------------------------------------------------------------------------------|
| Number of ground points | 24 terminals on TB1 and 24 terminals on TB2. Ground points use green terminal housings.                |
| Outputs                 | 12 outputs at 24 V dc $\pm 5\%$ , 30 mA capability on TB3. Power outputs use orange terminal housings. |
| <b>Physical</b>         |                                                                                                        |
| Size                    | 33 cm high x 3.2 cm wide (13 in x 1.25 in)                                                             |
| Technology              | Through hole                                                                                           |
| Temperature             | Operating: -30°C to 65°C (-22 °F to +149 °F)                                                           |

## ***Diagnostics***

There are no diagnostics specifically associated with JGPA, only those relating to devices that may be powered by JGPA.

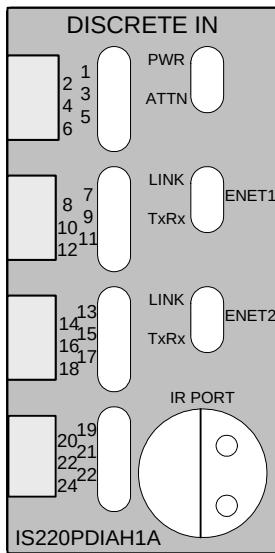
## ***Configuration***

There is no configuration associated with JGPA.

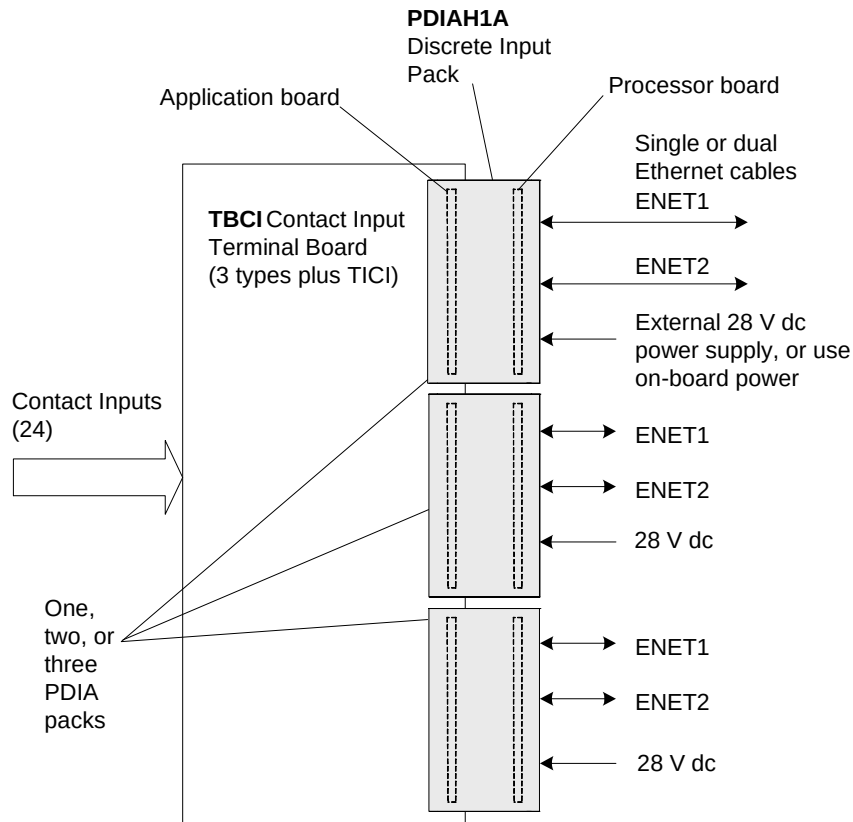
# PDIA Discrete Input

## PDIA Discrete Input

### Functional Description



The Discrete Input (PDIA) pack provides the electrical interface between one or two I/O Ethernet networks and a discrete input terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs and an acquisition board specific to the discrete input function. The pack accepts up to 24 contact inputs and terminal board specific feedback signals, PDIA accepts three different voltage levels (with types TBCIH1, H2 and H3 terminal boards). Connections for the isolated discrete input board with voltage sensing (with type TICI board) are available. System input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Discrete signal input is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PDIAH1A is compatible with five types of discrete contact input terminal boards, including the TBCI boards, TICI boards, STCI boards, but not the DIN-rail mounted DTCI board. The following table gives details of the compatibility:

| Terminal Board | TBCIH1, H2, H3 & TICI |            |         | DTCI | STCIH1A     |
|----------------|-----------------------|------------|---------|------|-------------|
| Control mode   | Simplex-yes           | Dual - yes | TMR-yes | No   | Simplex-yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

## Installation

### ➤ To install the PDIA pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PDIA I/O pack for simplex or three PDIA I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

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**Note** The PDIA mounts directly on a Mark VIe terminal board. Simplex terminal boards have a single DC-37 pin connector that receives the PDIA. TMR-capable terminal boards have three DC-37 pin connectors, one used for simplex operation, two for dual operation, and three for TMR operation. PDIA directly supports all of these connections.

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# Operation

## Processor

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

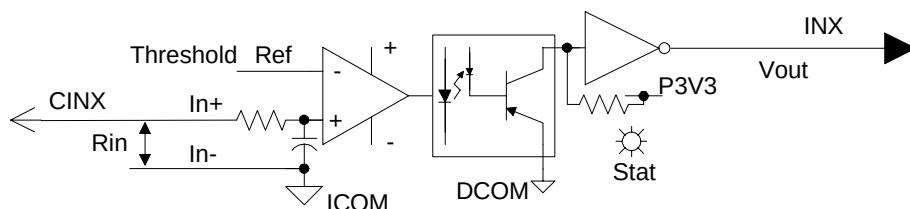
The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## Input Signals

The discrete input acquisition board provides the second stage of signal conditioning and level shifting to interface the terminal board inputs to the control logic. Initial signal conditioning is provided on the terminal board. The discrete input acquisition input circuit is a comparator with a variable threshold. Each input is isolated from the control logic through an opto-coupler and an isolated power supply. The inputs are not isolated from each other. Each of the twenty-four inputs has filtering, hysteresis, and a yellow status LED, that indicates when an input is picked up. The LED will be OFF when the input is dropped-out.



### Variable Threshold

The input threshold is derived from the contact wetting voltage input terminal. In most applications this voltage is scaled to provide a 50% input threshold. This threshold is clamped to 13% to prevent an indeterminate state if the contact wetting voltage drops to zero. If the contact wetting voltage drops below 40% of the nominal voltage, the under-voltage detector annunciates this condition to the control. A special test mode is provided to force the inputs from the control pack. Every four seconds, the threshold is pulsed high and then low and the response of the opto-couplers is checked. Non-responding inputs are alarmed.

### ID Line

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

### Power Management

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Connectors

The pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

## Specifications

| Item                    | Specification                                                                                                     |
|-------------------------|-------------------------------------------------------------------------------------------------------------------|
| Number of channels      | 24 dry contact voltage input channels                                                                             |
| Input isolation in pack | Optical isolation to 1500 V on all inputs                                                                         |
| Input Filter            | Hardware filter, 4 ms                                                                                             |
| Ac voltage rejection    | 60 V r ms @ 50/60 Hz at 125 V dc excitation                                                                       |
| Frame rate              | System dependent scan rate for control purposes<br>1,000 Hz scan rate for sequence of events monitoring           |
| Fault detection         | Loss of contact input excitation voltage<br>Non-responding contact input in test mode<br>Incorrect terminal board |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Monitoring for loss of contact input excitation voltage on the terminal board
- Detecting a non-responding contact input during diagnostic test. In this test, the threshold is pulsed high and low and the response of the opto-couplers is checked.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter              | Description                                      | Choices                  |       |
|------------------------|--------------------------------------------------|--------------------------|-------|
| PDIA_Mod_Configuration |                                                  |                          |       |
| System Limits          | Enable all system limit checking                 | Enable, disable          |       |
| Redundancy             | Redundancy mode of the pack                      | Simplex, Dual, TMR       |       |
| PDIA_Input             | Terminal board connected to PDIA                 | Connected, not connected |       |
| Contact Input          |                                                  |                          |       |
| Signal Invert          | Inversion makes signal true if contact is open   | Normal, Invert           |       |
| Sequence of Events     | Record contact transitions in sequence of events | Enable, disable          |       |
| Diag Vote Enable       | Enable voting disagreement diagnostic            | Enable, disable          |       |
| Signal Filter          | Contact input filter in msec                     | 0, 10, 20, 50            |       |
| IS22PDIA               |                                                  | Direction                | Type  |
| L3DIAG_PDIA            | I/O diagnostic indication                        | Input                    | BIT   |
| LINK_OK_PDIA           | I/O link okay indication                         | Input                    | BIT   |
| ATTN_PDIA              | I/O attention indication                         | Input                    | BIT   |
| IOPackTmpr             | I/O pack temperature                             | Input                    | FLOAT |
| IS200TBCI PointDefs    |                                                  |                          |       |
| Contact01              |                                                  |                          |       |
| :                      |                                                  |                          |       |
| Contact24              |                                                  |                          |       |

# Alarms

## PDIA Specific Alarms

| Alarm ID | Alarm Description                                       | Possible Cause                                                                                              | Solution                                                                                                                                                                        |
|----------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32-55    | Contact Input [ ] not responding to low self-test mode  | The input hardware internal to I/O pack has experienced a failure.                                          | Replace I/O pack                                                                                                                                                                |
| 56-79    | Contact Input [ ] not responding to high self-test mode | The input hardware internal to I/O pack has experienced a failure.                                          | Replace I/O pack                                                                                                                                                                |
| 112-135  | Logic Signal [ ] Voting Mismatch                        | In a TMR application the values for the specified contact do not agree between R, S, and T.                 | Verify R, S, and T I/O packs are equal with ToolboxST configuration.<br>Check I/O pack power and networking.<br>Check I/O pack mounting on terminal board.<br>Replace I/O pack. |
| 240      | Excitation Voltage not valid, Contact Inputs not valid  | The contact wetting voltage applied to the terminal board is not within the acceptable range for the board. | Check power distribution and wiring to ensure correct wetting power is applied to the terminal board.                                                                           |

## I/O Pack Alarms

| Fault | Fault Description                                         | Possible Cause                                                                                                                                            |
|-------|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                  | Board firmware programming error (board will not go online)                                                                                               |
| 3     | CRC failure override is active                            | Board firmware programming error (board is allowed to go online)                                                                                          |
| 4     | I/O pack in stand alone mode                              | Invalid command line option                                                                                                                               |
| 5     | I/O pack in remote I/O mode                               | Invalid command line option                                                                                                                               |
| 6     | Special user mode active. Now [ ]                         | Invalid command line option                                                                                                                               |
| 7     | I/O pack – The I/O pack has gone to the offline state     | Lost communication with controller                                                                                                                        |
| 16    | System limit checking is disabled                         | System checking was disabled by configuration                                                                                                             |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                  | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                      | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                | Supply voltage below 26.5 V dc                                                                                                                            |
| 257   | I/O pack power supply voltage is low                      | Supply voltage below 18 V dc                                                                                                                              |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                |
| 261   | Unable to read configuration file from flash              | Need to download configuration to the pack                                                                                                                |
| 262   | Bad configuration file detected                           | Configuration file not compatible, re-download                                                                                                            |
| 263   | I/O pack configuration – bad name detected                | Wrong configuration file for I/O pack                                                                                                                     |
| 264   | I/O pack configuration – bad config compatibility code    | Wrong configuration revision for I/O pack                                                                                                                 |
| 265   | I/O pack mapper – EGD header size mismatch                | Controller EGD revision code not supported                                                                                                                |
| 266   | I/O pack configuration – configuration size mismatch      | Incorrect configuration file size received                                                                                                                |
| 267   | FPGA – name mismatch detected                             | Wrong configuration for FPGA in I/O pack                                                                                                                  |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]         | Wrong revision of FPGA firmware                                                                                                                           |
| 269   | I/O pack mapper – initialization failure                  | Mapper process was not able to start.                                                                                                                     |
| 270   | I/O pack mapper – mapper terminated                       | Mapper process stopped, no communication                                                                                                                  |
| 271   | I/O pack mapper – unable to Export Exchange [ ]           | EGD not being sent to Controller                                                                                                                          |

| <b>Fault</b> | <b>Fault Description</b>                                                    | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 272          | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                           |
| 273          | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                            |
| 274          | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                    |
| 275          | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                            |
| 276          | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                |
| 277          | IONet-EGD – Signature mismatch E_Id= [ ]P_Id= [ ], =Expctd= [ ], Rcvd= [ ]  | Message version mismatch                                                                |
| 278          | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                           |
| 293          | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                             |
| 301          | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                |
| 314          | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                           |
| 315          | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                             |
| 316          | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected         |
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ]             | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                                   | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated                           | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                             | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch                          | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                             | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                                    | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                                  | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                             | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                               | Config Shmem CRC changed                                                                |

---

# ***TBCI Contact Input with Group Isolation***

## ***Functional Description***

The Contact Input with Group Isolation (TBCI) terminal board accepts 24 dry contact inputs wired to two barrier-type terminal blocks. Dc power is wired to TBCI for contact excitation. The contact inputs have noise suppression circuitry to protect against surge and high-frequency noise.

## ***Mark VI Systems***

In the Mark\* VI system, TBCI works with VTCC/VCRC and supports simplex and TMR applications. Cables with molded plugs connect TBCI to VME rack where the VCCC or VCRC processor board is located. Both board versions TBCIH\_B and TBCIH\_C work correctly with Mark VI and are functionally identical.

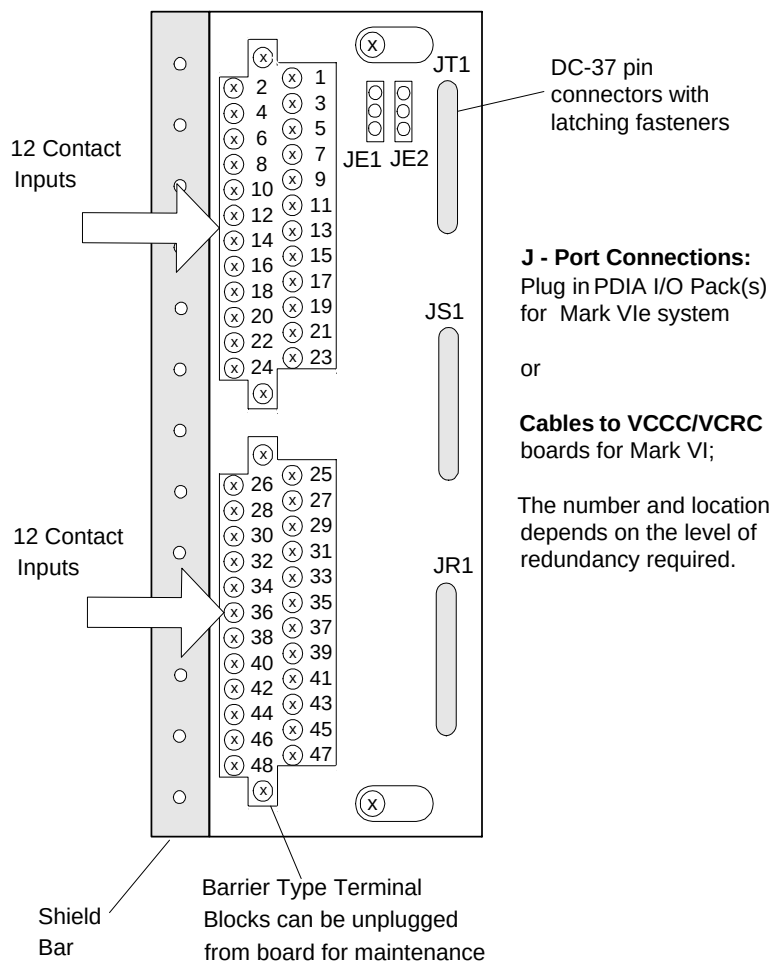
## ***Mark VIe Systems***

In the Mark VIe system, the TBCI works with the PDIA I/O pack and supports simplex, dual, and TMR applications. One, two, or three PDIAs can be plugged directly into the TBCI. Mark VIe requires the C version of this board for correct mechanical alignment of connector JT1 with I/O pack mechanical support.

## ***Board Versions***

Three versions of TBCI are available as follows:

| <b>Terminal Board</b> | <b>Contact Inputs</b> | <b>Excitation Voltage</b>                                |
|-----------------------|-----------------------|----------------------------------------------------------|
| TBCIH1C               | 24                    | Nominal 125 V dc, floating, ranging from 100 to 145 V dc |
| TBCIH2C               | 24                    | Nominal 24 V dc, floating, ranging from 16 to 32 V dc    |
| TBCIH3C               | 24                    | Nominal 48 V dc, floating, ranging from 32 to 64 V dc    |



*TBCI Contact Input Terminal Board*

## Installation

### Wiring

Connect the wires for the 24 dry contact inputs directly to two I/O terminal blocks on the terminal board. These blocks are held down with two screws and can be unplugged from the board for maintenance. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

### Power Connection

Connect TBCI to the contact excitation voltage source using plugs JE1 and JE2, as shown in following figure.

### Cabling Connections

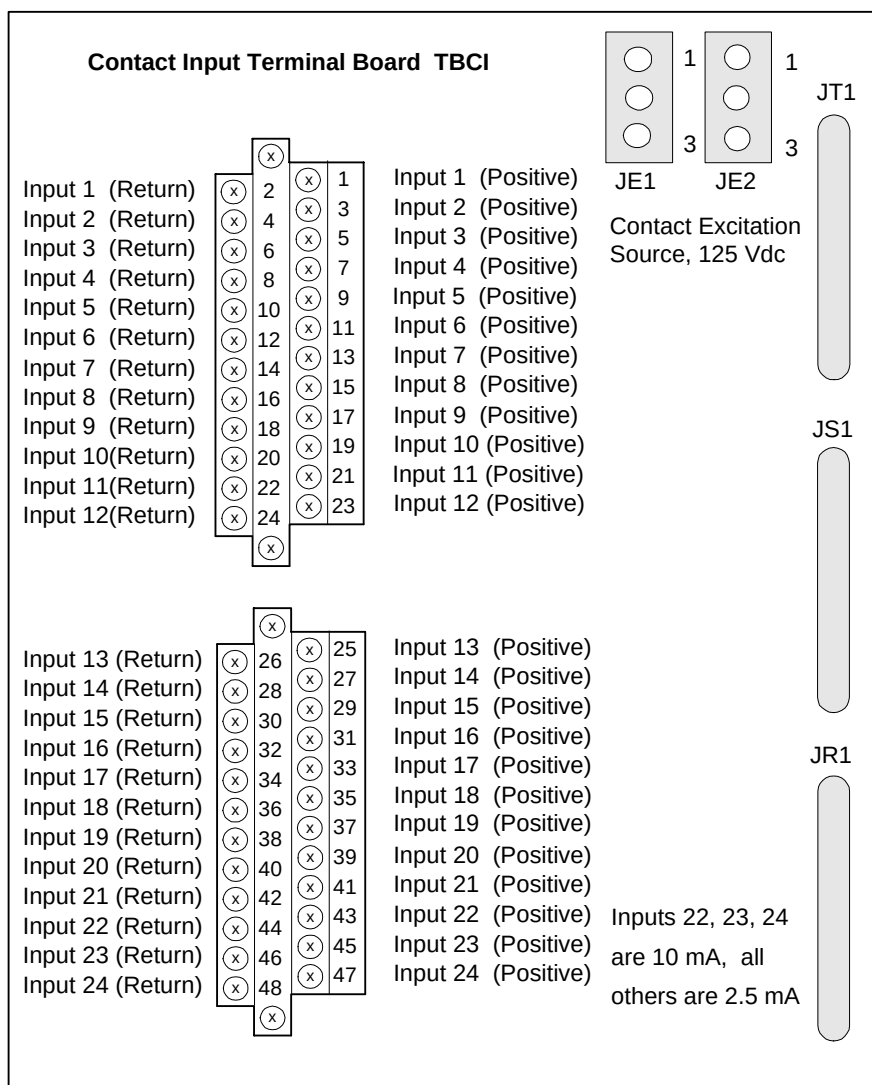
In a simplex system, connect TBCI to the I/O processor using connector JR1. In a TMR system, connect TBCI to the I/O processors using connectors JR1, JS1, and JT1. Cables or I/O packs are plugged in depending on the type of Mark VI or Mark VIe system, and the level of redundancy.

---

**Note** For a Mark VIe system, the I/O packs plug into TBCI and attach to side-mounting brackets. One or two Ethernet cables plug into the pack. Firmware may need to be downloaded. Refer to *GEH-6700, ToolboxST for Mark VIe Control*.

---





#### J - Port Connections:

Plug in PDIA I/O Pack(s) for Mark VIe system

or

**Cables to VCCC/VCRC** boards for Mark VI;

The number and location depends on the level of redundancy required.

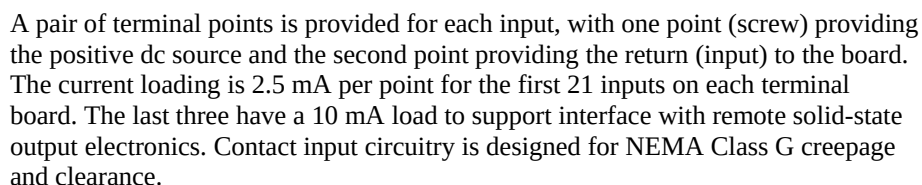
Terminal Blocks can be unplugged from terminal board for maintenance

Up to two #12 AWG wires per point with 300 volt insulation

#### TBCI1C Terminal Board Wiring and Cabling

Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The dry contact inputs on H1 are powered from a floating 125 V dc (100-145 V dc) supply from the turbine control. The 125 V dc bus is current limited in the power distribution module prior to feeding each contact input. H2 and H3 versions use lower voltages as shown in the specification table.

## Terminal Board TBCIH1C



## Specifications

| Item               | Specification                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels | 24 contact voltage input channels                                                                                                                                                                                                                                                                                                                                                  |
| Excitation voltage | H1: Nominal 125 V dc, floating, ranging from 100 to 145 V dc<br>H2: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc<br>H3: Nominal 48 V dc, floating, ranging from 32 to 64 V dc                                                                                                                                                                                           |
| Input current      | H1: For 125 V dc applications:<br>First 21 circuits draw 2.5 mA (50 k $\Omega$ )<br>Last three circuits draw 10 mA (12.5 k $\Omega$ )<br>H2: For 24 V dc applications:<br>First 21 circuits draw 2.5 mA (10 k $\Omega$ )<br>Last three circuits draw 9.9 mA (2.42 k $\Omega$ )<br>H3: For 48 V dc applications:<br>First 21 circuits draw 2.5 mA<br>Last three circuits draw 10 mA |
| Input filter       | Hardware filter, 4 ms                                                                                                                                                                                                                                                                                                                                                              |
| Power consumption  | 20.6 W on the terminal board                                                                                                                                                                                                                                                                                                                                                       |
| Temperature rating | 0 to 60°C (32 to 140 °F)                                                                                                                                                                                                                                                                                                                                                           |
| Fault detection    | Loss of contact input excitation voltage<br>Non-responding contact input in test mode<br>Unplugged cable                                                                                                                                                                                                                                                                           |
| <b>Physical</b>    |                                                                                                                                                                                                                                                                                                                                                                                    |
| Size               | 33.02 cm high x 10.16 cm wide (13.0 in. x 4.0 in)                                                                                                                                                                                                                                                                                                                                  |
| Temperature        | Operating: -30 to 65°C (-22 to 149 °F)                                                                                                                                                                                                                                                                                                                                             |

## Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm is set and latched by the I/O pack/board.
- As a test, all inputs associated with this terminal board are forced to the open contact (fail safe) state. Any input that fails the diagnostic test is forced to the failsafe state and a fault is created.
- If the input from this board does not match the TMR voted value from all three boards, a fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the controller and a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

There are no jumpers or hardware settings on the board.

---

# ***TICI Contact Input with Point Isolation***

## ***Functional Description***

The Contact Input with Point Isolation (TICI) terminal board provides 24 point isolated voltage detection circuits to sense a range of voltages across relay contacts, fuses, and switches.

### ***Mark VI Systems***

In the Mark\* VI system, the TICI is controlled by the VCCC board and supports simplex and TMR applications. Cables with molded plugs connect TICI to the VME rack where the I/O boards are mounted.

---

**Note** The VCRC J3 and J4 front connectors do not support TICI.

---

### ***Mark VIe Systems***

In the Mark VIe system, the TICI works with the PDIA I/O pack and supports simplex, dual, and TMR applications. One, two, or three PDIA's plug into the TICI to support a variety of system configurations.

## ***Installation***

### ***Wiring***

Connect the wires for the 24 isolated digital inputs directly to two I/O terminal blocks on the terminal board. These blocks are held down with two screws and can be unplugged from the board for maintenance. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

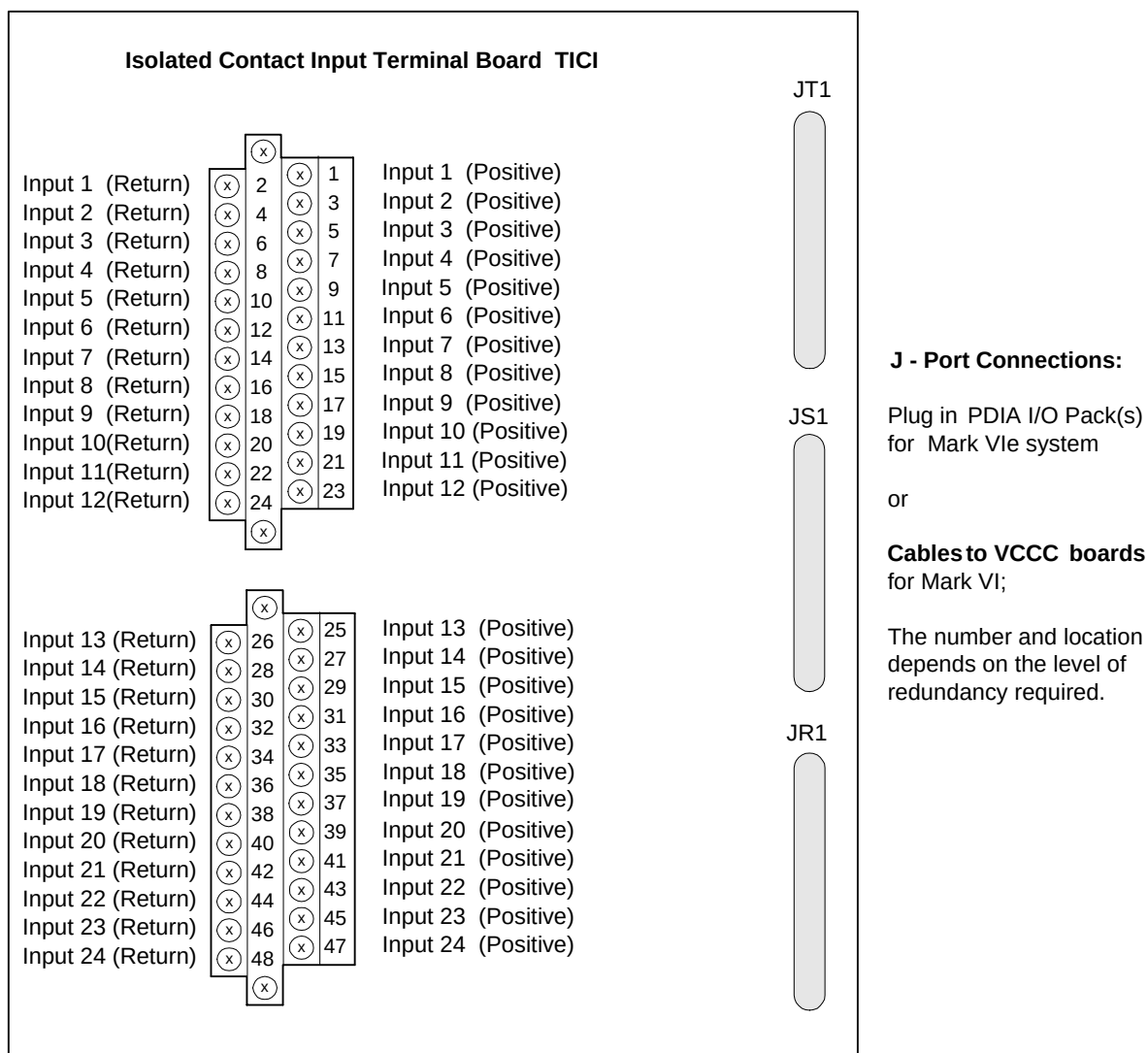
### ***Cabling Connections***

In a simplex system, connect TICI to the I/O processor using connector JR1. In a TMR system, connect TICI to the I/O processors using connectors JR1, JS1, and JT1. Cables or I/O packs are plugged in depending on the type of Mark VI or Mark VIe system, and the level of redundancy.

---

**Note** For a Mark VIe system, the I/O packs plug into TICI and attach to side-mounting brackets. One or two Ethernet cables plug into the pack. Firmware may need to be downloaded.

---



Terminal Blocks can be unplugged from terminal board for maintenance

Up to two #12 AWG wires per point with 300 volt insulation

### *TICI Terminal Board Wiring and Cabling*

## **Operation**

The TICI is similar to TBCI, except for the following items:

- No contact excitation is provided on the terminal board.
- Each input is electrically isolated from all others and from the active electronics.

There are two groups of the TICI with different nominal voltage thresholds. TICI1 has the following input voltage ranges:

- 70-145 V dc, nominal 125 V dc, with a detection of 39 to 61 V dc
- 200-250 V dc, nominal 250 V dc, with a detection of 39 to 61 V dc
- 90-132 V rms, nominal 115 V rms, 47-63 Hz, with a detection of 35 to 76 V ac
- 190-264 V rms, nominal 230 V rms, 47-63 Hz, with a detection of 35 to 76 V ac

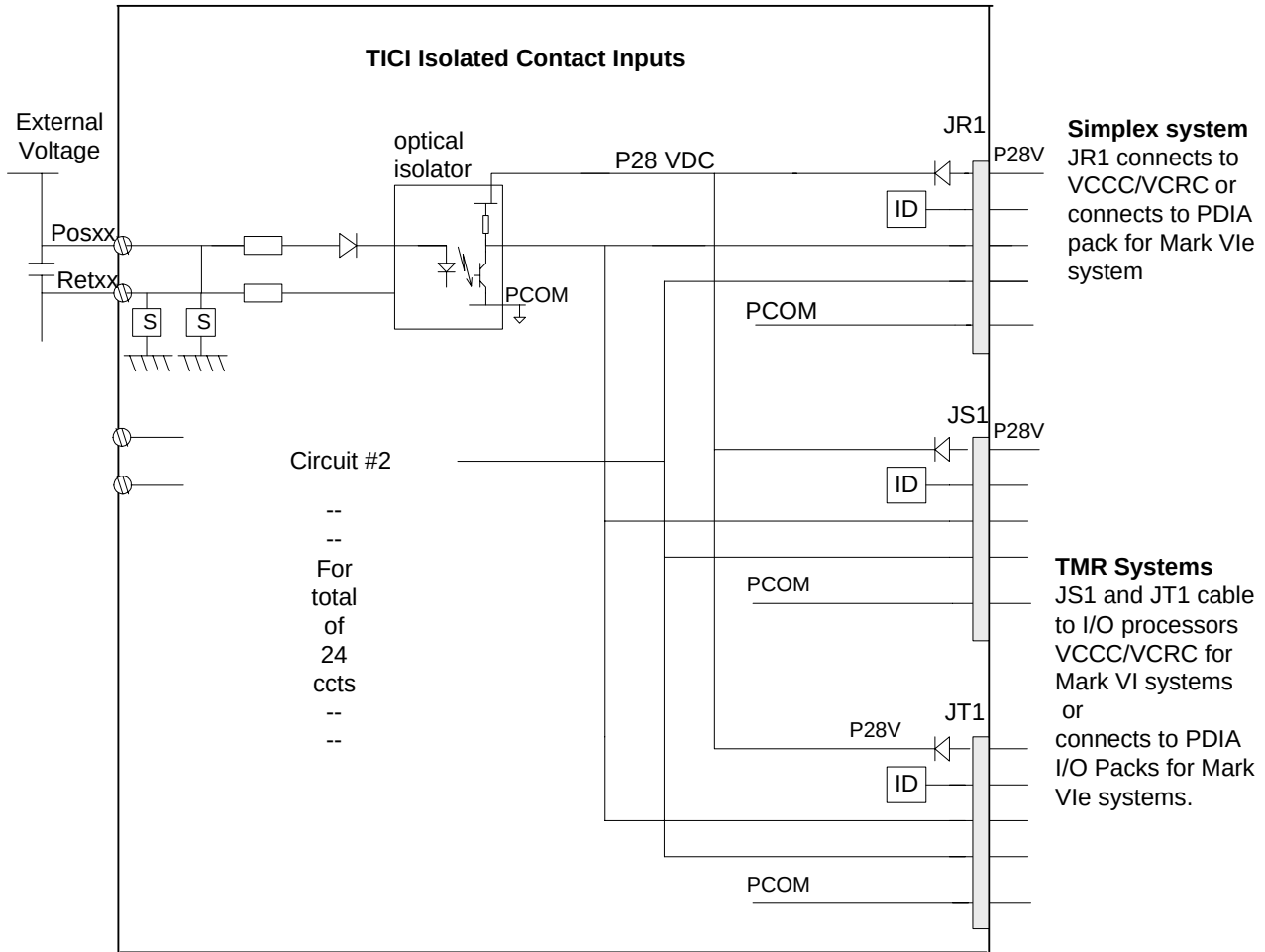
TICIH2 has the following input voltage range:

- 16-32 V dc, nominal 24 V dc, with a detection threshold of 9.5 to 15 V dc

TICI provides input hardware filtering with time delays of 15 ms, nominal:

- For dc applications the time delay is  $15 \pm 8$  ms
- For ac applications the time delay is  $15 \pm 13$  ms

In addition to hardware filters, the contact input state is software-filtered, using configurable time delays selected from 0, 10, 20, 50, and 100 ms. For ac inputs, a filter of at least 10 ms is recommended.



*TICI Circuits for Sensing Voltage across typical device*

The following restrictions should be noted regarding creepage and clearance on the 230 V rms application:

- For NEMA requirements: 230 V single-phase
- For CE Certification: 230 V single or 3-phase

Refer to VCC or PDIO documentation for information on monitoring contact inputs.

## Specifications

| Item                         | Specification                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels           | 24 input channels for isolated voltage sensing                                                                                                                                                                                                                                                                                                                                                                                                       |
| Input voltage                | TICIH2:<br>16-32 V dc, nominal 24 V dc, with a detection threshold of 9.5 to 15 V dc<br>TICIH1:<br>70 -145 V dc, nominal 125 V dc, with a detection threshold of 39 to 61 V dc<br>200 -250 V dc, nominal 250 V dc, with a detection threshold of 39 to 61 V dc<br>90 -132 V rms, nominal 115 V rms, 47-63 Hz, with a detection threshold of 35 to 76 V ac<br>190-264 V rms, nominal 230 V rms, 47-63 Hz, with a detection threshold of 35 to 76 V ac |
| Fault detection in I/O board | Non-responding contact input in test mode<br>Unplugged cable or failed ID chip                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Physical</b>              |                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Size                         | 17.8 cm high x 33.02 cm wide (7.0 in. x 13.0 in.)                                                                                                                                                                                                                                                                                                                                                                                                    |
| Temperature                  | Operating -30 to +65°C (-22 to +149 °F)                                                                                                                                                                                                                                                                                                                                                                                                              |

## Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm is set and latched by the I/O pack/board.
- As a test, all inputs associated with this terminal board are forced to the open contact (fail safe) state. Any input that fails the diagnostic test is forced to the failsafe state and a fault is created.
- If the input from this board does not match the TMR voted value from all three boards, a fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the controller and a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

There are no jumpers or hardware settings on the board.

---

# STCI Simplex Contact Input

## Functional Description

The Simplex Contact Input (STCI) terminal board is a compact contact input terminal board designed for DIN-rail or flat mounting. The STCI board accepts 24 contact inputs that are supplied with a nominal 24, 48, and 125 V dc excitation from an external source. The contact inputs have noise suppression to protect against surge and high-frequency noise. The STCI works with Mark\* Vle systems.

## Mark Vle Systems

In the Mark Vle systems, the PDIA I/O pack works with the STCI. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet. Only simplex systems are supported.

## Board Versions

Four versions of STCI are available as follows:

| Terminal Board | Contact Inputs | TB Type   | Excitation Voltage                                       |
|----------------|----------------|-----------|----------------------------------------------------------|
| STCIH1A        | 24             | Fixed     | Nominal 24 V dc, floating, ranging from 16 to 32 V dc    |
| STCIH2A        | 24             | Pluggable | Nominal 24 V dc, floating, ranging from 16 to 32 V dc    |
| STCIH4A        | 24             | Pluggable | Nominal 48 V dc, floating, ranging from 32 to 64 V dc    |
| STCIH6A        | 24             | Pluggable | Nominal 125 V dc, floating, ranging from 100 to 145 V dc |

## Installation

The STCI plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN rail. Optionally the STCI plus insulator mounts on a sheet metal assembly that then bolts in a cabinet. The contact inputs are wired directly to the terminal block, typically using #18 AWG wires. Shields should be terminated on a separate bracket.

---

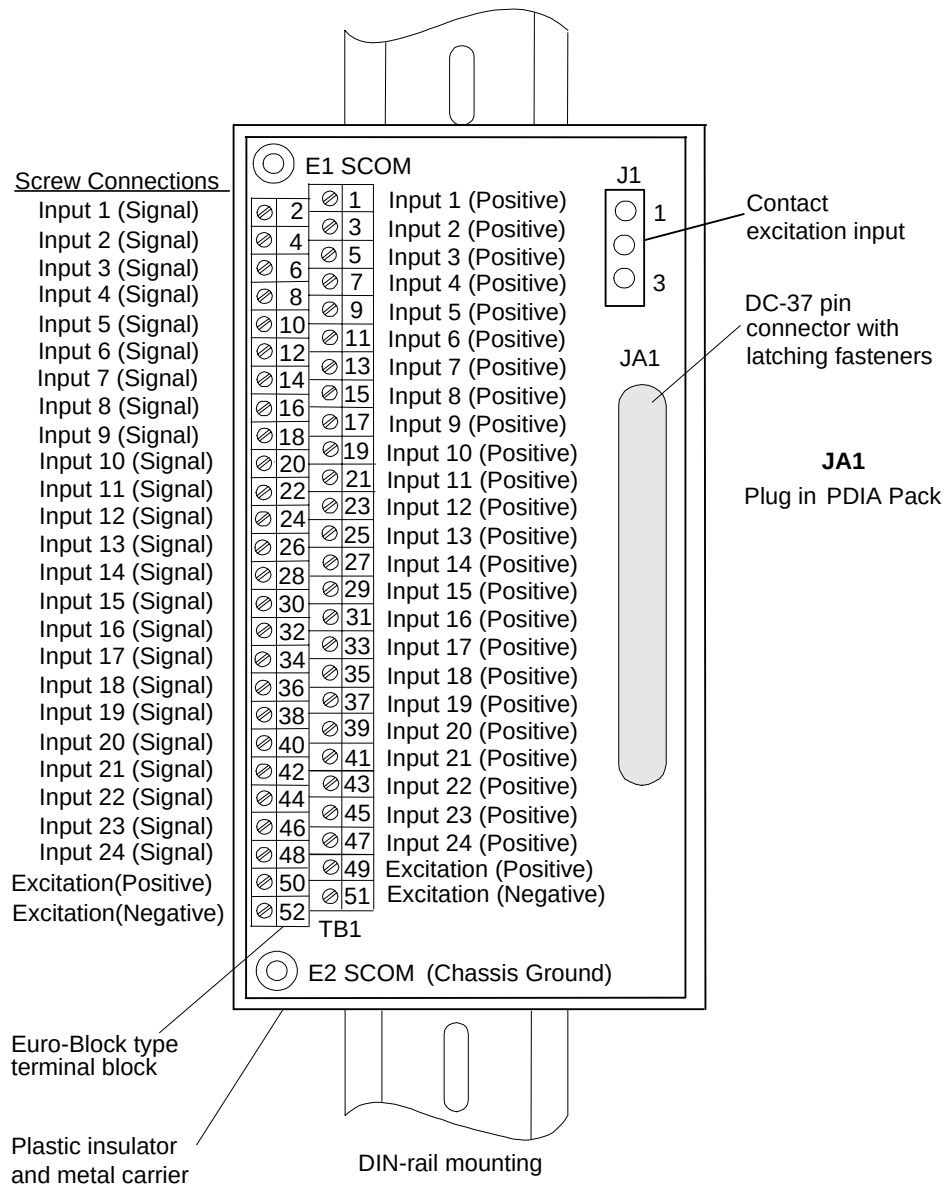
**Note** E1 and E2 are chassis grounding screws for SCOM.

---



Two types of Euro-block terminal blocks are available:

- STCIH1 has a permanently mounted terminal block with 52 terminals
- STCIH2, STCIH4, and STCIH6 has a right-angle header accepting a range of commercially available pluggable terminal blocks, with a total of 52 terminals

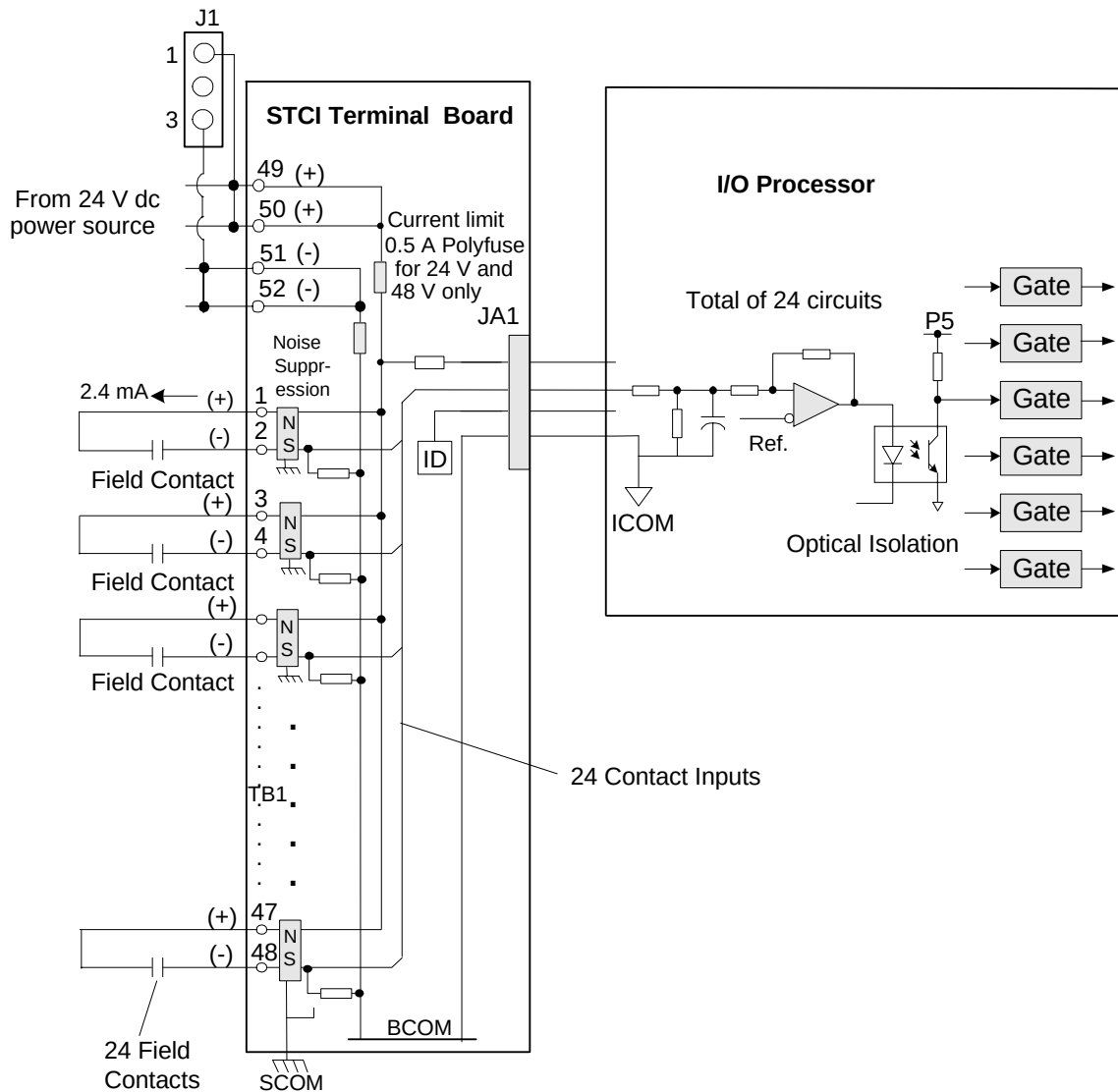


Wiring to STCI Terminal Board

## Operation

The function and on-board signal conditioning are the same as those on TBCI, they are scaled for 24, 48, and 125 V dc excitation. The input excitation range is 16 to 32 V dc, 32 to 64 V dc, and 100 to 145 V dc respectively. The threshold voltage is 50% of the excitation voltage. The contact sensing circuits are shown in the figure. Contact input currents are resistance limited to 2.5 mA on the first 21 circuits, and 10 mA on circuits 22 through 24. The 24 V dc supply is current limited to 0.5 A using polymer positive temperature coefficient fuses that can be reset.

Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The discrete input voltage signals go to the I/O processor which passes them through optical isolators, converts them to digital signals, and transfers them to the controller.



STCI Contact Input Circuits

## ***Specifications***

| <b>Item</b>                  | <b>Specification</b>                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels           | 24 dry contact voltage input channels                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Excitation voltage           | H1: Nominal 24 V dc, floating, ranging from 18 to 32 V dc (Fixed TB)<br>H2: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc (Pluggable TB)<br>H4: Nominal 48 V dc, floating, ranging from 32 to 64 V dc (Pluggable TB)<br>H6: Nominal 125 V dc, floating, ranging from 100 to 145 V dc (Pluggable TB)                                                                                                                                                  |
| Input current                | H1: For 24 V dc applications:<br>First 21 circuits each draw 2.5 mA (50 k $\Omega$ )<br>Last three circuits each draw 10 mA (12.5 k $\Omega$ )<br>H2: For 24 V dc applications:<br>First 21 circuits draw 2.5 mA<br>Last three circuits draw 10 mA<br>H4: For 48 V dc applications:<br>First 21 circuits draw 2.5 mA<br>Last three circuits draw 10.4 mA<br>H6: For 125 V dc applications:<br>First 21 circuits draw 2.55 mA<br>Last three circuits draw 10 mA |
| Input filter                 | Hardware filter, 4 ms                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Fault detection in I/O board | Loss of contact input excitation voltage<br>Non-responding contact input in test mode                                                                                                                                                                                                                                                                                                                                                                          |
| AC voltage rejection         | 12 V rms at 24 V dc excitation. (H1 & H2)<br>24 V rms at 48 V dc excitation. (H4)<br>60 V rms at 125 V dc excitation. (H6)                                                                                                                                                                                                                                                                                                                                     |
| <b>Physical</b>              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Size                         | 15.9 cm high x 10.2 cm wide (6.25 in. x 4.0 in)                                                                                                                                                                                                                                                                                                                                                                                                                |
| Temperature                  | -30 to + 65°C (-22 to 149 °F)                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Technology                   | Surface-mount                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

## ***Diagnostics***

The I/O processor monitors the following functions on STCI:

- The contact excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm (fault) is set and latched.
- As a test, all inputs associated with this terminal board are forced to the open contact state. Any input that fails the diagnostic test is forced to the failsafe state (open) and a fault is created.
- The terminal board connector has an ID device that is interrogated by the I/O processor. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. If a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no jumpers or hardware settings on the board.

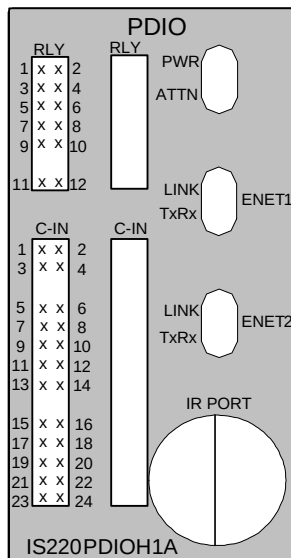
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## ***Notes***

# PDIO Discrete Input/Output

## PDIO Discrete Input/Output

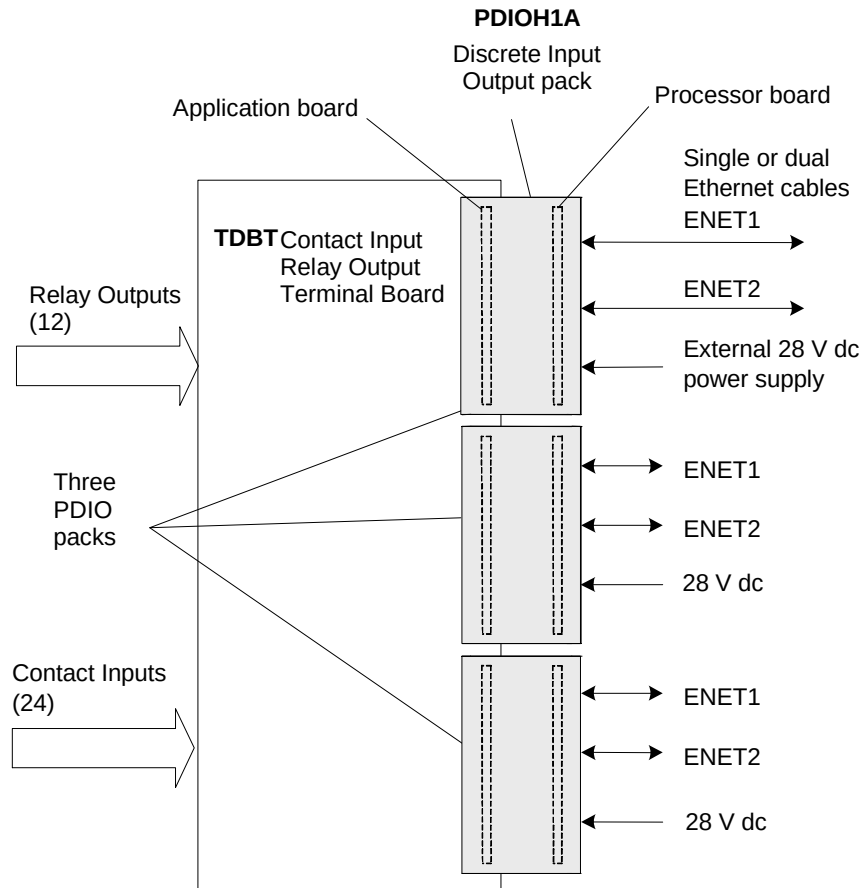
### Functional Description



The Discrete Input/Output (PDIO) pack provides the electrical interface between one or two I/O Ethernet networks and a discrete input/output terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs and an acquisition board specific to the discrete input/output function. The pack accepts up to 24 contact inputs, controls up to 12 relay outputs, and receives terminal board specific feedback signals. The associated terminal board determines voltage capability of PDIO. System input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Discrete signal input/output is through a DC-62 connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.

PDIO is the functional equivalent of a PDIA and PDOA I/O pack combined into a single assembly. For simplex applications, it goes on a TDBS terminal board that is the equivalent of a SRLY relay terminal board combined with a STCI contact input terminal board. For TMR applications, it goes on a TDBT terminal board that, with the WROB option, provides the equivalent of a TRLYH1B relay terminal board combined with a TBCI contact input terminal board.

The following illustration shows the connections when three PDIO packs are mounted on a TDBT terminal board.



## Compatibility

PDIOH1A is compatible with two types of discrete contact input/output terminal boards: TDBS for single PDIO applications and TDBT for TMR PDIO applications. The relay output portion of the terminal board accepts option cards as described later in this document. The following table gives details of the compatibility:

| Terminal Board | Control Mode | DI Voltage | DO Option Cards  |
|----------------|--------------|------------|------------------|
| TDBSH2         | Simplex      | 24 V dc    | WROB, WROF, WROG |
| TDBSH4         | Simplex      | 48 V dc    | WROB, WROF, WROG |
| TDBSH6         | Simplex      | 125 V dc   | WROB, WROF, WROG |
| TDBTH2         | TMR          | 24 V dc    | WROB             |
| TDBTH4         | TMR          | 48 V dc    | WROB             |
| TDBTH6         | TMR          | 125 V dc   | WROB             |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

## Installation

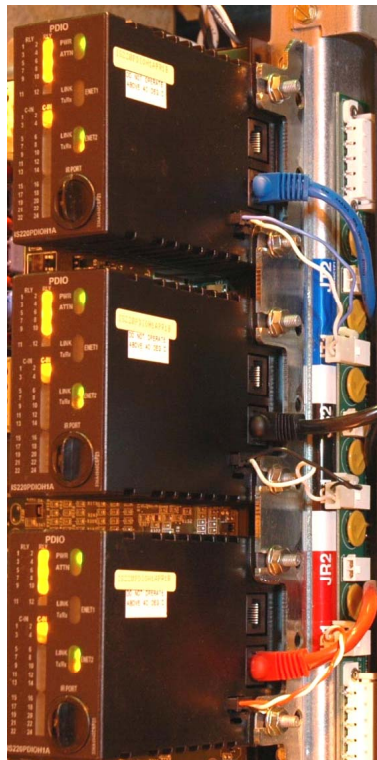
### ➤ To install the PDIO pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PDIO I/O pack for simplex or three PDIO I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

---

**Note** The PDIO mounts directly on a Mark VIe terminal board. Simplex terminal boards have a single DC-62 pin connector that receives the PDIO. TMR-capable terminal boards have three DC-62 pin connectors, one used for simplex operation, two for dual operation, and three for TMR operation. PDIO directly supports all of these connections.

---



# Operation

## Processor

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

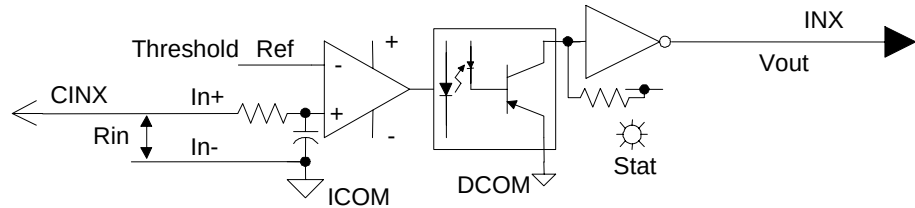
The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).



## Contact Input Signals

The discrete input/output acquisition board provides the second stage of signal conditioning and level shifting to interface the terminal board inputs to the control logic. Initial signal conditioning is provided on the terminal board. The discrete input acquisition input circuit is a comparator with a variable threshold. Each input is isolated from the control logic through an opto-coupler and an isolated power supply. The inputs are not isolated from each other. Each of the twenty-four inputs has filtering, hysteresis, and a yellow status LED, that indicates when an input is picked up. The LED will be OFF when the input is dropped-out. The LEDs are grouped at the bottom left of the PDIO pack.

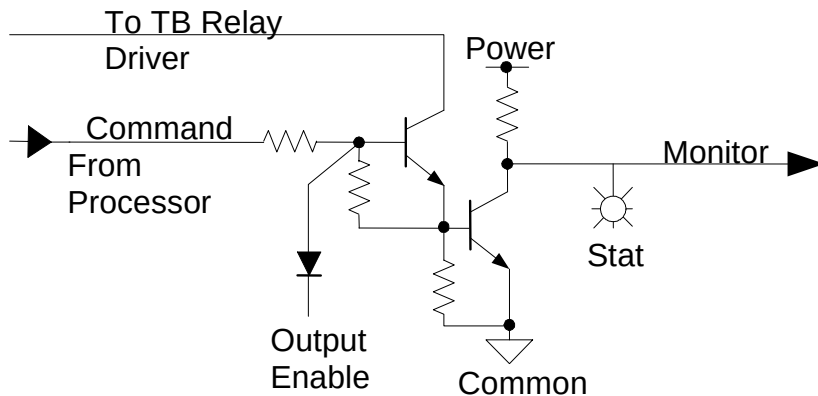


## Variable Input Threshold

The input threshold is derived from the contact wetting voltage input terminal. In most applications this voltage is scaled to provide a 50% input threshold. This threshold is clamped to 13% to prevent an indeterminate state if the contact wetting voltage drops to zero. If the contact wetting voltage drops below 40% of the nominal voltage, the under-voltage detector annunciates this condition to the control. A special test mode is provided to force the inputs from the control pack. Every four seconds, the threshold is pulsed high and then low and the response of the opto-couplers is checked. Non-responding inputs are alarmed.

## Relay Command Signals

The PDIO relay command signals are the first stage of signal conditioning and level shifting to interface the terminal board outputs to the control logic. Each output is an open collector transistor circuit with a current monitor to sense when the output is picked up and connected to a load. The status LEDs and monitor outputs indicate when an output is picked up and connected to the terminal board. If an output is commanded to be picked up and the correct load is not sensed, the status LED will be off and the monitor line will be false. The LEDs are grouped at the top left of the PDIO pack.



Relay Command Signals

## ***Output Enable***

All of the outputs are disabled during power application until a variety of internal self-tests are completed. An enable line reflects the status of all required conditions for operation. This function provides a path independent of the command to ensure relays stay dropped-out during power-up and initialization.

## ***Monitor Inputs/Control***

There are 15 inverting level shifting monitor input circuits. On a typical terminal board 12 of these circuits are used as relay contact feedbacks and the other three are used for fuse status. An inverting level shifting line is also provided from the control to the terminal board for status feedback multiplexing control allowing the pack to receive two sets of 15 signals from a terminal board.

## ***Sequence Of Events***

All of the inputs and outputs may be individually configured to generate SOE records when the signal changes. Input hardware is scanned at a 1000 Hz rate for SOE time stamping while output commands are captured when a change of command is received through Ethernet from the controller.

## ***ID Line***

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-62 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## ***Power Management***

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Connectors

The pack contains the following connectors:

- A DC-62 pin connector on the underside of the PDIO pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

## Specifications

| Item                             | Specification                                                                                                   |
|----------------------------------|-----------------------------------------------------------------------------------------------------------------|
| Number of input channels         | 24 dry contact voltage input channels                                                                           |
| Input isolation in pack          | Optical isolation to 1500 V on all inputs (group isolation)                                                     |
| Input Filter                     | Hardware filter, 4 ms                                                                                           |
| Ac voltage rejection             | 60 V r ms @ 50/60 Hz at 125 V dc wetting voltage                                                                |
| Number of relay command channels | 12 relays                                                                                                       |
| Relay and coil monitoring        | 15 pack inputs. The selection of monitor feedbacks depends on the type of terminal board used, based on ID chip |
| I/O pack response time           | From Ethernet command to output is typically 4 ms.                                                              |
| SOE reporting                    | Each relay may be configured to report operation in the sequence of events (SOE) record.                        |
| Frame rate                       | System dependent scan rate for control purposes<br>1,000 Hz scan rate for sequence of events monitoring         |
| Fault detection                  | Loss of contact input wetting voltage<br>Non-responding contact input in test mode<br>Incorrect terminal board  |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A powerup self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware.
- Continuous monitoring of the internal power supplies for correct operation.
- A powerup check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- Monitoring for loss of contact input wetting voltage on the terminal board takes place at the selected system frame rate.
- Detecting a non-responding contact input during diagnostic test. In this test, the threshold is pulsed high and low and the response of the opto-couplers is checked. The test typically runs once every four seconds, and can be observed as a very brief period when all twenty-four contact input lights turn on.
- A frame rate comparison is made between the commanded state of each relay drive and the feedback from the command output circuit.
- Relay board specific feedback is read by the pack and processed every frame. The information varies depending on the relay board type. Refer to relay terminal board documentation for feedback specifics.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter                     | Description                                                                                | Choices                                  |
|-------------------------------|--------------------------------------------------------------------------------------------|------------------------------------------|
| <b>PDIO_Mod_Configuration</b> |                                                                                            |                                          |
| Redundancy                    | Redundancy mode of the pack                                                                | Simplex, TMR                             |
| <b>PDIO_Input</b>             | Terminal board connected to PDIO                                                           | Connected, not connected                 |
| Relay Feedback                | Selection will enable Relay feedback inputs                                                | Used, Unused                             |
| Contact Input                 | Selection will enable Contact Input feedbacks                                              | Used, Unused                             |
| Signal Invert                 | Inversion makes signal true if contact is open                                             | Normal, Invert                           |
| Sequence of Events            | Record contact transitions in sequence of events                                           | Enable, disable                          |
| Diag Vote Enable              | Enable voting disagreement diagnostic                                                      | Enable, disable                          |
| Signal Filter                 | Contact input digital filter in msec (in addition to 4 ms hardware filter)                 | 0, 10, 20, 50, 100                       |
| <b>PDIO_Output</b>            |                                                                                            |                                          |
| Relay Output                  | Selection will enable use of the relay                                                     | Used, Unused                             |
| Signal Invert                 | Inversion makes relay closed if signal is false                                            | Normal, Invert                           |
| SeqOfEvents                   | Record relay command transitions in sequence of events                                     | Enable, Disable                          |
| FuseDiag                      | Enable fuse diagnostic - Will appear as configuration item for use with Fuse daughterboard | Enable, Disable                          |
| Output_State                  | Select the state of the Relay condition based on IOPack going offline with controller      | PwrDownMode, HoldLastValue, Output_Value |

# Alarms

## PDIO Specific Alarms

| Alarm ID  | Alarm Description                                       | Possible Cause                                                                                                                                           | Solution |
|-----------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 34-45     | Fuse [ ] blown                                          | Indicates a Fuse blown                                                                                                                                   |          |
| 46        | All Fuses Blown or No Terminal Board Excitation         | Either indicates that all the fuses are blown or the Terminal board Excitation has failed or not been provided.                                          |          |
| 47-58     | Relay Coil [ ] Failure                                  | Mismatch between the terminal board Relay feedback and the Relay command. Indicates a Relay Failure                                                      |          |
| 59-70     | Relay Output Driver [ ] Failure                         | Mismatch between the Relay command signal and the Acquisition card's Re-Input of the Signal.                                                             |          |
| 72-95     | Contact Input [ ] not responding to high self-test mode | Normally a PDIO problem, or the battery reference voltage is missing to the terminal board.                                                              |          |
| 96-119    | Contact Input [ ] not responding to low self-test mode  | Normally a PDIO problem, or the battery reference voltage is missing to the terminal board.                                                              |          |
| 120       | Excitation Voltage not valid, Contact Inputs not valid  | The contact input terminal board may not exist, or the contact excitation may not be on, or be unplugged, or the excitation may be below required levels |          |
| 1082-1210 | Logic Signal [ ] Voting Mismatch                        | Voter disagreement between the R, S and T IO Packs                                                                                                       |          |

## I/O Pack Alarms

| Fault | Fault Description                                         | Possible Cause                                                                                                                                            |
|-------|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                  | Board firmware programming error (board will not go online)                                                                                               |
| 3     | CRC failure override is active                            | Board firmware programming error (board is allowed to go online)                                                                                          |
| 4     | I/O pack in stand alone mode                              | Invalid command line option                                                                                                                               |
| 5     | I/O pack in remote I/O mode                               | Invalid command line option                                                                                                                               |
| 6     | Special user mode active. Now [ ]                         | Invalid command line option                                                                                                                               |
| 7     | I/O pack – The I/O pack has gone to the offline state     | Lost communication with controller                                                                                                                        |
| 16    | System limit checking is disabled                         | System checking was disabled by configuration                                                                                                             |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                  | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                      | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                | Supply voltage below 26.5 V dc                                                                                                                            |
| 257   | I/O pack power supply voltage is low                      | Supply voltage below 18 V dc                                                                                                                              |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                |
| 261   | Unable to read configuration file from flash              | Need to download configuration to the pack                                                                                                                |
| 262   | Bad configuration file detected                           | Configuration file not compatible, re-download                                                                                                            |
| 263   | I/O pack configuration – bad name detected                | Wrong configuration file for I/O pack                                                                                                                     |
| 264   | I/O pack configuration – bad config compatibility code    | Wrong configuration revision for I/O pack                                                                                                                 |

| <b>Fault</b> | <b>Fault Description</b>                                                    | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 265          | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                              |
| 266          | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                              |
| 267          | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                |
| 268          | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                         |
| 269          | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                   |
| 270          | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                |
| 271          | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                        |
| 272          | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                           |
| 273          | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                            |
| 274          | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                    |
| 275          | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                            |
| 276          | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                |
| 277          | IONet-EGD – Signature mismatch E_Id= [ ]P_Id= [ ], =Expctd= [ ], Rcvd= [ ]  | Message version mismatch                                                                |
| 278          | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                           |
| 293          | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                             |
| 301          | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                |
| 314          | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                           |
| 315          | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                             |
| 316          | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected         |
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ]             | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                                   | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated                           | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                             | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch                          | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                             | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                                    | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                                  | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                             | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                               | Config Shmem CRC changed                                                                |

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# ***TDBS Simplex Discrete Input/Output***

## ***Functional Description***

The Simplex Discrete Input/Output (TDBS) terminal board is a simplex contact input/output terminal board designed for DIN-rail or flat mounting. The TDBS board accepts 24 group isolated contact inputs that are supplied with a nominal 24, 48, or 125 V dc wetting voltage from an external source. The contact inputs have noise suppression to protect against surge and high-frequency noise. TDBS provides 12 form-C relay outputs and accepts different option cards to expand relay functions.

## ***Mark VIe Systems***

In the Mark\* VIe systems, the PDIO I/O pack works with the TDBS. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet. A single connection point for PDIO is provided with one or two network connections possible from PDIO to the controllers.

## ***Board Versions***

Three versions of TDBS are available as follows:

| <b>Terminal Board</b> | <b>Contact Inputs</b> | <b>TB Type</b> | <b>Wetting Voltage</b>                                   |
|-----------------------|-----------------------|----------------|----------------------------------------------------------|
| TDBSH2A               | 24                    | Pluggable      | Nominal 24 V dc, floating, ranging from 16 to 32 V dc    |
| TDBSH4A               | 24                    | Pluggable      | Nominal 48 V dc, floating, ranging from 32 to 64 V dc    |
| TDBSH6A               | 24                    | Pluggable      | Nominal 125 V dc, floating, ranging from 100 to 145 V dc |

There are three option boards available that plug on to TDBS:

- IS200WROB turns the relay portion of TDBS into the functional equivalent of IS200TRL YH1B. This option provides fused and sensed power distribution to the first six relay outputs and dedicated power to the last relay output.
- IS200WROF puts a single fuse in series with each relay common connection. Fuse voltage feedback is included.
- IS200WROG distributes power from an input connector to each relay through a single fuse. Fuse voltage feedback is included.

## ***Installation***

The TDBS plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN rail. Optionally the TDBS plus insulator mounts on a sheet metal assembly that then bolts in a cabinet. The connections are wired directly to two sets of 48 point terminal blocks, typically using #18 AWG wires. The upper set of terminals, TB1, connects to the relay portion of the board and the lower set of terminals, TB2, connect to the contact input circuits. Shields should be terminated on a separate bracket.

If a relay option board is used, it plugs onto TDBS connectors JW1 and JW2 and is held in place by the force of the connectors. The following table identifies the function of each relay terminal point grouped as TB1 as it relates to the presence of an option board. If external power is to be supplied it is wired to a connector provided on the option board.

- NC - normally closed contact of a form C relay
- COM - common point of a form C relay contact
- NO - normally open contact of a form C relay
- SOL - return circuit path for a solenoid that is powered by the relay board
- VSENSE - the input to a voltage sensor that looks between VSENSE and COM
- RETURN - return power path for devices powered by the WROG option

| Output Terminal | Relay | TDBS | TDBS + WROB | TDBS/WROF with Fuses | TDBS/WROF without Fuses | TDBS + WROG |
|-----------------|-------|------|-------------|----------------------|-------------------------|-------------|
| 1               | 1     | NC   | NC          | NC                   | NC                      | NC          |
| 2               |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 3               |       | NO   | NO          | NO                   | NO                      | NO          |
| 4               |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 5               | 2     | NC   | NC          | NC                   | NC                      | NC          |
| 6               |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 7               |       | NO   | NO          | NO                   | NO                      | NO          |
| 8               |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 9               | 3     | NC   | NC          | NC                   | NC                      | NC          |
| 10              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 11              |       | NO   | NO          | NO                   | NO                      | NO          |
| 12              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 13              | 4     | NC   | NC          | NC                   | NC                      | NC          |
| 14              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 15              |       | NO   | NO          | NO                   | NO                      | NO          |
| 16              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 17              | 5     | NC   | NC          | NC                   | NC                      | NC          |
| 18              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 19              |       | NO   | NO          | NO                   | NO                      | NO          |
| 20              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 21              | 6     | NC   | NC          | NC                   | NC                      | NC          |
| 22              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 23              |       | NO   | NO          | NO                   | NO                      | NO          |
| 24              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 25              | 7     | NC   | NC          | NC                   | NC                      | NC          |
| 26              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 27              |       | NO   | NO          | NO                   | NO                      | NO          |
| 28              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 29              | 8     | NC   | NC          | NC                   | NC                      | NC          |
| 30              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 31              |       | NO   | NO          | NO                   | NO                      | NO          |
| 32              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 33              | 9     | NC   | NC          | NC                   | NC                      | NC          |
| 34              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |

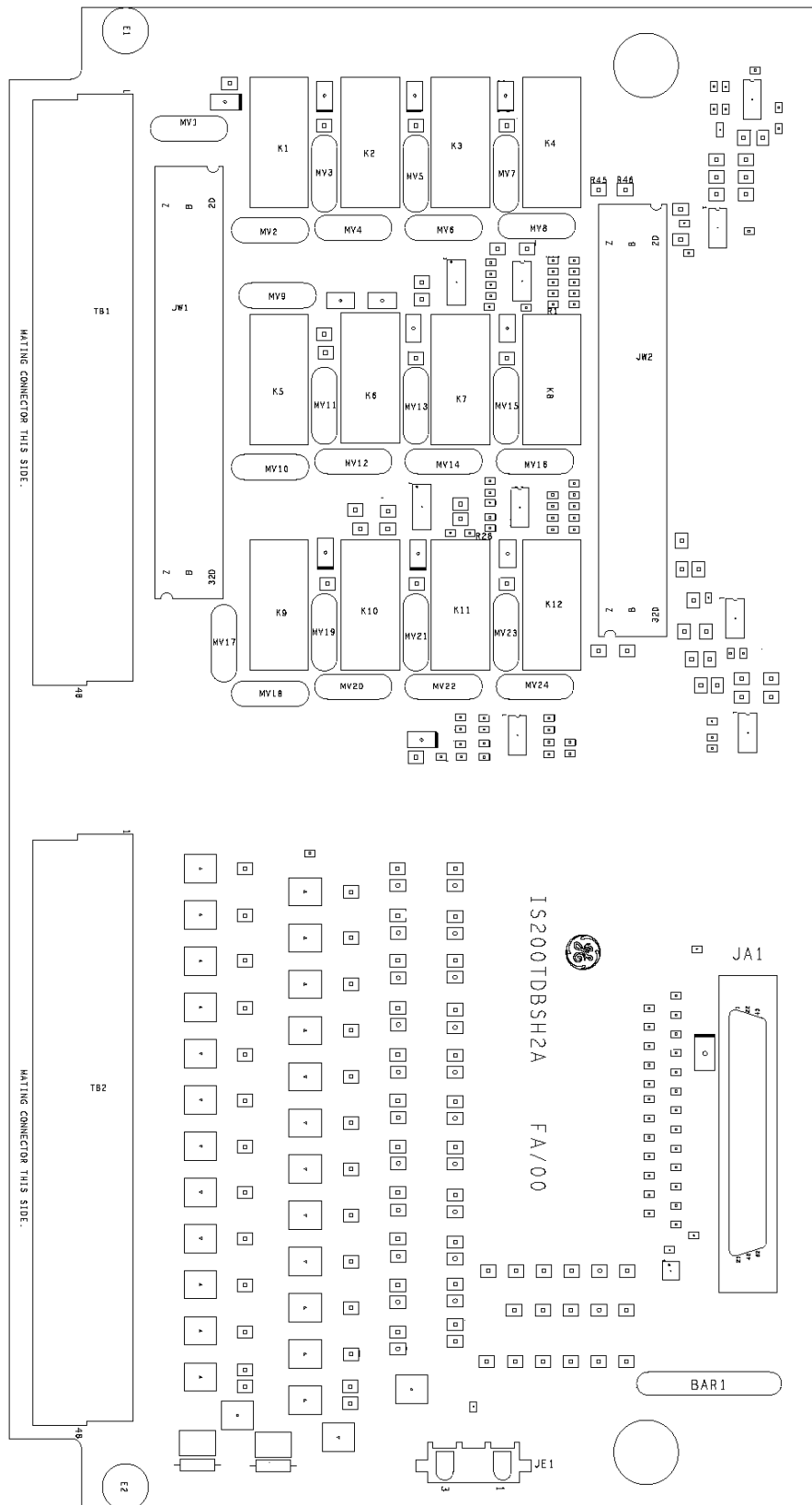


| Output Terminal | Relay | TDBS | TDBS + WROB | TDBS/WROF with Fuses | TDBS/WROF without Fuses | TDBS + WROG |
|-----------------|-------|------|-------------|----------------------|-------------------------|-------------|
| 35              |       | NO   | NO          | NO                   | NO                      | NO          |
| 36              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 37              | 10    | NC   | NC          | NC                   | NC                      | NC          |
| 38              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 39              |       | NO   | NO          | NO                   | NO                      | NO          |
| 40              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 41              | 11    | NC   | NC          | NC                   | NC                      | NC          |
| 42              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 43              |       | NO   | NO          | NO                   | NO                      | NO          |
| 44              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 45              | 12    | NC   | NC          | NC                   | NC                      | NC          |
| 46              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 47              |       | NO   | NO          | NO                   | NO                      | NO          |
| 48              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |

Contact input connections are made to the 48 terminals on the lower portion of the terminal board, grouped as TB2. Contact wetting voltage is provided to the board through the JE1 3-pin Mate-N-Lok<sup>®</sup> connector on the lower portion of the board.

| Terminal | Signal | Terminal | Signal |
|----------|--------|----------|--------|
| 1        | Wet 1  | 25       | Wet 13 |
| 2        | In 1   | 26       | In 13  |
| 3        | Wet 2  | 27       | Wet 14 |
| 4        | In 2   | 28       | In 14  |
| 5        | Wet 3  | 29       | Wet 15 |
| 6        | In 3   | 30       | In 15  |
| 7        | Wet 4  | 31       | Wet 16 |
| 8        | In 4   | 32       | In 16  |
| 9        | Wet 5  | 33       | Wet 17 |
| 10       | In 5   | 34       | In 17  |
| 11       | Wet 6  | 35       | Wet 18 |
| 12       | In 6   | 36       | In 18  |
| 13       | Wet 7  | 37       | Wet 19 |
| 14       | In 7   | 38       | In 19  |
| 15       | Wet 8  | 39       | Wet 20 |
| 16       | In 8   | 40       | In 20  |
| 17       | Wet 9  | 41       | Wet 21 |
| 18       | In 9   | 42       | In 21  |
| 19       | Wet 10 | 43       | Wet 22 |
| 20       | In 10  | 44       | In 22  |
| 21       | Wet 11 | 45       | Wet 23 |
| 22       | In 11  | 46       | In 23  |
| 23       | Wet 12 | 47       | Wet 24 |
| 24       | In 12  | 48       | In 24  |

The wetting voltage output terminals are all connected in parallel and fed from the positive voltage applied to JE1 pin 1. It is permissible to run a single wetting voltage lead from the board terminal to a group of remote contacts and then bring the individual contact wires back to the inputs. Negative or return wetting voltage is supplied by JE1 pin 3.



TDBS Layout

## Operation

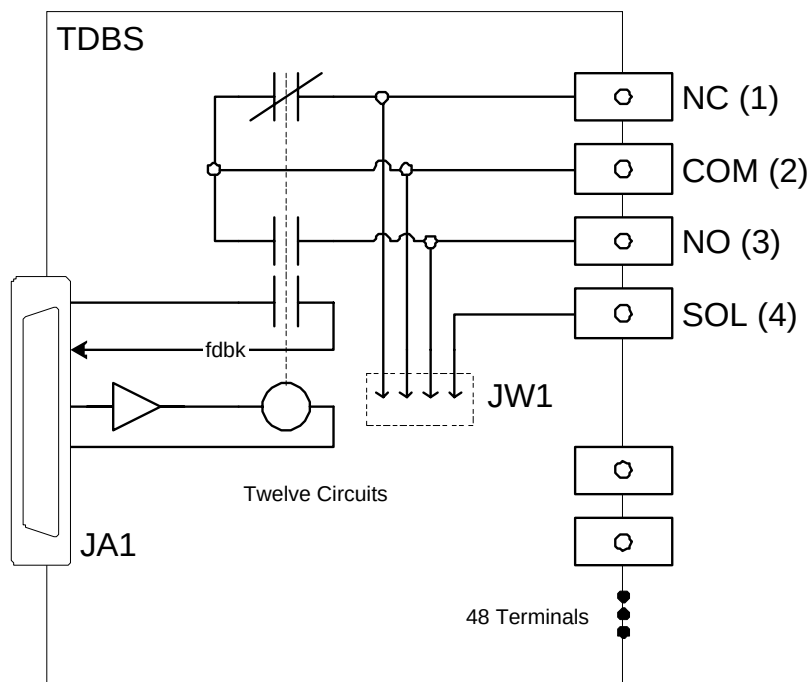
### Contact Inputs

The contact input function and on-board signal conditioning are scaled for 24, 48, and 125 V dc wetting voltage. The input wetting voltage range is 16 to 32 V dc, 32 to 64 V dc, and 100 to 145 V dc respectively. The threshold voltage is 50% of the wetting voltage. The contact sensing circuits are shown in the I/O pack description. Contact input currents are resistance limited to 2.5 mA on the first 21 circuits, and 10 mA on circuits 22 through 24. The 24 V dc supply on TDBSH2 is current limited to 0.5 A using polymer positive temperature coefficient fuses that can be reset.

Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The discrete input voltage signals go to the I/O processor which passes them through optical isolators, converts them to digital signals, and transfers them to the controller.

### Relay Outputs

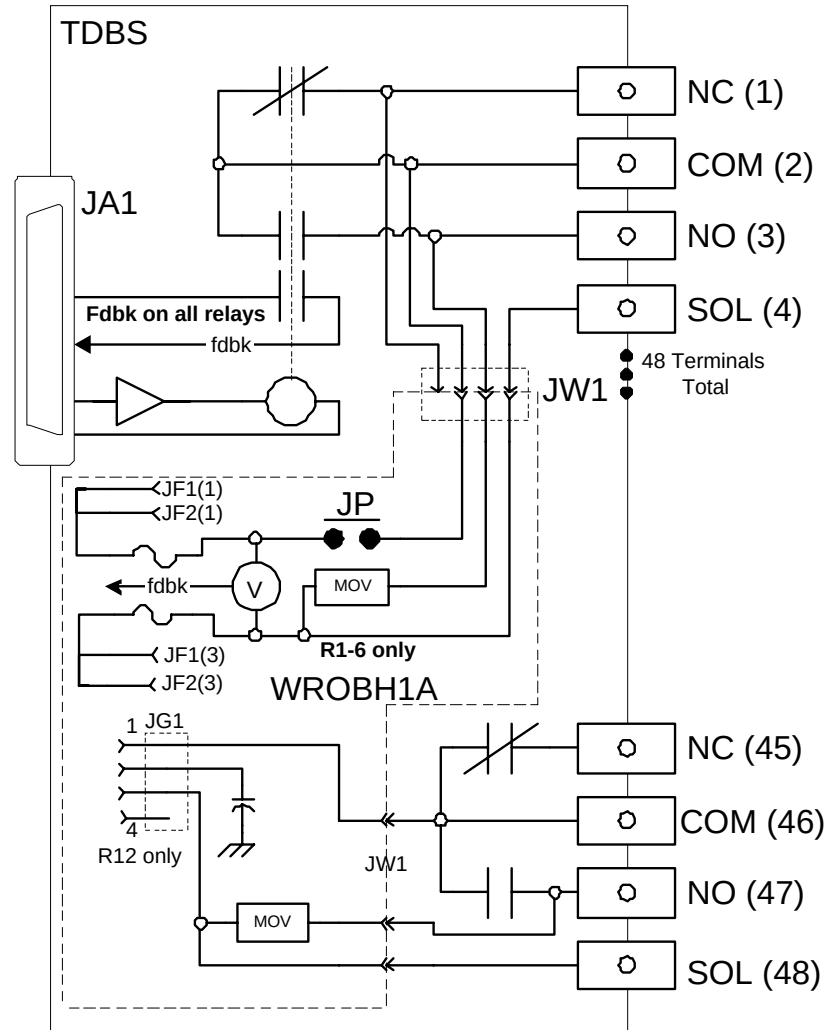
TDBS uses pluggable type terminals and has connectors JW1 and JW2 supporting option board connection. The relay portion of TDBS does not change between groups H2, H4, and H6, only the contact input circuits change. TDBS relays may be used at any specified ac or dc voltage without regard to board group. Electrically TDBS has the following circuit for each of the 12 relays:



Without an option board, the SOL terminal associated with each relay has no connection. TDBS is designed to support a current rating of 5 A and voltage clearance greater than is needed for 250 V ac on all customer screw and JW1 circuits. The relay rating is the limiting item for each application.

## TDBS +WROB

Option board IS200WROBH1A adds capability to TDBS to yield a combination that has the same relay circuit functionality as an IS200TRLYH1B terminal board when used simplex. Included are fused sensed power distribution to the first six relays and dedicated power to the last relay. Electrically IS200TDBS plus IS200WROBH1 has the following circuit. IS200WROBH1 has default fuse values of 3.15 A. Connector JW2 and its connections to JA1 are omitted for clarity.



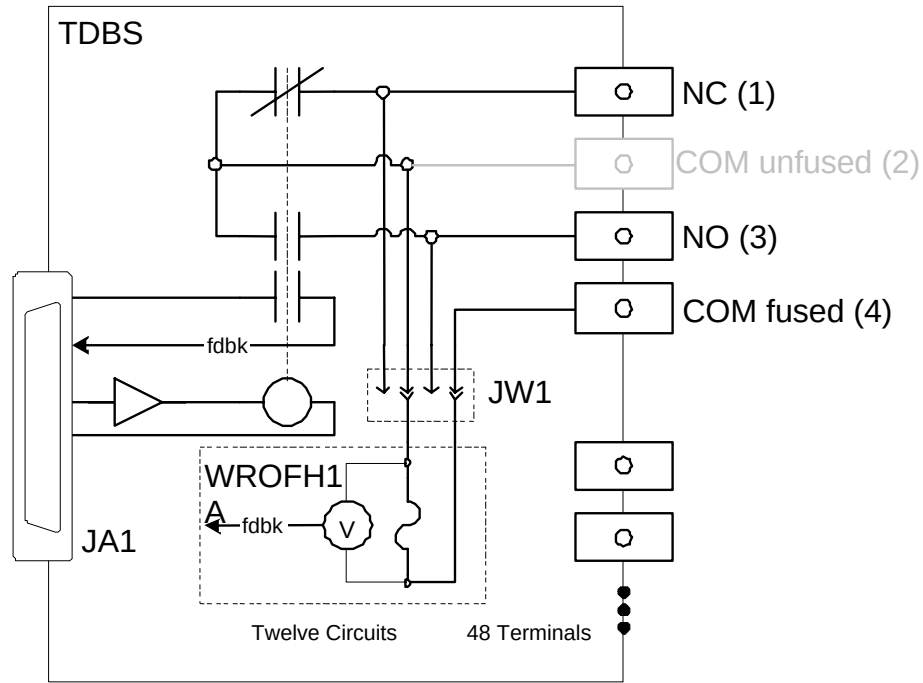
Both sides of the power distribution on relays 1-6 are fused allowing the board to be used in systems where dc power is floating with respect to earth. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications as well as 120 V and 240 V ac applications.

The following table lists the relationship between fuses, jumpers, relays, and terminals.

| Relay | +Fuse | -Fuse | Jumper | Terminals |
|-------|-------|-------|--------|-----------|
| 1     | FU7   | FU1   | JP1    | 1-4       |
| 2     | FU8   | FU2   | JP2    | 5-8       |
| 3     | FU9   | FU3   | JP3    | 9-12      |
| 4     | FU10  | FU4   | JP4    | 13-16     |
| 5     | FU11  | FU5   | JP5    | 17-20     |
| 6     | FU12  | FU6   | JP6    | 21-24     |

## TDBS + WROF

Option board IS200WROFH1A adds an optional fuse in series with the COM connection for each relay output by using the SOL terminal in place of COM. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications as well as 120 V and 240 V ac applications. IS200WROFH1 has default fuse values of 3.15 A. Electrically IS200TDBS plus IS200WROFH1 has the following circuit. Connector JW2 and its connections to JA1 are omitted for clarity.

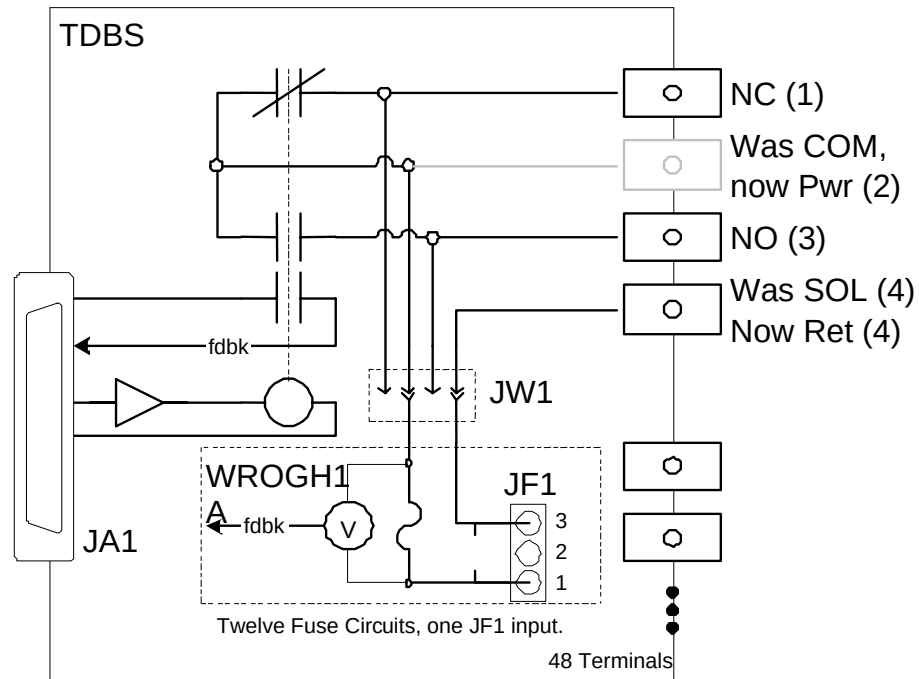


The normal application for this board is when it is desired that each relay output have a fuse in series and power applied from an external source. The board has a second potential application. If the fuse is removed from a circuit, the isolated voltage detector remains. The fourth terminal may now be wired to either the NC or NO terminal to provide isolated contact voltage feedback. I/O pack firmware has a configuration option to turn off fuse blown alarm generation for a given relay if it is being used in this fashion. The terminal table identifies this application as making the fourth screw Vsense.

Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively.

## TDBS + WROG

Option board IS200WROGH1A adds fused power distribution for all twelve relay outputs. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications, as well as 120 V and 240 V ac applications. IS200WROGH1 has default fuse values of 3.15 A. Electrically IS200TDBS plus IS200WROGH1 has the following circuit. Connector JW2 and its connections to JA1 are omitted for clarity.



Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively.

## Specifications

| Item                         | Specification                                                                                                                                                                                                                                                                                                            |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of input channels     | 24 dry contact voltage input channels                                                                                                                                                                                                                                                                                    |
| Wetting voltage              | H2: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc (Pluggable TB)<br>H4: Nominal 48 V dc, floating, ranging from 32 to 64 V dc (Pluggable TB)<br>H6: Nominal 125 V dc, floating, ranging from 100 to 145 V dc (Pluggable TB)                                                                                    |
| Input current                | H2: For 24 V dc applications:<br><br>First 21 circuits draw 2.5 mA<br>Last three circuits draw 10 mA<br>H4: For 48 V dc applications:<br><br>First 21 circuits draw 2.5 mA<br>Last three circuits draw 10.4 mA<br>H6: For 125 V dc applications:<br><br>First 21 circuits draw 2.55 mA<br>Last three circuits draw 10 mA |
| Input filter                 | Hardware filter, 4 ms                                                                                                                                                                                                                                                                                                    |
| Fault detection in I/O board | Loss of contact input wetting voltage<br>Non-responding contact input in test mode                                                                                                                                                                                                                                       |

| Item                            | Specification                                                                                                                                                                                                                                                          |
|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AC voltage rejection            | 12 V rms at 24 V dc wetting voltage. (H2)<br>24 V rms at 48 V dc wetting voltage. (H4)<br>60 V rms at 125 V dc wetting voltage. (H6)                                                                                                                                   |
| Number of relay channels        | 12 relays                                                                                                                                                                                                                                                              |
| Rated voltage on relay contacts | a: Nominal 24 V dc, 48 V dc, or 125 V dc<br>b: Nominal 120 V ac or 240 V ac                                                                                                                                                                                            |
| Max load current                | a: 0.4 A for 125 V dc operation<br>b: 1.2 A for 48 V dc operation<br>c: 3.15 A for 24 V dc operation<br>d: 3.15 A for 120/240 V ac, 50/60 Hz operation                                                                                                                 |
| Max response time on            | 25 ms typical                                                                                                                                                                                                                                                          |
| Max response time off           | 25 ms typical                                                                                                                                                                                                                                                          |
| Contact material                | Silver cad-oxide                                                                                                                                                                                                                                                       |
| Contact life                    | Electrical operations: 100,000<br>Mechanical operations: 10,000,000                                                                                                                                                                                                    |
| Fault detection                 | Relay position feedback using contact pair separate from load contacts.                                                                                                                                                                                                |
| <b>WROBH1 Option Board</b>      |                                                                                                                                                                                                                                                                        |
| Powered Output Circuits         | 6 fused, associated with relays 1-6, fed from parallel connectors JF1 and JF2. Both sides of the power source are fused for each output. MOV suppression on NO contact.<br>1 unfused, associated with relay 12, fed from connector JG1. MOV suppression on NO contact. |
| <b>WROFH1 Option Board</b>      |                                                                                                                                                                                                                                                                        |
| Fused Output Circuits           | 12 fused circuits, one per relay.                                                                                                                                                                                                                                      |
| <b>WROGH1 Option Board</b>      |                                                                                                                                                                                                                                                                        |
| Powered Output Circuits         | 12 fused circuits, one associated with each relay. Single side fusing of the power is associated with the power input on JF1 pin 1. Return power path through JF1pin 3 is not fused.                                                                                   |
| Physical                        |                                                                                                                                                                                                                                                                        |
| Size - TDBS                     | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                                                                                                                                                        |
| Temperature                     | -30 to + 65°C (-22 to 149 °F)                                                                                                                                                                                                                                          |
| Technology                      | Surface-mount                                                                                                                                                                                                                                                          |

## ***Diagnostics***

The I/O processor monitors the following functions on TDBS:

- The contact input wetting voltage is monitored. If the wetting voltage drops to below 40% of the nominal voltage, a diagnostic alarm (fault) is set and latched.
- The TDBS provides diagnostic feedback to PDIO indicating the state of each relay by monitoring an isolated set of contacts on each relay.
- When WROB is used with TDBS isolated voltage feedback is used to detect fuse status for the six fuse pairs on the board.
- When WROF is used with TDBS isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open a diagnostic is generated. The diagnostic may be disabled in PDIO configuration should it be desired to use the feedback circuit with the fuse removed.
- When WROG is used with PDIO isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open a diagnostic is generated.
- The terminal board connector has an ID device that is interrogated by the I/O processor. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. Any relay option card also contains an ID. If a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no jumpers or hardware settings on TDBS.

Option board WROBH1 includes six jumpers that are used to apply or remove power from a relay. Boards are produced with all six jumpers in place. The jumper is removed from the board when a relay is to be used as dry contacts and power distribution is not desired.

There are no jumpers associated with the WROFH1 board. For each relay the inclusion or exclusion of a series fuse is determined by the terminal point used as the relay common. For each relay the associated WROF fuse may be removed to allow direct use of the fuse voltage sensing circuit as a voltage detector.

There are no jumpers associated with the WROGH1 board. For each relay the corresponding fuse may be removed if the relay is to be used to provide dry contacts.



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# TDBT Discrete Input/Output

## Functional Description

The Discrete Input/Output (TDBT) terminal board is a TMR contact input/output terminal board designed for DIN-rail or flat mounting. The TDBT board accepts 24 group isolated contact inputs that are supplied with a nominal 24, 48, or 125 V dc wetting voltage from an external source. The contact inputs have noise suppression to protect against surge and high-frequency noise. TDBT provides 12 form-C relay outputs and accepts an option card to expand relay functions.

In Mark\* Vle systems, the PDIO I/O pack works with the TDBT. Three I/O packs plug into D-type connectors and communicate with the controllers over Ethernet. Three connection points for PDIO are provided. With dual controllers the PDIO on TDBT connector JR1 would be networked to the R controller, JS1 PDIO to the S controller, and JT1 PDIO to both R and S controllers. With TMR controllers one network connection is provided to each PDIO leading to the respective controller. TDBT is not designed to operate correctly with a single PDIO I/O pack.

## Board Versions

Three versions of TDBT are available as follows:

| Terminal Board | Contact Inputs | TB Type   | Wetting Voltage                                          |
|----------------|----------------|-----------|----------------------------------------------------------|
| TDBTH2A        | 24             | Pluggable | Nominal 24 V dc, floating, ranging from 16 to 32 V dc    |
| TDBTH4A        | 24             | Pluggable | Nominal 48 V dc, floating, ranging from 32 to 64 V dc    |
| TDBTH6A        | 24             | Pluggable | Nominal 125 V dc, floating, ranging from 100 to 145 V dc |

IS200WROB is an option board that plugs into TDBT to provide fused and sensed power distribution to the first six relay outputs and dedicated power to the last relay output.

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**Note** The IS200WROF and IS200WROG boards are not compatible with IS200TDBT.

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## Installation

The TDBT plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN rail. Optionally the TDBT plus insulator mounts on a sheet metal assembly that then bolts in a cabinet. The connections are wired directly to two sets of 48 terminal blocks, typically using #18 AWG wires. The upper set of terminals, TB1, connects to the relay portion of the board and the lower set of terminals, TB2, connect to the contact input circuits. Screw assignments for the two sets of terminals are identical to those found on the SRLY relay board and the STCI contact input terminal board. Shields should be terminated on a separate bracket.

## Relay Outputs

If a relay option board is used, it plugs onto TDBT connectors JW1 and JW2 and is held in place by the force of the connectors. The following table identifies the function of each relay terminal point grouped as TB1 as it relates to the presence of an option board. If external power is to be supplied it is wired to a connector provided on the option board.

| TB1<br>Terminal | Relay | TDBT | TDBT +<br>WROB |
|-----------------|-------|------|----------------|
| 1               | 1     | NC   | NC             |
| 2               |       | COM  | COM            |
| 3               |       | NO   | NO             |
| 4               |       |      | SOL            |
| 5               | 2     | NC   | NC             |
| 6               |       | COM  | COM            |
| 7               |       | NO   | NO             |
| 8               |       |      | SOL            |
| 9               | 3     | NC   | NC             |
| 10              |       | COM  | COM            |
| 11              |       | NO   | NO             |
| 12              |       |      | SOL            |
| 13              | 4     | NC   | NC             |
| 14              |       | COM  | COM            |
| 15              |       | NO   | NO             |
| 16              |       |      | SOL            |
| 17              | 5     | NC   | NC             |
| 18              |       | COM  | COM            |
| 19              |       | NO   | NO             |
| 20              |       |      | SOL            |
| 21              | 6     | NC   | NC             |
| 22              |       | COM  | COM            |
| 23              |       | NO   | NO             |
| 24              |       |      | SOL            |

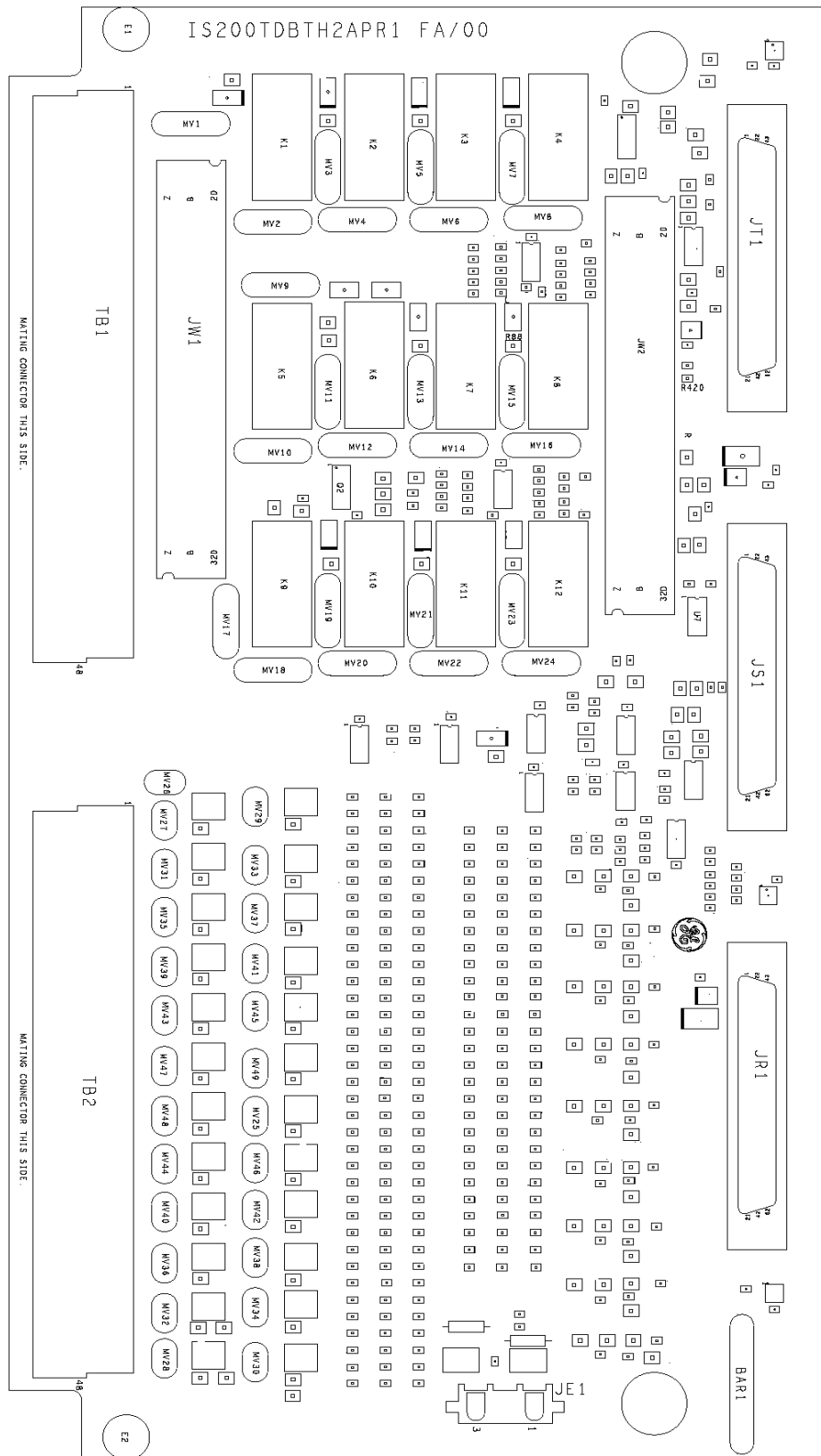
| TB1<br>Terminal | Relay | TDBT | TDBT +<br>WROB |
|-----------------|-------|------|----------------|
| 25              | 7     | NC   | NC             |
| 26              |       | COM  | COM            |
| 27              |       | NO   | NO             |
| 28              |       |      |                |
| 29              | 8     | NC   | NC             |
| 30              |       | COM  | COM            |
| 31              |       | NO   | NO             |
| 32              |       |      |                |
| 33              | 9     | NC   | NC             |
| 34              |       | COM  | COM            |
| 35              |       | NO   | NO             |
| 36              |       |      |                |
| 37              | 10    | NC   | NC             |
| 38              |       | COM  | COM            |
| 39              |       | NO   | NO             |
| 40              |       |      |                |
| 41              | 11    | NC   | NC             |
| 42              |       | COM  | COM            |
| 43              |       | NO   | NO             |
| 44              |       |      |                |
| 45              | 12    | NC   | NC             |
| 46              |       | COM  | COM            |
| 47              |       | NO   | NO             |
| 48              |       |      | SOL            |

## Contact Inputs

Contact input connections are made to the 48 terminals on the lower portion of the terminal board, grouped as TB2. Contact wetting voltage is provided to the board through the JE1 3-pin Mate-n-lok<sup>®</sup> connector on the lower portion of the board.

| <b>TB2</b>      |               | <b>TB2</b>      |               |
|-----------------|---------------|-----------------|---------------|
| <b>Terminal</b> | <b>Signal</b> | <b>Terminal</b> | <b>Signal</b> |
| 1               | Wet 1         | 25              | Wet 13        |
| 2               | In 1          | 26              | In 13         |
| 3               | Wet 2         | 27              | Wet 14        |
| 4               | In 2          | 28              | In 14         |
| 5               | Wet 3         | 29              | Wet 15        |
| 6               | In 3          | 30              | In 15         |
| 7               | Wet 4         | 31              | Wet 16        |
| 8               | In 4          | 32              | In 16         |
| 9               | Wet 5         | 33              | Wet 17        |
| 10              | In 5          | 34              | In 17         |
| 11              | Wet 6         | 35              | Wet 18        |
| 12              | In 6          | 36              | In 18         |
| 13              | Wet 7         | 37              | Wet 19        |
| 14              | In 7          | 38              | In 19         |
| 15              | Wet 8         | 39              | Wet 20        |
| 16              | In 8          | 40              | In 20         |
| 17              | Wet 9         | 41              | Wet 21        |
| 18              | In 9          | 42              | In 21         |
| 19              | Wet 10        | 43              | Wet 22        |
| 20              | In 10         | 44              | In 22         |
| 21              | Wet 11        | 45              | Wet 23        |
| 22              | In 11         | 46              | In 23         |
| 23              | Wet 12        | 47              | Wet 24        |
| 24              | In 12         | 48              | In 24         |

The wetting voltage output terminals are all in parallel and fed from the positive voltage applied to JE1 pin 1. It is permissible to run a single wetting voltage lead from the board terminal to a group of remote contacts and then bring the individual contact wires back to the inputs. Negative or return wetting voltage is supplied by JE1 pin 3.



TDBT Layout

## Operation

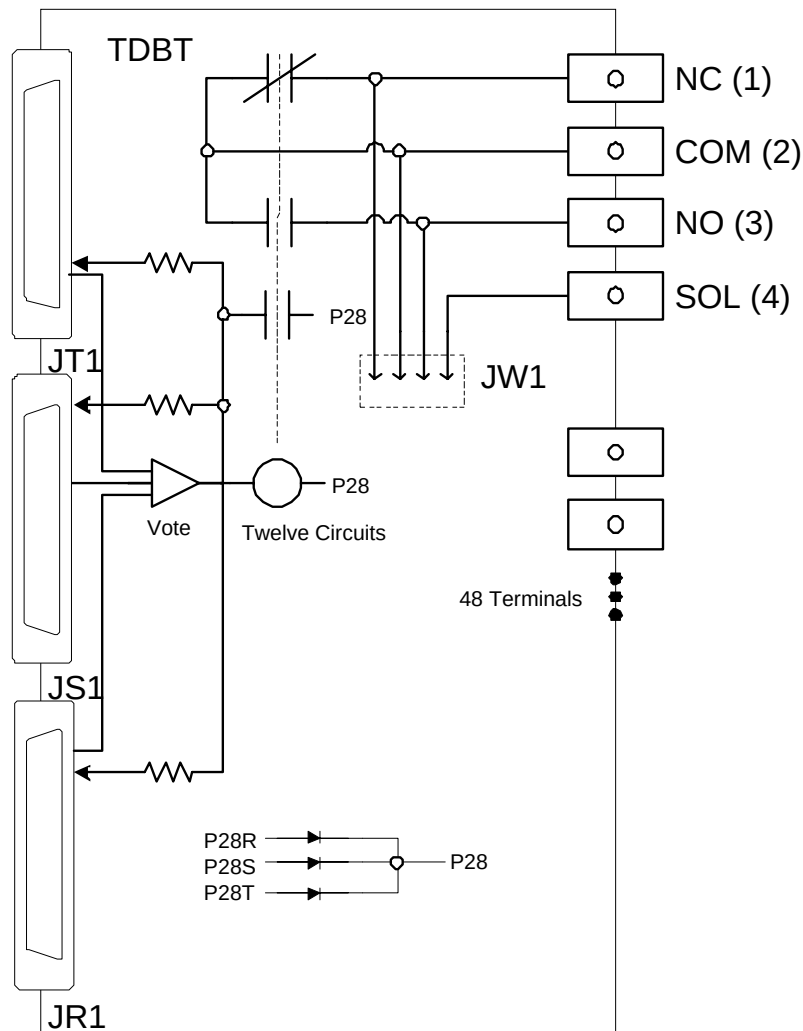
### Contact Inputs

The contact input function and on-board signal conditioning are the same as those on STCI, they are scaled for 24, 48, and 125 V dc wetting voltage. The input wetting voltage range is 16 to 32 V dc, 32 to 64 V dc, and 100 to 145 V dc respectively. The threshold voltage is 50% of the wetting voltage. The contact sensing circuits are shown in the I/O pack description. Contact input currents are resistance limited to 2.5 mA on the first 21 circuits, and 10 mA on circuits 22 through 24. The 24 V dc supply on TDBTH2 is current limited to 0.5 A using polymer positive temperature coefficient fuses that can be reset.

Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The discrete input voltage signals go to the I/O processor which passes them through optical isolators, converts them to digital signals, and transfers them to the controller.

### Relay Outputs

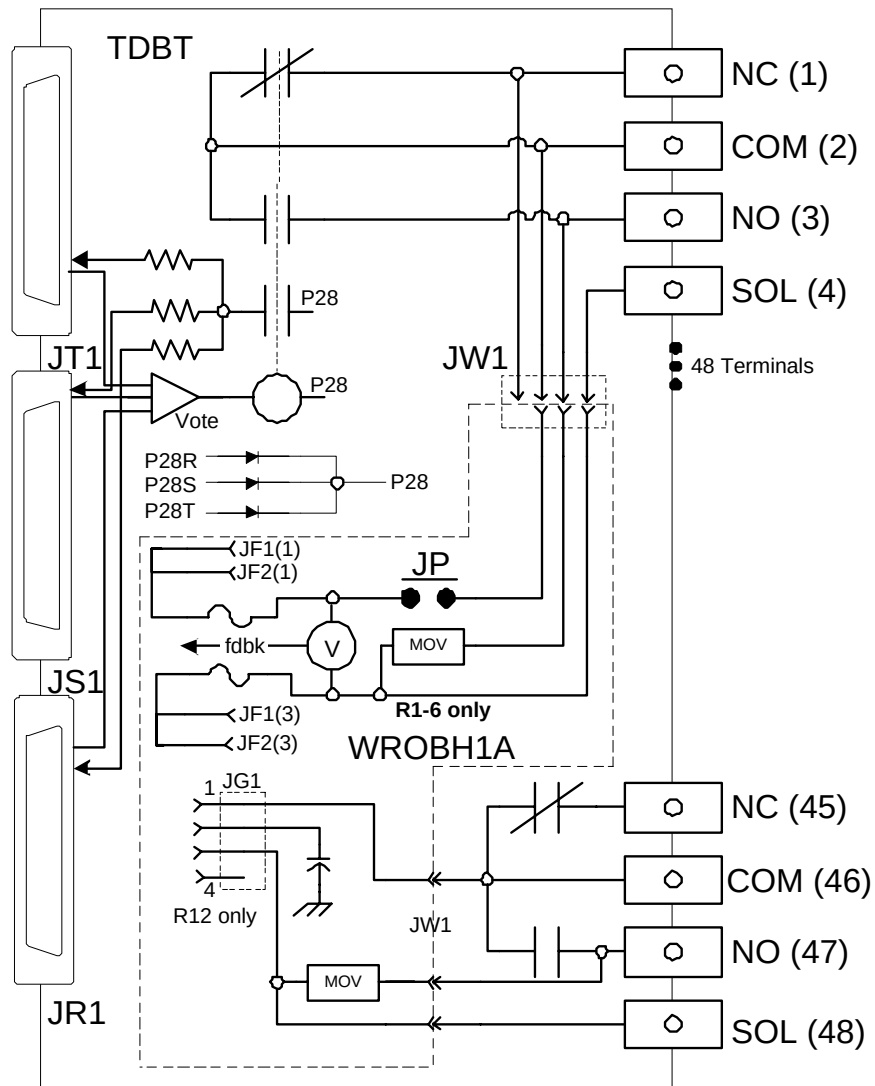
TDBT uses pluggable type terminals and has connectors JW1 and JW2 supporting option board connection. The relay portion of TDBT does not change between groups H2, H4, and H6, only the contact input circuits change. TDBT relays may be used at any specified ac or dc voltage without regard to board group. Electrically TDBT has the following circuit for each of the 12 relays:



Without an option board, the SOL terminal associated with each relay has no connection. TDBT is designed to support a current rating of 5 A and voltage clearance greater than is needed for 250 V ac on all customer screw and JW1 circuits. The relay contact rating is the limiting item for each application.

### TDBT +WROB

Option board IS200WROBH1A adds capability to TDBT to yield a combination that has the same relay circuit functionality as an IS200TRL YH1B terminal board when used in a TMR system. Included are fused sensed power distribution to the first six relay contacts and dedicated power to the last relay contact. Electrically IS200TDBT plus IS200WROBH1 has the following circuit. IS200WROBH1 has default fuse values of 3.15 A. Connector JW2 and its connections to J1 are omitted for clarity.



Both sides of the power distribution on relays 1-6 are fused allowing the board to be used in systems where dc power is floating with respect to earth. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications as well as 120 V and 240 V ac applications.

The following table lists the relationship between fuses, jumpers, relays, and terminals.

| +Fuse | -Fuse | Jumper | Terminals |
|-------|-------|--------|-----------|
| FU7   | FU1   | JP1    | 1-4       |
| FU8   | FU2   | JP2    | 5-8       |
| FU9   | FU3   | JP3    | 9-12      |
| FU10  | FU4   | JP4    | 13-16     |
| FU11  | FU5   | JP5    | 17-20     |
| FU12  | FU6   | JP6    | 21-24     |

## Specifications

| Item                                       | Specification                                                                                                                                                                                                                                                                                                |
|--------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels                         | 24 dry contact voltage input channels                                                                                                                                                                                                                                                                        |
| Wetting voltage                            | H2: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc (Pluggable TB)<br>H4: Nominal 48 V dc, floating, ranging from 32 to 64 V dc (Pluggable TB)<br>H6: Nominal 125 V dc, floating, ranging from 100 to 145 V dc (Pluggable TB)                                                                        |
| Input current                              | H2: For 24 V dc applications:<br>First 21 circuits draw 2.5 mA<br>Last three circuits draw 10 mA<br>H4: For 48 V dc applications:<br>First 21 circuits draw 2.5 mA<br>Last three circuits draw 10.4 mA<br>H6: For 125 V dc applications:<br>First 21 circuits draw 2.55 mA<br>Last three circuits draw 10 mA |
| Input filter                               | Hardware filter, 4 ms                                                                                                                                                                                                                                                                                        |
| Fault detection in I/O board               | Loss of contact input wetting voltage<br>Non-responding contact input in test mode                                                                                                                                                                                                                           |
| AC voltage rejection                       | 12 V rms at 24 V dc wetting voltage. (H2)<br>24 V rms at 48 V dc wetting voltage. (H4)<br>60 V rms at 125 V dc wetting voltage. (H6)                                                                                                                                                                         |
| Number of relay channels on one TDBT board | 12 relays                                                                                                                                                                                                                                                                                                    |
| Rated voltage on relay contacts            | a: Nominal 24 V dc, 48 V dc, or 125 V dc<br>b: Nominal 120 V ac or 240 V ac                                                                                                                                                                                                                                  |
| Max load current                           | a: 0.4 A for 125 V dc operation<br>b: 1.2 A for 48 V dc operation<br>c: 3.15 A for 24 V dc operation<br>d: 3.15 A for 120/240 V ac, 50/60 Hz operation                                                                                                                                                       |
| Max response time on                       | 25 ms typical                                                                                                                                                                                                                                                                                                |
| Max response time off                      | 25 ms typical                                                                                                                                                                                                                                                                                                |
| Contact material                           | Silver cad-oxide                                                                                                                                                                                                                                                                                             |
| Contact life                               | Electrical operations: 100,000<br>Mechanical operations: 10,000,000                                                                                                                                                                                                                                          |
| Fault detection                            | Relay position feedback using contact pair separate from load contacts.                                                                                                                                                                                                                                      |

| Item                       | Specification                                                                                                                                                                                                                                                                              |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>WROBH1 Option Board</b> |                                                                                                                                                                                                                                                                                            |
| Powered Output Circuits    | 6 fused, associated with relays 1-6, fed from parallel connectors JF1 and JF2. Both sides of the power source are fused for each output. MOV suppression across NO relay contact.<br>1 unfused, associated with relay 12, fed from connector JG1. MOV suppression across NO relay contact. |
| <b>Πηψισαλ</b>             |                                                                                                                                                                                                                                                                                            |
| Size - TDBT                | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                                                                                                                                                                            |
| Temperature                | -30 to + 65°C (-22 to 149 °F)                                                                                                                                                                                                                                                              |
| Technology                 | Surface-mount                                                                                                                                                                                                                                                                              |

## ***Diagnostics***

The I/O processor monitors the following functions on TDBT:

- The contact wetting voltage is monitored. If the wetting voltage drops to below 40% of the nominal voltage, a diagnostic alarm (fault) is set and latched.
- The TDBT provides diagnostic feedback to PDIO indicating the state of each relay by monitoring an isolated set of contacts on each relay. Position feedback is fanned out to all three PDIO packs.
- When WROB is used with TDBT isolated voltage feedback is used to detect fuse status for the six fuse pairs on the board. TDBT provides this feedback to all three PDIO packs.
- Each terminal board I/O pack connector has an ID device that is interrogated by the I/O processor. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. WROB contains three ID devices, one for each PDIO. If a mismatch between I/O pack, terminal board, or option card is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no jumpers or hardware settings on TDBT.

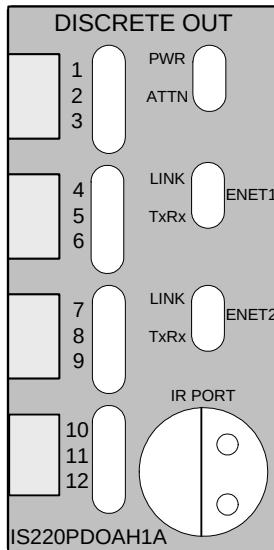
Option board WROBH1 includes six jumpers that are used to apply or remove power from a relay. Boards are produced with all six jumpers in place. The jumper is removed from the board when a relay is to be used as dry contacts and power distribution is not desired.



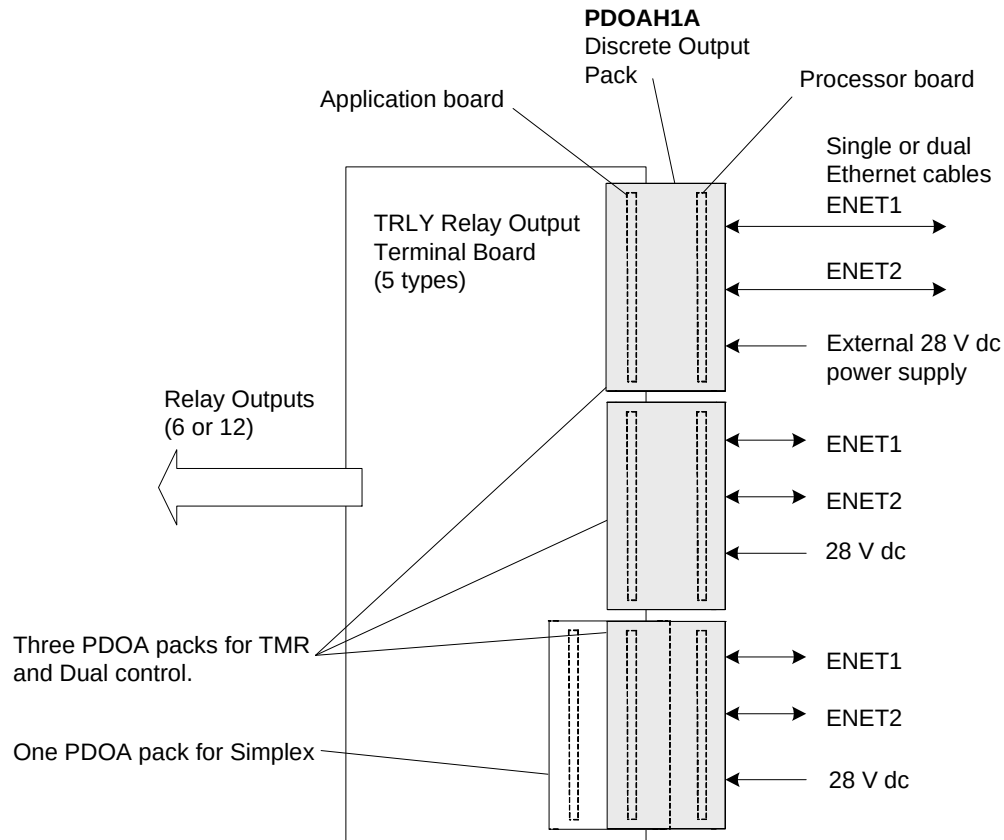
# PDOA Discrete Output

## PDOA Discrete Output

### Functional Description



The Discrete Output (PDOA) pack provides the electrical interface between one or two I/O Ethernet networks and a discrete output terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs and an acquisition board specific to the discrete output function. The pack is capable of controlling up to 12 relays and accepts terminal board specific feedback. Electromagnetic relays (with types TRLYH1B, C, D, and F terminal boards) and solid-state relays (with type TRLYH1E boards) are available. Input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PDOAH1A is compatible with six types of discrete (relay) output terminal boards, including the TRLY boards and SRLY boards, but not the DIN-rail mounted DRLY boards. The following table gives details of the compatibility:

| Terminal Board | TRLYH1B, H1C, H1D, H1E & H1F        | DRLY | SRLYH1A & B  |
|----------------|-------------------------------------|------|--------------|
| Control mode   | Simplex -Yes    Dual-No    TMR -Yes | No   | Simplex -Yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

## Installation

### ➤ To install the PDOA pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PDOA I/O pack for simplex or three PDOA I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC37 connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

---

**Note** The PDOA mounts directly on a Mark VIe terminal board. Simplex terminal boards have a single DC-37 connector that receives the PDOA. TMR-capable terminal boards have four DC-37 connectors, one used for simplex operation and three used for TMR operation. PDOA directly supports all of these connections.

---

# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

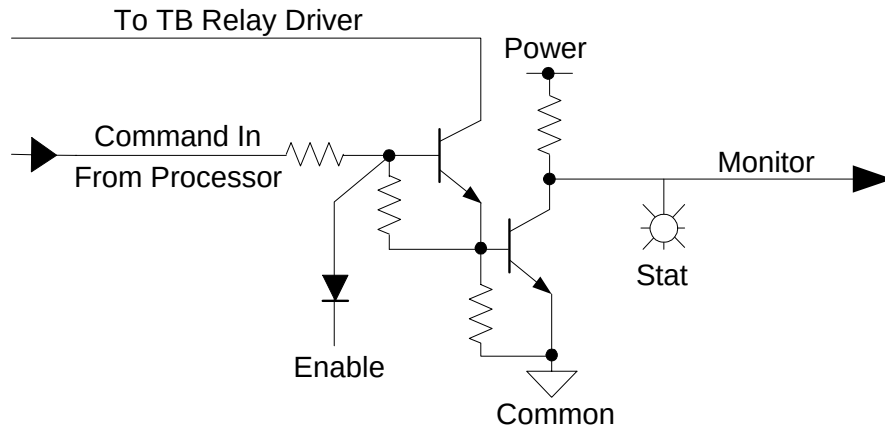
The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## Relay Command Signals

The PDOA relay command signals are the first stage of signal conditioning and level shifting to interface the terminal board outputs to the control logic. Each output is an open collector transistor circuit with a current monitor to sense when the output is picked up and connected to a load. The status LEDs and monitor outputs indicate when an output is picked up and connected to the terminal board. If an output is picked up and the correct load is not sensed, the status LED will be off and the monitor line will be false.



Relay Command Signals

## Output Enable

All of the outputs are disabled during power application until a variety of internal self-tests are completed. An enable line reflects the status of all required conditions for operation. This function provides a path independent of the command to ensure relays stay dropped-out during power-up and initialization.

## Monitor Inputs/Control

There are 15 inverting level shifting monitor input circuits. On a typical TRL Y terminal board 12 of these circuits are used as relay contact feedbacks and the other three are used for fuse status. An inverting level shifting line is also provided from the control to the terminal board for status feedback multiplexing control allowing the pack to receive two sets of 15 signals from a terminal board.

## ID Line

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## Power Management

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly (¼ cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed (¾ cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Connectors

- A DC-62 pin connector on the underside of the I/O pack connects directly to a discrete output terminal board.
- An RJ45 Ethernet connector named ENET1 on the pack side is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the pack side is the redundant or secondary system interface.

---

**Note** The terminal board provides fused power output from a power source that is applied directly to the terminal board, not through this pack connector.

---

## Specifications

| Item                                      | Specification                                                                                                   |
|-------------------------------------------|-----------------------------------------------------------------------------------------------------------------|
| Number of relay channels in one PDOA pack | 12 relays (different types depending on the terminal board)                                                     |
| Relay and coil monitoring                 | 15 pack inputs. The selection of monitor feedbacks depends on the type of terminal board used, based on ID chip |
| I/O pack response time                    | From Ethernet command to output is approximately in 6 ms.                                                       |
| SOE reporting                             | Each relay may be configured to report operation in the Sequence of Events (SOE) record.                        |
| <b>Physical</b>                           |                                                                                                                 |
| Size                                      | 8.26 cm high x 4.19 cm wide x 12.1 cm deep<br>(3.25 in. x 1.65 in. x 4.78 in.)                                  |
| Technology                                | Surface-mount                                                                                                   |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- A comparison is made between the commanded state of each relay drive and the feedback from the command output circuit.
- Relay board specific feedback is read by the pack and processed. The information varies depending on the relay board type. Refer to relay terminal board documentation for feedback specifics.

Details of the individual diagnostics are available in the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter     | Description                                             | Choices            |
|---------------|---------------------------------------------------------|--------------------|
| PDOA_ModGrps  |                                                         |                    |
| System Limits | Enable or disable all system limit checking.            | Enable, disable    |
| Redundancy    | Redundancy mode of the pack                             | Simplex, Dual, TMR |
| FuseSignJ3    | RelayFdbk signals. Monitor fuse volts or contact volts. |                    |
| PDOA_Input1   |                                                         |                    |
| ContactInput  |                                                         |                    |
| Signal Invert | Inversion makes signal true if contact is open.         |                    |
| SeqOfEvents   | Record contact transitions in sequence of events        |                    |
| DiagVoteEnab  | Enable voting disagreement diagnostic                   |                    |
| SignalFilter  |                                                         |                    |
| PDOA_Output   |                                                         |                    |
| Relay Output  |                                                         | Used, Unused       |
| Signal Invert | Inversion makes relay closed if signal is false.        |                    |
| SeqOfEvents   | Record relay command transitions in sequence of events  |                    |
| PDOA_Output1  |                                                         |                    |
| Relay Output  |                                                         |                    |
| Signal Invert | Inversion makes relay closed if signal is false.        |                    |
| SeqOfEvents   | Record relay command transitions in sequence of events  |                    |
| FuseDiag      | Enable fuse diagnostic                                  |                    |

| IS220PDOA PointsDef        |                                                   | Direction  | Type        |
|----------------------------|---------------------------------------------------|------------|-------------|
| L3DIAG_PDOA                | I/O diagnostic indication                         | Input      | BIT         |
| LINK_OK_PDOA               | I/O link okay indication                          | Input      | BIT         |
| ATTN_PDOA                  | I/O Attention Indication                          | Input      | BIT         |
| IOPackTmpr                 | I/O pack temperature                              | Input      | FLOAT       |
| <b>IS200TRLY PointDefs</b> |                                                   |            |             |
| Relay01                    |                                                   |            |             |
| Relay01Fdbk                | Relay 01 contact voltage (first set of 12 relays) | Point Edit | (Input BIT) |
| Fuse01Fdbk                 | Fuse voltage                                      | Point edit | (Input BIT) |

## Alarms

### PDOA Specific Alarms

| Alarm ID | Alarm Description                                                | Possible Cause                                                                                                                                                                          | Solution                                                                                                                                                                                                                        |
|----------|------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 33-129   | Logic Signal [ ] Voting Mismatch                                 | Voter disagreement detected between R, S, & T controller.                                                                                                                               | Signal received from one I/O pack of a TMR set does not agree with the other two.                                                                                                                                               |
| 130-141  | Fuse [ ] blown.                                                  | I/O pack fuse status feedback indicates a possible blown fuse.                                                                                                                          | Check the indicated fuse. Check power input to the terminal board. Check terminal board configuration. Check I/O pack configuration. Confirm all connectors aligned and fully seated. Replace I/O pack. Replace terminal board. |
| 142      | All fuses blown or no terminal board excitation                  | All fuse sensing indicates an open fuse. This may be due to loss of input power to the terminal board. Without power to the fuses the sensing may indicate a false open fuse condition. | Confirm correct input power to terminal board. Check pack connector alignment and seating. Check pack configuration. Check all fuses. Replace I/O pack. Replace terminal board.                                                 |
| 143-154  | Relay Output Coil [ ] does not match requested state             | TRLY__B, TRLY__F, SRLY specific indication that relay feedback does not match commanded state.                                                                                          | Clear voter disagreements. Check I/O pack connector alignment and seating. Check I/O pack configuration. Replace terminal board.                                                                                                |
| 155-166  | NO [Normally Open] contact [ ] voltage disagreement with command | Voltage is not detected across an open TRLY__C or TRLY__E output contact.                                                                                                               | Clear voter disagreements. Check application to ensure voltage should be present when relay is open. Check that voltage is within published detection range. Check I/O pack configuration. Replace terminal board.              |
| 167-178  | Relay Driver [ ] does not match requested state                  | Relay command signal as seen at the I/O pack output connector to the terminal board does not match the commanded state.                                                                 | Command signal feedback requires a properly connected terminal board. Check pack-terminal board connector alignment and seating. Replace I/O pack. Replace terminal board.                                                      |
| 179-190  | Solenoid Coil [ ] Bad                                            | TRLY__D specific indication that a connected load does not fall within published impedance limits.                                                                                      | Clear voter disagreements. Check for field wiring open or short circuits. Check attached load to ensure impedance is within published limits for TRLY__D. Check TRLY input power. Relace TRLY__D.                               |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |



| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

## ***TRL YH1B Relay Output with Coil Sensing***

### ***Functional Description***

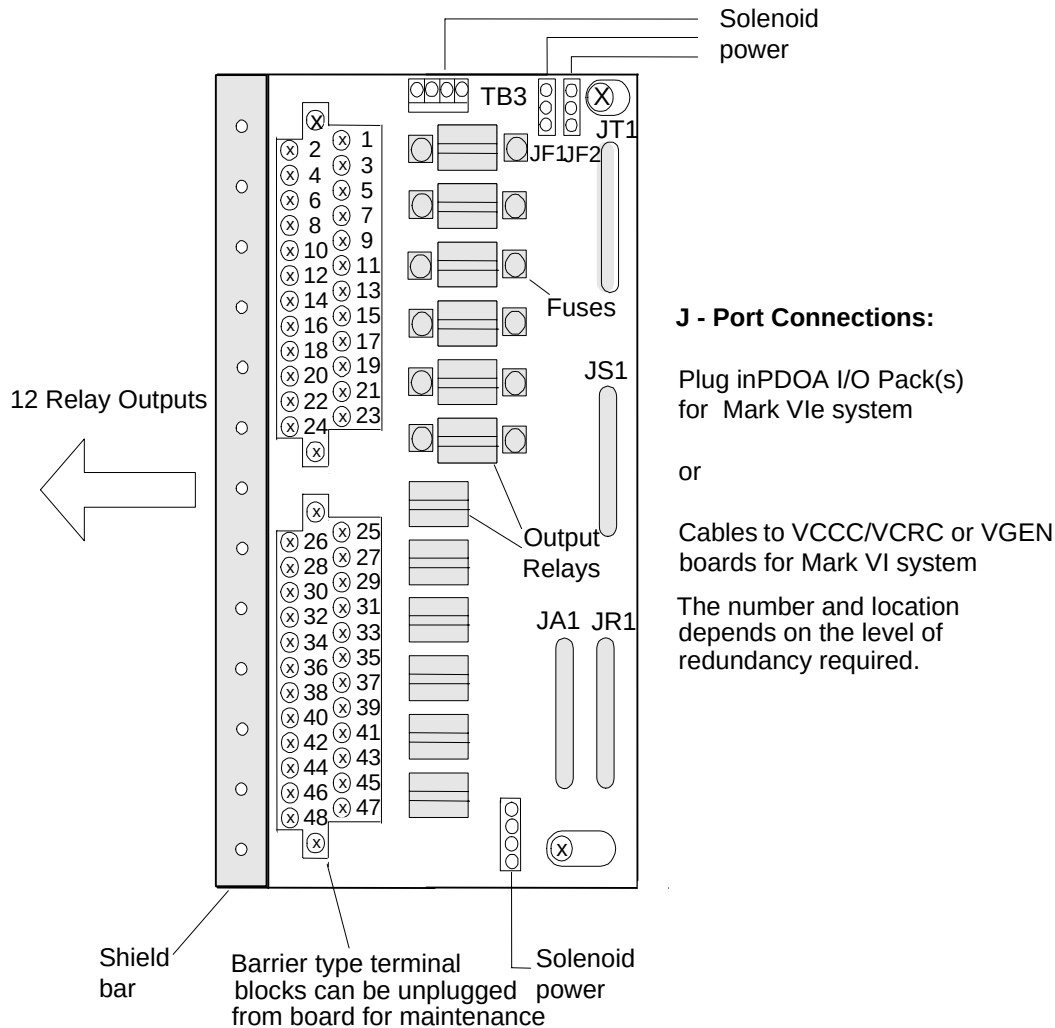
The Relay Output with coil sensing (TRL YH1B) terminal board holds 12 plug-in magnetic relays. The first six relay circuits configured by jumpers for either dry, Form-C contact outputs, or to drive external solenoids. A standard 125 V dc or 115/230 V ac source, or an optional 24 V dc source with individual jumper selectable fuses and on-board suppression, can be provided for field solenoid power. The next five relays (7-11) are unpowered isolated Form-C contacts. Output 12 is an isolated Form-C contact, used for special applications such as ignition transformers.

### ***Mark VI Systems***

In Mark\* VI systems, TRL Y is controlled by the VCCC, VCRC, or VGEN board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

## Mark VIe Systems

In the Mark VIe system, the TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.



TRLYH1B Relay Output Terminal Board

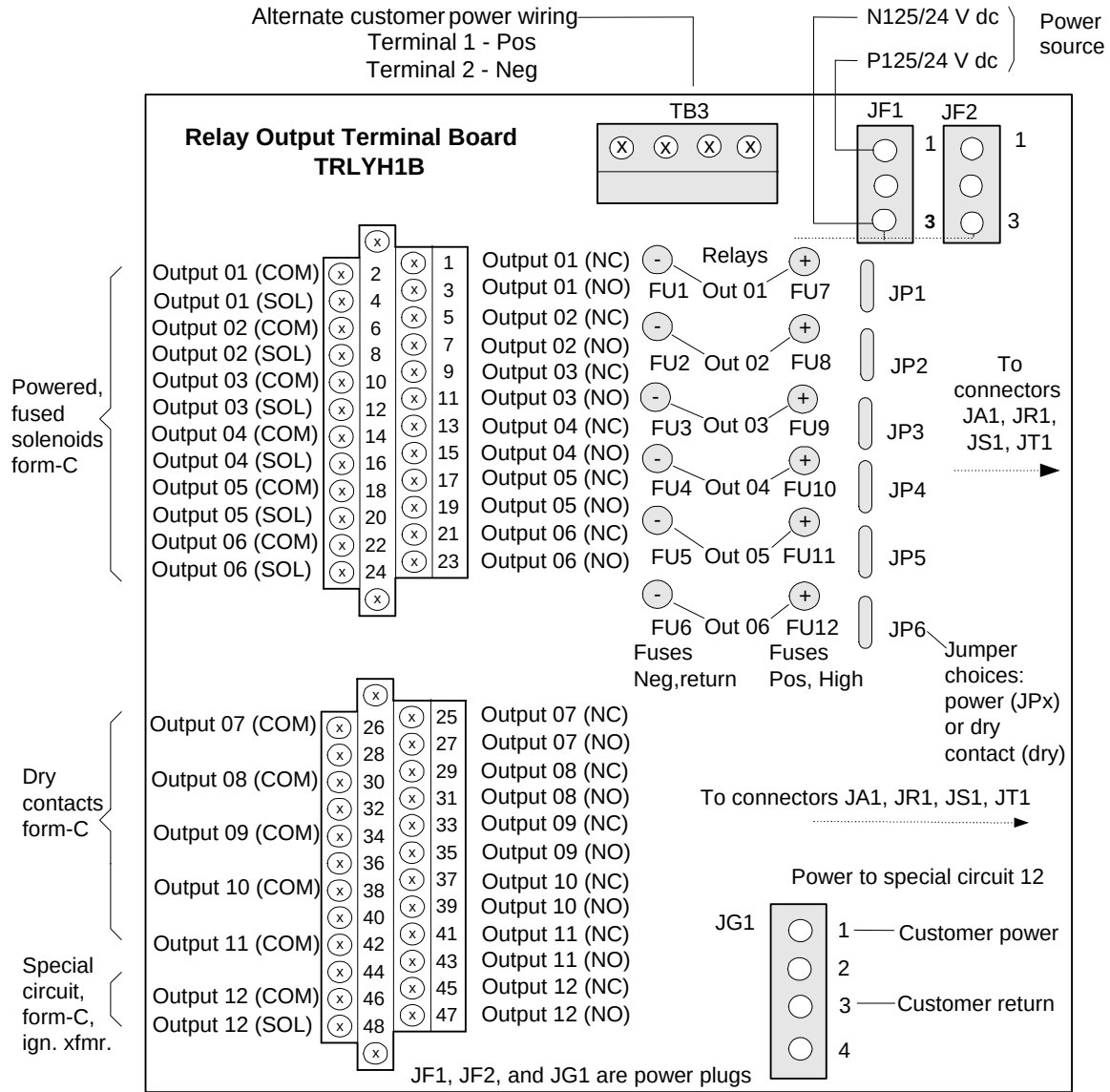
## Installation

Connect the wires for the 12 relay outputs directly to two I/O terminal blocks on the terminal board as shown in the figure, *TRLYH1B Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located on the left side of each terminal block.

Connect the solenoid power for outputs 1-6 to JF1. JF2 can be used to daisy chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used. Connect power for the special solenoid, Output 12, to connector JG1.

Jumpers JP1-JP6 are removed in the factory and shipped in a plastic bag. Re-install the appropriate jumper if power to a field solenoid is required. Conduct individual loop energization checks as per standard practices and install the jumpers as required. For isolated contact applications, remove the fuses to ensure that suppression leakage is removed from the power bus.

**Note** These jumpers are also for isolation of the monitor circuit when used on isolated contact applications.

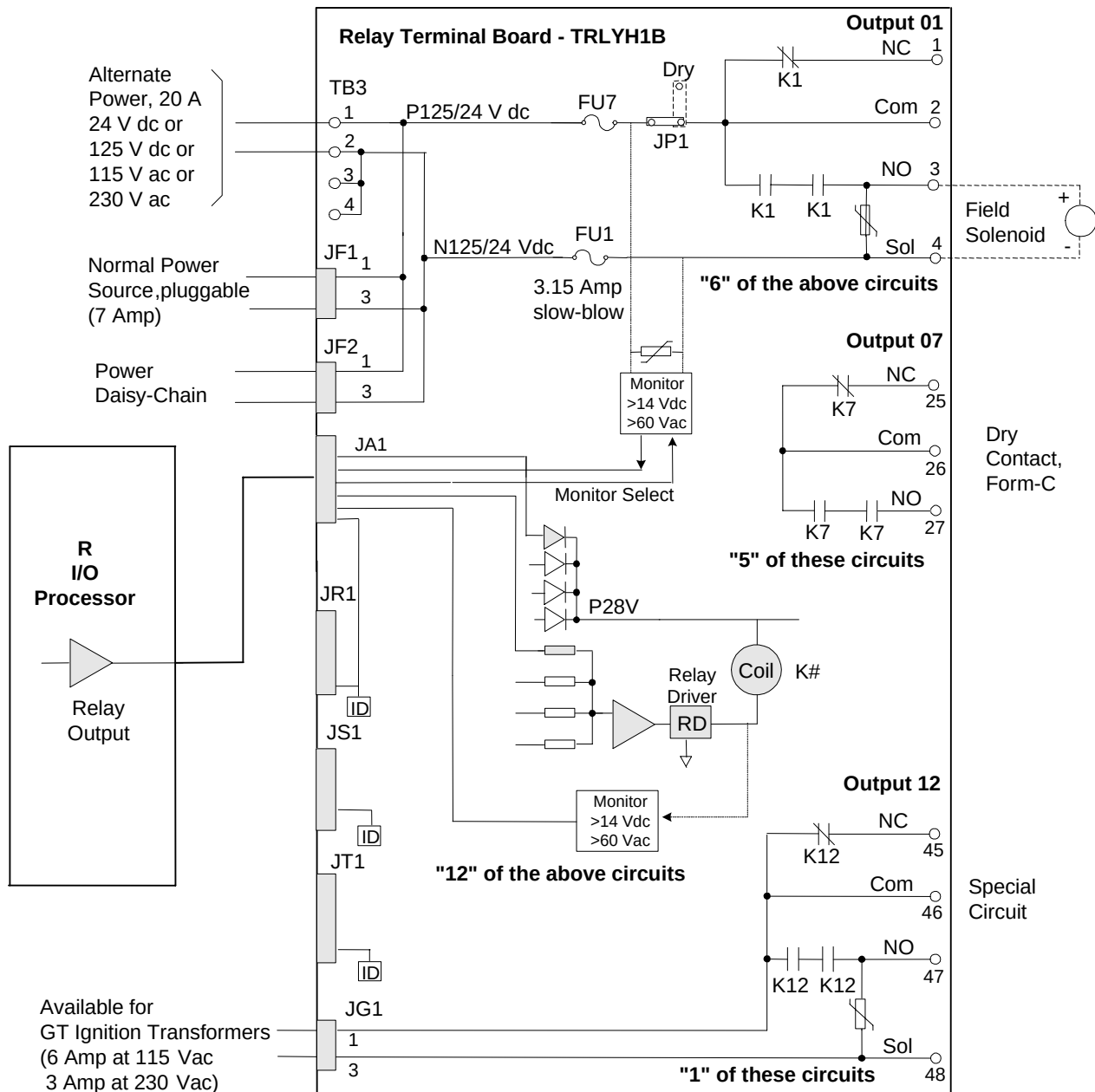


TRLYH1B Terminal Board Wiring

## Operation

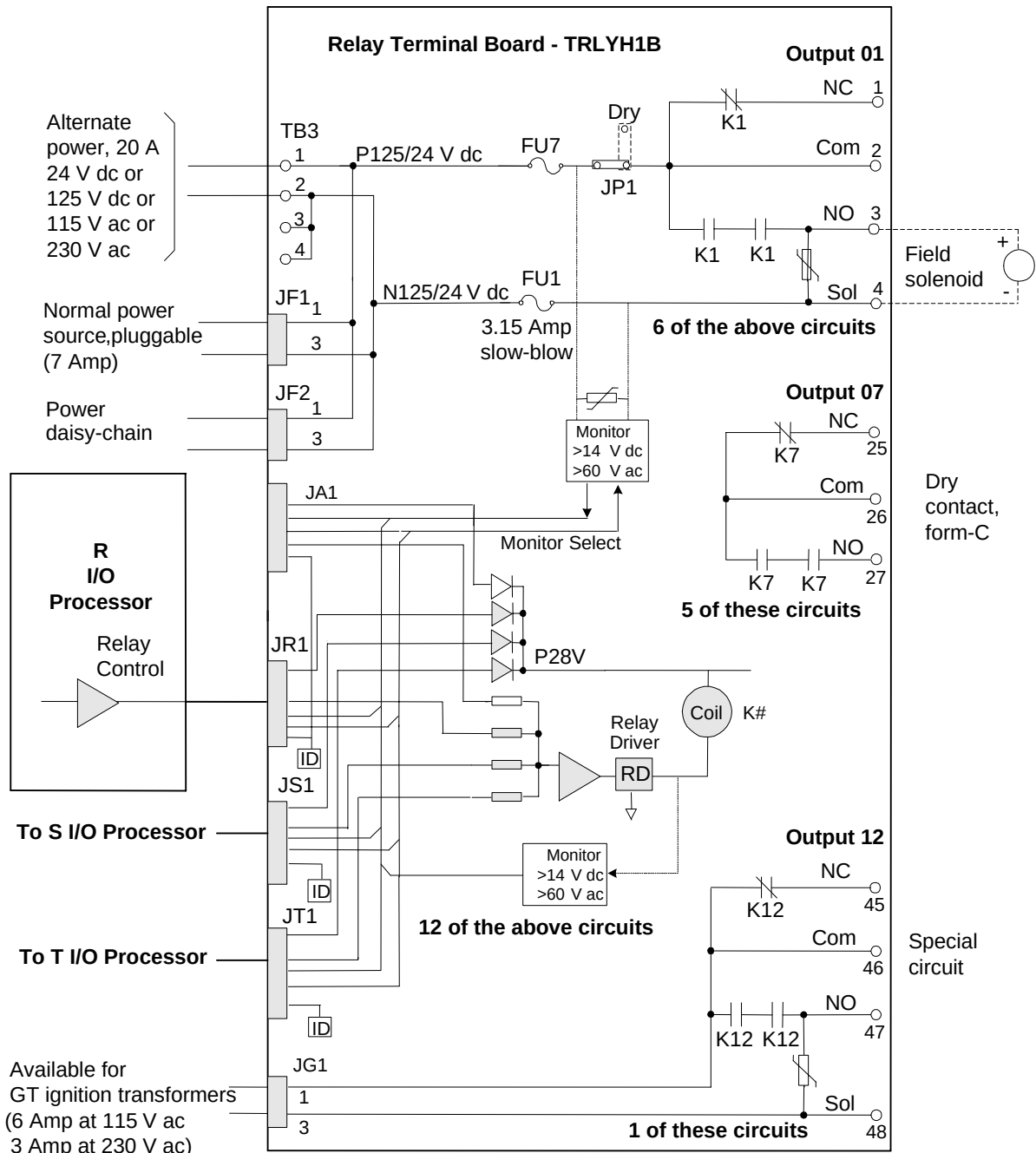
Relay drivers, fuses, and jumpers are mounted on the TRLYH1B. For simplex operation, D-type connectors carry control signals and monitor feedback voltages between the I/O processors and TRLY through JA1.

Relays are driven at the frame rate and have a 3.0 A rating. The rated contact-to-contact voltage is 500 V ac for one minute. The rated coil to contact voltage is 1,500 V ac for one minute. The typical time to operate is 10 ms. Relays 1-6 have a 250 V metal oxide varistor (MOV) for transient suppression between normally open (NO) and the power return terminals. The relay outputs have a failsafe feature that vote to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O processor is lost.



TRLYH1B Circuits, Simplex System

For TMR applications, relay control signals are fanned into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay coils comes from all three I/O processors and is diode-shared. The following figure shows a TRLYH1B in a TMR system.



TRLYH1B Circuits, TMR System

## ***Specifications***

| <b>Item</b>                                | <b>Specifications</b>                                                                                                                                                                                                  |
|--------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of relay channels on one TRLY board | 12: 6 relays with optional solenoid driver voltages<br>5 relays with dry contacts only<br>1 relay with 7 A rating                                                                                                      |
| Rated voltage on relays                    | a: Nominal 125 V dc or 24 V dc<br>b: Nominal 115/230 V ac                                                                                                                                                              |
| Max load current                           | a: 0.6 A for 125 V dc operation<br>b: 3.0 A for 24 V dc operation<br>c: 3.0 A for 115/230 V ac, 50/60 Hz operation                                                                                                     |
| Max response time on                       | 25 ms typical                                                                                                                                                                                                          |
| Max response time off                      | 25 ms typical                                                                                                                                                                                                          |
| Maximum inrush current                     | 10 A                                                                                                                                                                                                                   |
| Contact material                           | Silver cad-oxide                                                                                                                                                                                                       |
| Contact life                               | Electrical operations: 100,000<br>Mechanical operations: 10,000,000                                                                                                                                                    |
| Fault detection                            | Loss of relay solenoid excitation current<br>Coil current disagreement with command<br>Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost. |
| <b>Physical</b>                            |                                                                                                                                                                                                                        |
| Size                                       | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                                                                                                        |
| Temperature                                | -30 to + 65°C (-22 to +149 °F)                                                                                                                                                                                         |

## ***Diagnostics***

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG\_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## **Configuration**

Board adjustments are made as follows:

- Jumpers JP1 through JP12. If contact voltage sensing is required, insert jumpers for selected relays.
- Fuses FU1 through FU12. If power is required for relays 1-6, two fuses should be placed in each power circuit supplying those relays. For example, FU1 and FU7 supply relay output 1. Refer to terminal board wiring diagram for more information.

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## **TRL YH1C Relay Output with Contact Sensing**

### **Functional Description**

The Relay Output with contact sensing (TRL YH1C) terminal board holds 12 plug-in magnetic relays. The first six relay circuits are Form-C contact outputs to drive external solenoids. A standard 125 V dc or 115 V ac source with fuses and on-board suppression is provided for field solenoid power. TRL YH2C holds 12 plug-in magnetic relays. The first six relay circuits are Form-C contact outputs to drive external solenoids. A standard 24 V dc source with fuses and on-board suppression is provided for field solenoid power.

The next five relays (7-11) are unpowered, isolated Form-C contacts. Output 12 is an isolated Form-C contact with non-fused power supply, used for ignition transformers. For example, 12 NO contacts have jumpers to apply or remove the feedback voltage sensing.

TRL YH1C and H2C are the same as the standard TRL YH1B board except for the following:

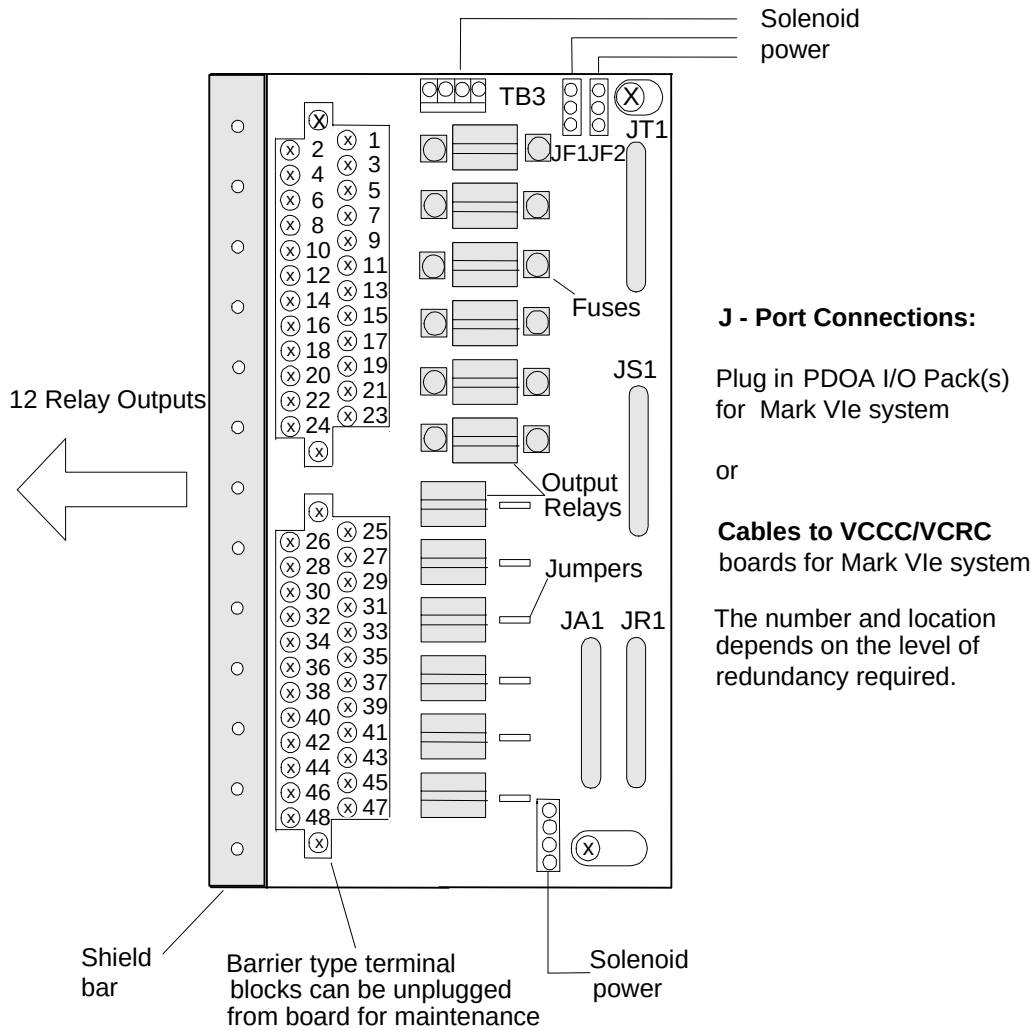
- Six jumpers for converting the solenoid outputs to dry contact type are removed. These jumpers were associated with the fuse monitoring.
- Input relay coil monitoring is removed from the 12 relays.
- Relay contact voltage monitoring is added to the 12 relays. Individual monitoring circuits have voltage suppression and can be isolated by removing their associated jumper.
- High-frequency snubbers are installed across the NO and SOL terminals on the six solenoid driver circuits and on the special circuit, output 12.

### **Mark VI Systems**

In the Mark\* VI system, the TRL Y is controlled by the VCCC or VCRC board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

## Mark Vle Systems

In the Mark Vle system, TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.



*TRLYH1C Relay Output Terminal Board With Voltage Sensing*

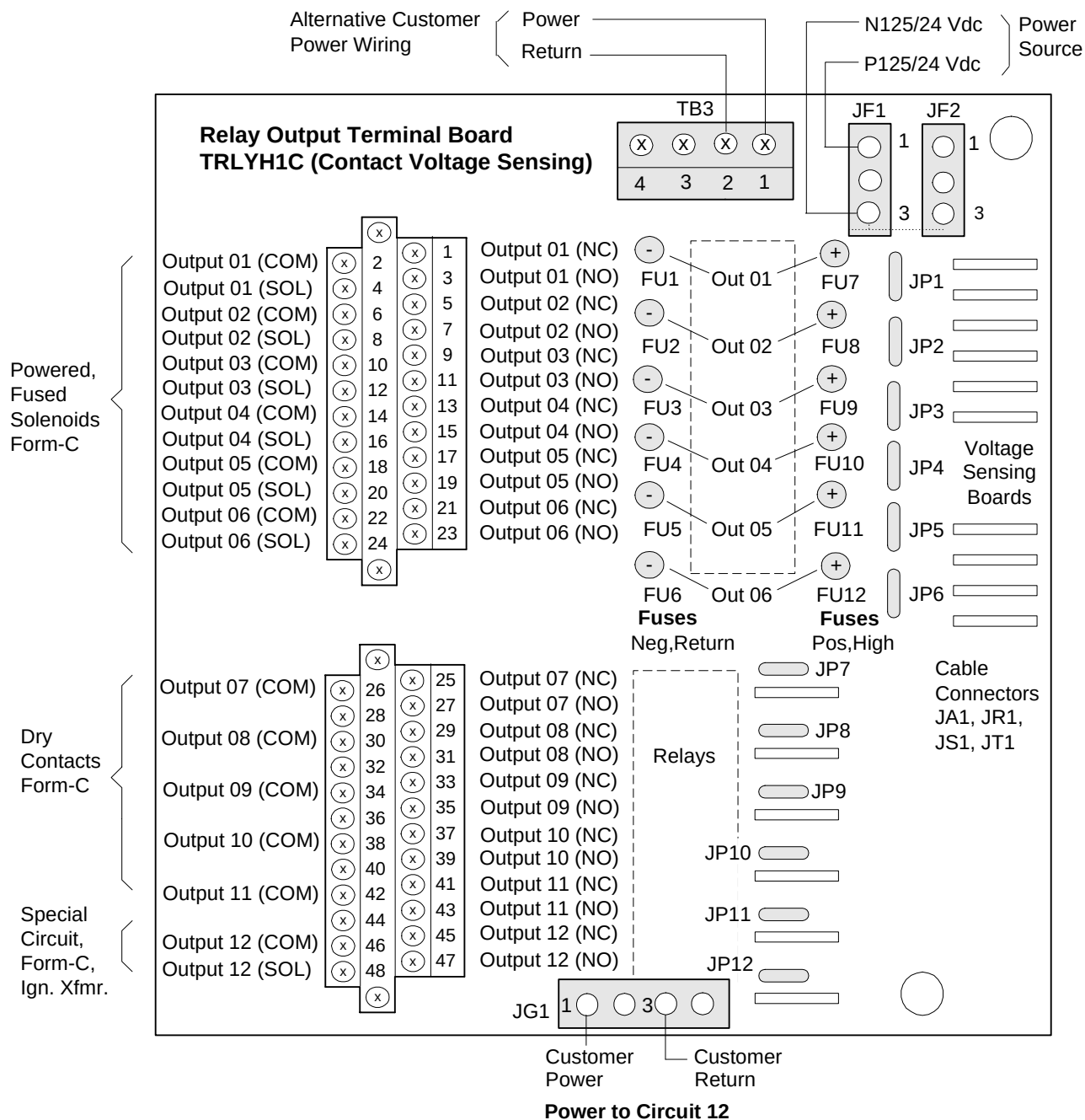


## Installation

Connect the wires for the 12 relay outputs directly to two I/O terminal blocks on the terminal board as shown in the figure, *TRLYH1C Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

Connect the solenoid power for outputs 1-6 to JF1 normally. JF2 can be used to daisy-chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used. Connect power for the special solenoid, Output 12, to connector JG1.

Jumpers JP1-12 remove the voltage monitoring from selected outputs.



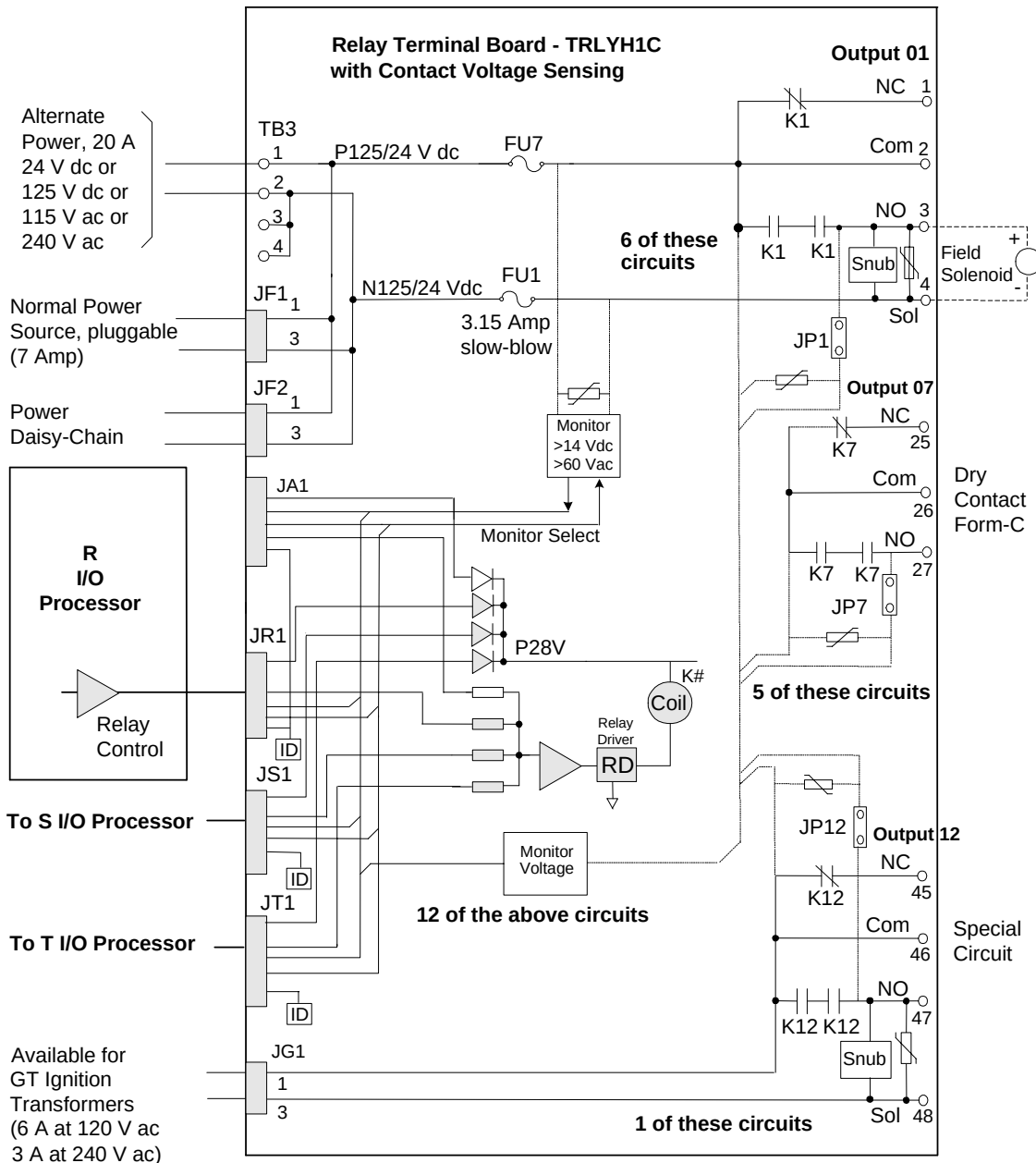
TRLYH1C Terminal Board Wiring

## Operation

Relay drivers, fuses, and jumpers are mounted on the TRLYH1C. Relays 1-6 have a 250 V MOV for transient suppression between the NO and power return terminals.

Relays are driven at the frame rate and have a 3.0 A rating. The rated contact-to-contact voltage is 500 V ac for one minute. The rated coil to contact voltage is 1,500 V ac for one minute. The typical time to operate is 10 ms. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O board is lost.

For simplex operation, a cable carries control signals and monitor feedback voltages between the I/O board and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O boards R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. The 28 V power for the relay coils comes in from all three I/O boards and is diode-shared. The following figure shows a TRLYH1C in a TMR system.



TRLYH1C Circuits

## Specifications

| Item                                       | Specifications                                                                                                                                                                                                     |
|--------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of relay channels on one TRLY board | 12: Six relays with solenoid driver voltages<br>Five relays with dry contacts only<br>One relay with 7 A rating                                                                                                    |
| Rated voltage on relays                    | a: Nominal 125 V dc or 24 V dc<br>b: Nominal 120 V ac or 240 V ac                                                                                                                                                  |
| Max load current                           | a: 0.6 A for 125 V dc operation<br>b: 3.0 A for 24 V dc operation<br>c: 3.0 A for 115/230 V ac, 50/60 Hz operation                                                                                                 |
| Max response time on                       | 25 ms typical                                                                                                                                                                                                      |
| Max response time off                      | 25 ms typical                                                                                                                                                                                                      |
| H1C contact feedback threshold             | 70-145 V dc, nominal 125 V dc, threshold 45 to 65 V dc<br>90-132 V rms, nominal 115 V rms, 47-63 Hz, threshold 45 to 72 V ac<br>190-264 V rms, nominal 230 V rms, 47-63 Hz, threshold 45 to 72 V ac                |
| H2C contact feedback threshold             | 16-32 V dc, nominal 24 V dc, threshold 10 to 16 V dc                                                                                                                                                               |
| Max response time off                      | 25 ms typical                                                                                                                                                                                                      |
| Contact material                           | Silver cad-oxide                                                                                                                                                                                                   |
| Contact life                               | Electrical operations: 100,000<br>Mechanical operations: 10,000,000                                                                                                                                                |
| Fault detection                            | Loss of relay excitation current<br>NO contact voltage disagreement with command<br>Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost |
| <b>Physical</b>                            |                                                                                                                                                                                                                    |
| Size                                       | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                                                                                                    |
| Temperature                                | -30 to + 65°C (-22 to 149 °F)                                                                                                                                                                                      |

## Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG\_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## **Configuration**

Board adjustments are made as follows:

- Jumpers JP1 through JP12. If contact voltage sensing is required, insert jumpers for selected relays.
- Fuses FU1 through FU12. If power is required for relays 1-6, two fuses should be placed in each power circuit supplying those relays. For example, FU1 and FU7 supply relay output 1. Refer to terminal board wiring diagram for more information.

---

## **TRLYH1D Relay Output with Solenoid Integrity Sensing**

### **Functional Description**

The Relay Output with Solenoid Integrity Sensing (TRLYH1D) terminal board holds six plug-in magnetic relays. The six relay circuits are Form-C contact outputs, powered and fused to drive external solenoids. A standard 24 V dc or 125 V dc source can be used. The board provides special feedback on each relay circuit to detect a bad external solenoid. Sensing is applied between the NO output terminal and the SOL output terminal.

TRLYH1D is similar to the standard TRLYH1B board except for the following:

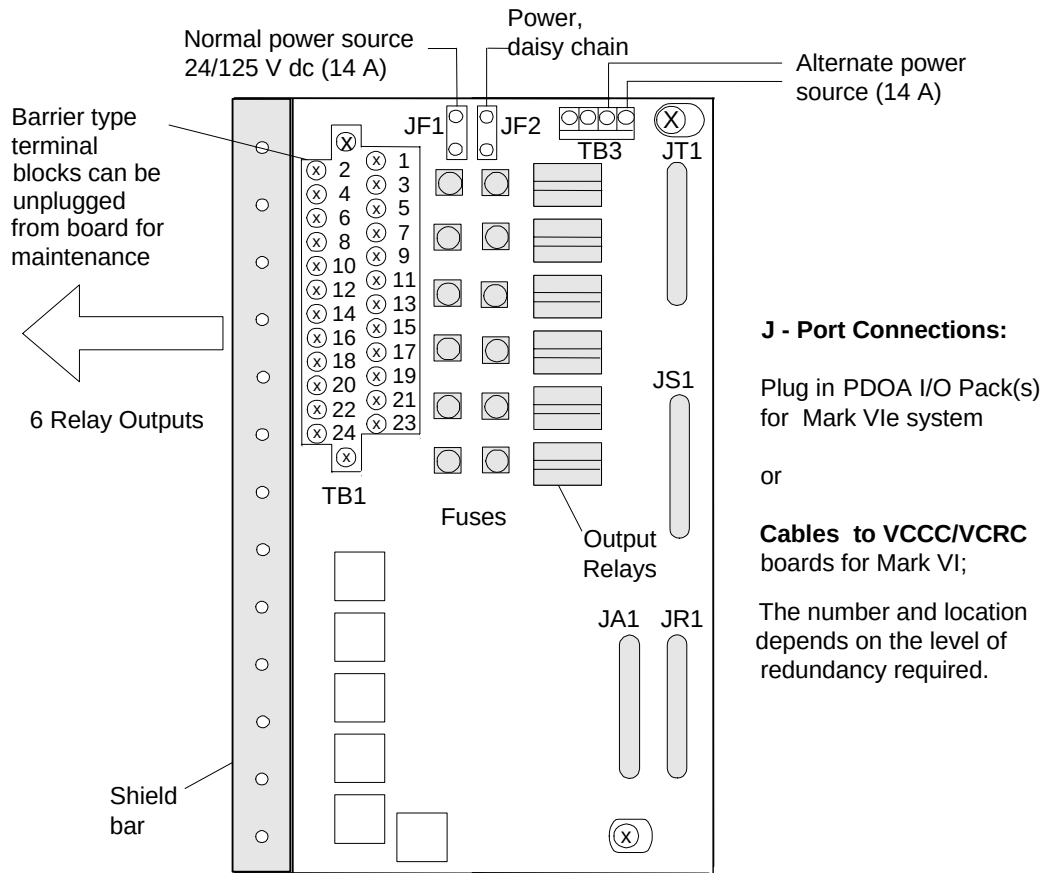
- There are only six relays.
- The board is designed for 24/125 V dc applications only.
- Relay circuits have a NO contact in the return side as well as the source side.
- The relays cannot be configured for dry contact use.
- Input relay coil monitoring is removed.
- The terminal board provides monitoring of field solenoid integrity.
- There is no special-use relay for driving an ignition transformer.

### **Mark VI Systems**

In the Mark\* VI systems, the TRLY is controlled by the VCCC or VCRC board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

## Mark VIe Systems

In the Mark VIe systems, the TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

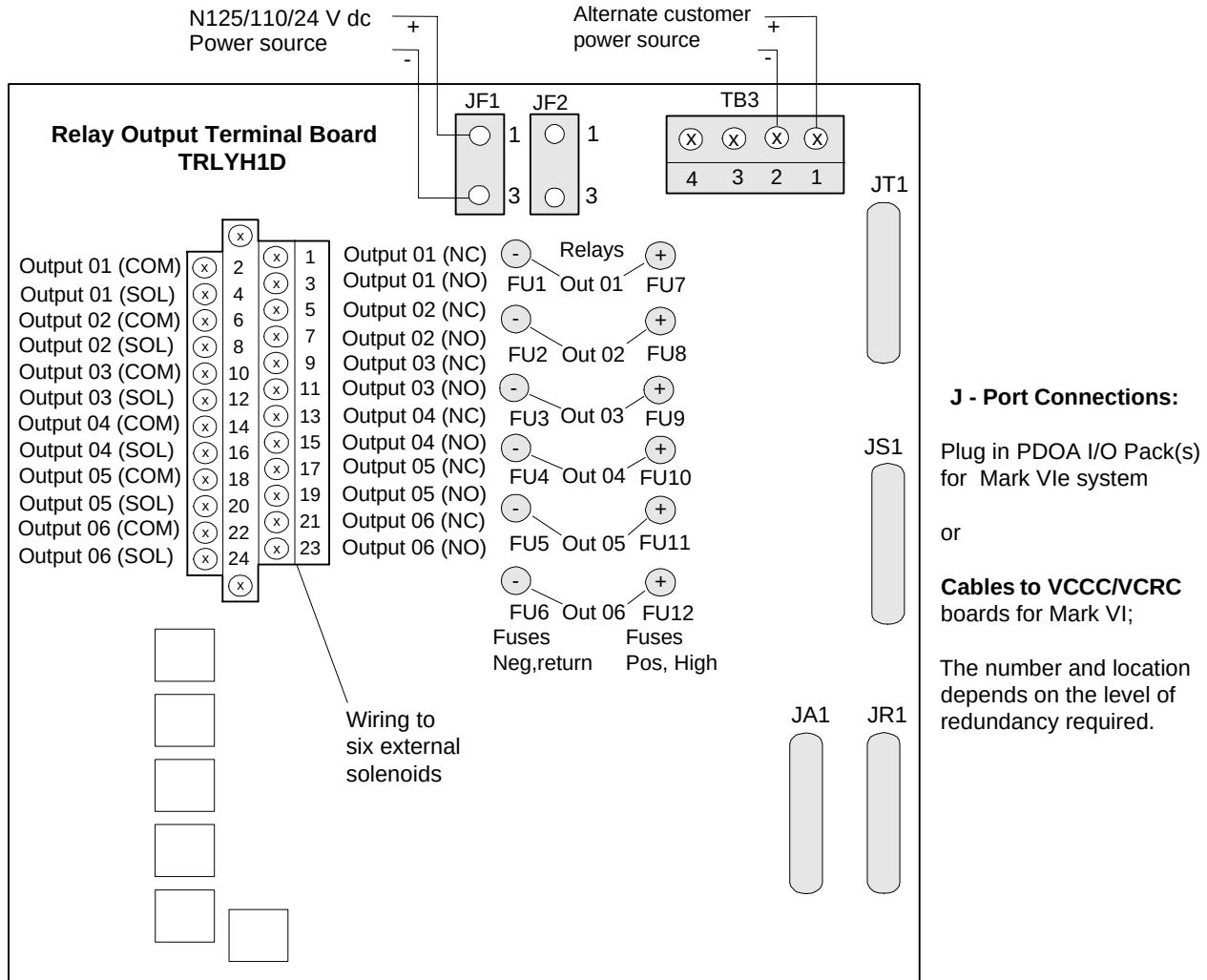


TRLYH1D Relay Output Terminal Board

## Installation

Connect the wires for the six relay outputs directly to the TB1 terminal block on the terminal board as shown in the figure, TRLYH1D Terminal Board Wiring. The block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip, attached to chassis ground, is located immediately to the left of the terminal block.

Connect the solenoid power for outputs 1-6 to JF1. JF2 can be used to daisy-chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used.

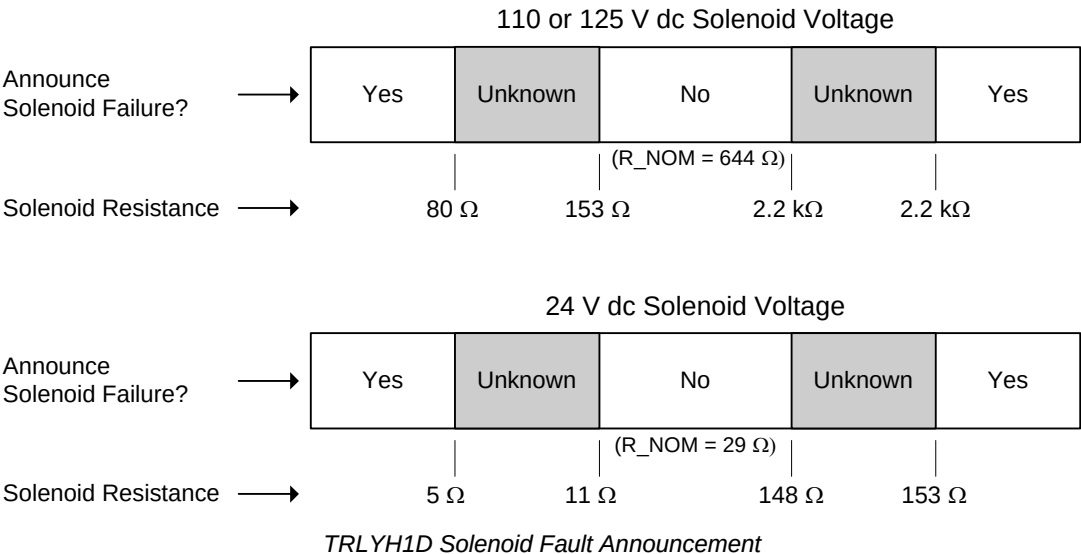


TRLYH1D Terminal Board Wiring

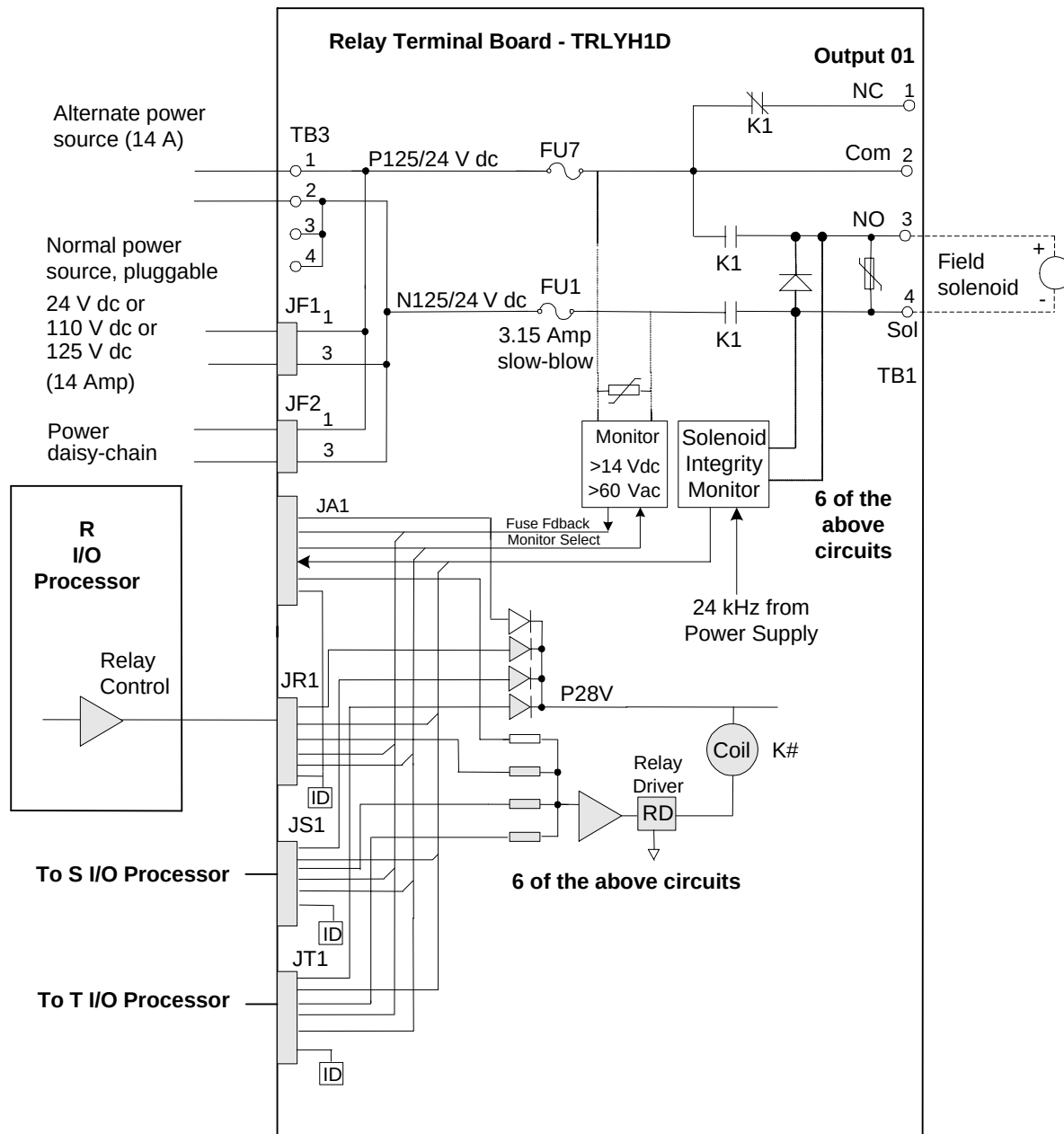
# Operation

The six relays have a MOV and clamp diode for transient suppression between the NO and power return terminals. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O board is lost.

TRL YH1D monitors each solenoid between the NO and SOL output terminals. When the relay is de-energized, the circuit applies a bias of less than 8% nominal voltage to determine if the load impedance is within an allowable band. If the impedance is too low or high for consecutive scans, an alarm feedback is generated. The contacts must be open for at least 1.3 seconds to get a valid reading.



For simplex operation, cables carry control signals and solenoid monitoring feedback voltages between the I/O board and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O processor boards R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay coils comes in from all three I/O boards and is diode-shared. The following figure shows TRLYH1D in a TMR system.



TRLYH1D Circuits, TMR System



## Specifications

| Item                                      | Specification                                                                                                                                                                                                                                       |
|-------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of relay channels                  | Six relays with special customer solenoid monitoring                                                                                                                                                                                                |
| Rated voltage on relays                   | Nominal 125 V dc or 24 V dc                                                                                                                                                                                                                         |
| Relay contact rating for 24 V dc voltage  | Current rating 10 A, resistive<br>Current rating 2 A, L/R = 7 ms, without suppression                                                                                                                                                               |
| Relay contact rating for 125 V dc voltage | Current rating 0.5 A, resistive<br>Current rating 0.2 A, L/R = 7 ms, without suppression<br>Current rating 0.65 A, L/R = 150 ms, with suppression (MOV) across the load                                                                             |
| Maximum response time on                  | 25 ms typical                                                                                                                                                                                                                                       |
| Maximum response time off                 | 25 ms typical                                                                                                                                                                                                                                       |
| Contact life                              | Electrical operations: 100,000                                                                                                                                                                                                                      |
| Board size                                | 17.8 cm by 33.0 cm (7 in by 13 in)                                                                                                                                                                                                                  |
| Fault detection                           | Loss of solenoid voltage supply (fuse monitor)<br>Solenoid resistance measured to detect open and short circuits<br>Unplugged cable or loss of communication with I/O board (relays de-energize if communication with associated I/O board is lost) |
| <b>Physical</b>                           |                                                                                                                                                                                                                                                     |
| Size                                      | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                                                                                                                                     |
| Temperature                               | -30 to +65°C (-22 to +149 °F)                                                                                                                                                                                                                       |

## Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG\_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

There are no jumpers or hardware settings on the board.

---

# **TRLYH1E Solid-State Relay Output**

## ***Functional Description***

The solid-state Relay Output (TRLYH1E) terminal board is a 12-output relay board using solid-state relays for the outputs and featuring isolated output voltage feedback on all 12 circuits. The solid-state relays allow the board to be certified for Class 1 Division 2 applications. The use of solid-state relays requires three different board types:

- TRLYH1E for 115 V ac applications
- TRLYH2E for 24 V dc applications
- TRLYH3E for 125 V dc applications

Unlike the form-C contacts provided on the mechanical relay boards, all 12 outputs on TRLYH1E are single, NO, contacts. There is no user solenoid power distribution on the board.

## ***Mark VI Systems***

In the Mark\* VI system, the TRLY is controlled by the VCCC or VCRC board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

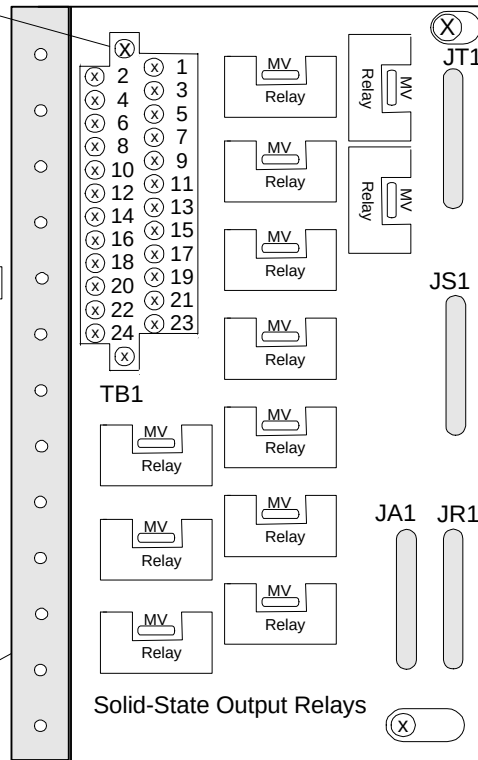
## ***Mark VIe Systems***

In the Mark VIe system, the TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Barrier type  
terminal blocks can  
be unplugged from  
board for  
maintenance

12 Relay Outputs

Shield  
bar



#### J - Port Connections:

Plug in PDOA I/O Pack(s)  
for Mark VIe system

or

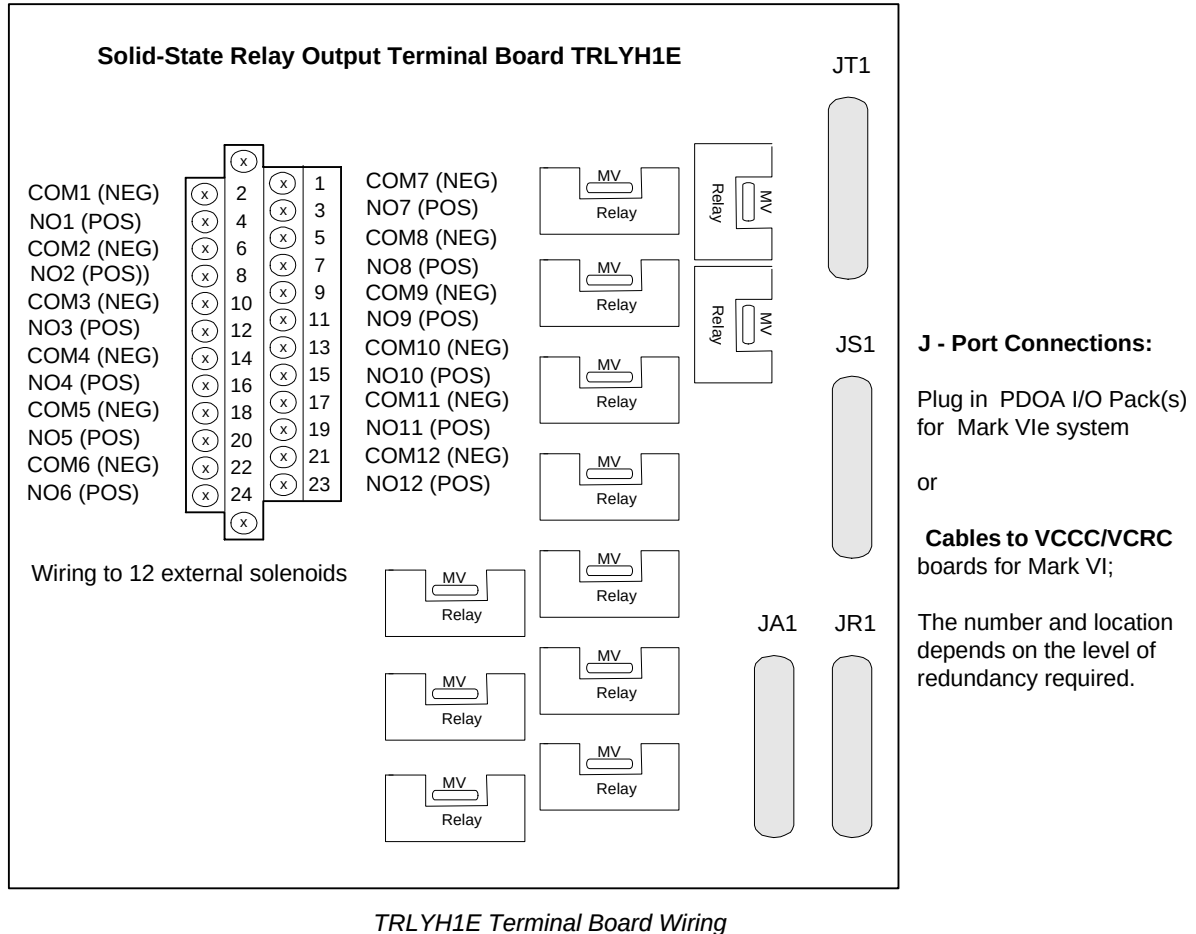
**Cables to VCCC/VCRC**  
boards for Mark VI;

The number and location  
depends on the level of  
redundancy required.

*TRLYH1E Solid-State Relay Output Terminal Board*

## Installation

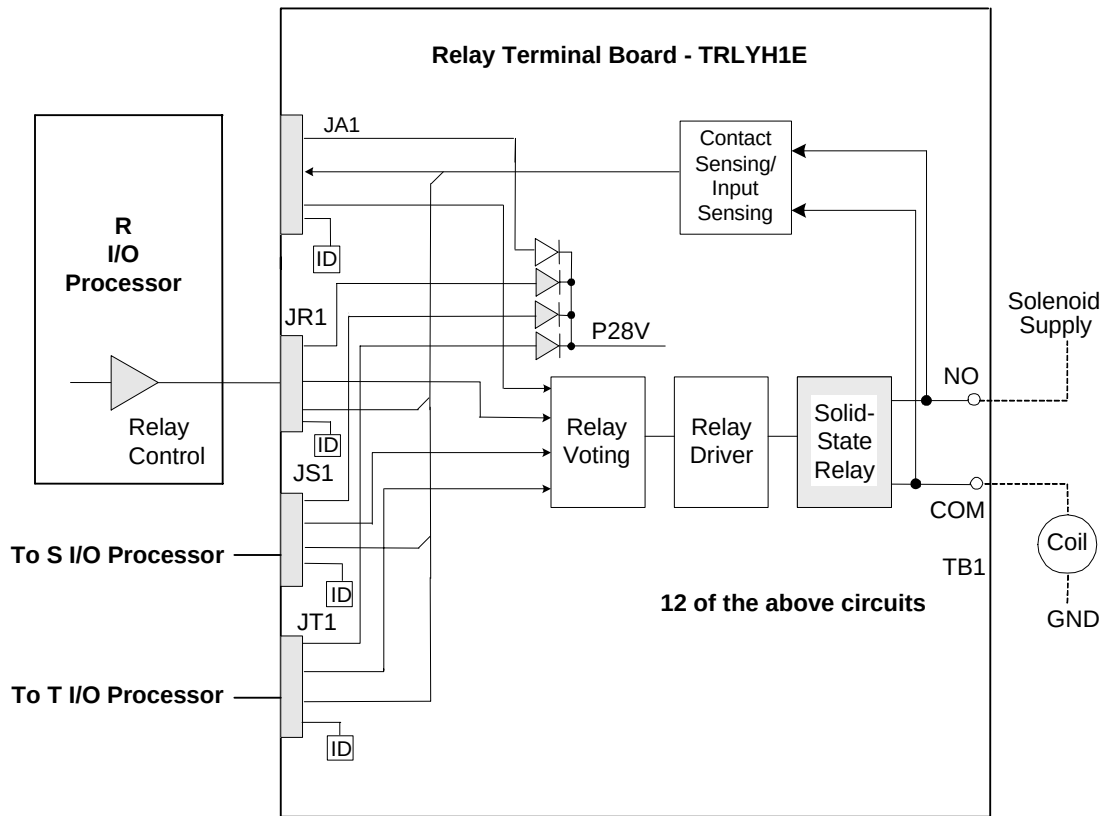
Connect the wires for the 12 solenoids directly to the I/O terminal block on the terminal board as shown in the figure, *TRLYH1E Terminal Board Wiring*. The terminal block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. The dc relays are unidirectional, so care should be taken about polarity when connecting load to these relays. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block. The solenoids must be powered externally by the customer.



## Operation

NO solid-state relays, relay drivers, and output monitoring are mounted on TRLYH1E. During power up, relays stay de-energized while connected to any control. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O processor is lost.

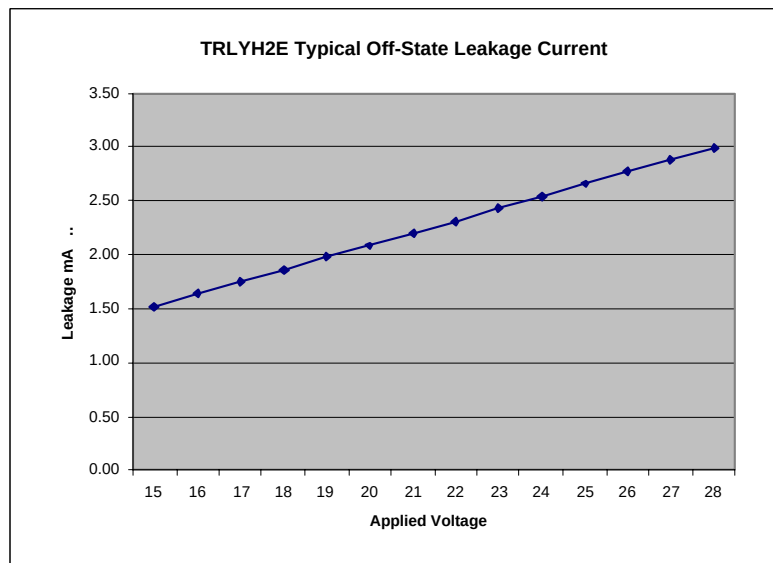
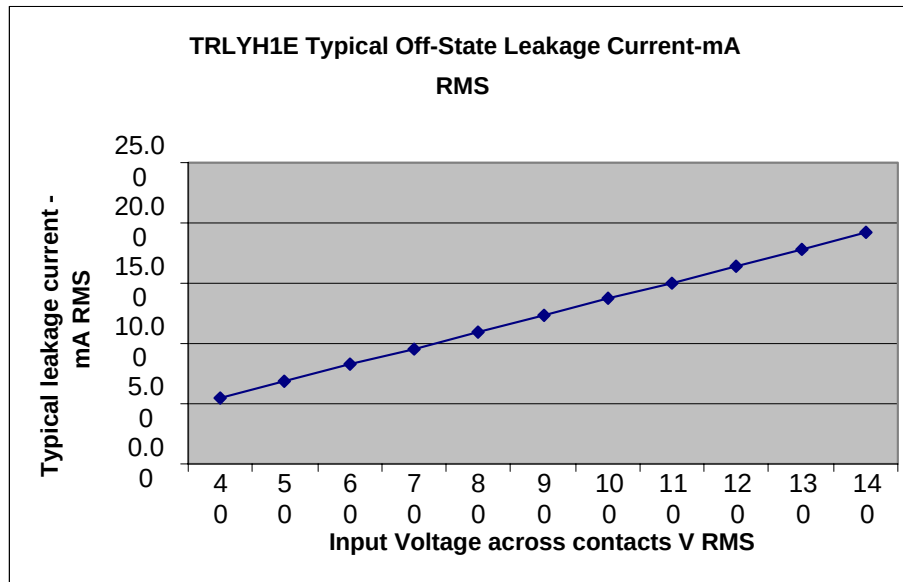
For simplex operation, control signals and relay output voltage feedback signals pass between the I/O processor and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay drivers comes in from all three I/O processors and is diode-shared. The following figure shows TRLYH1E in a TMR system.

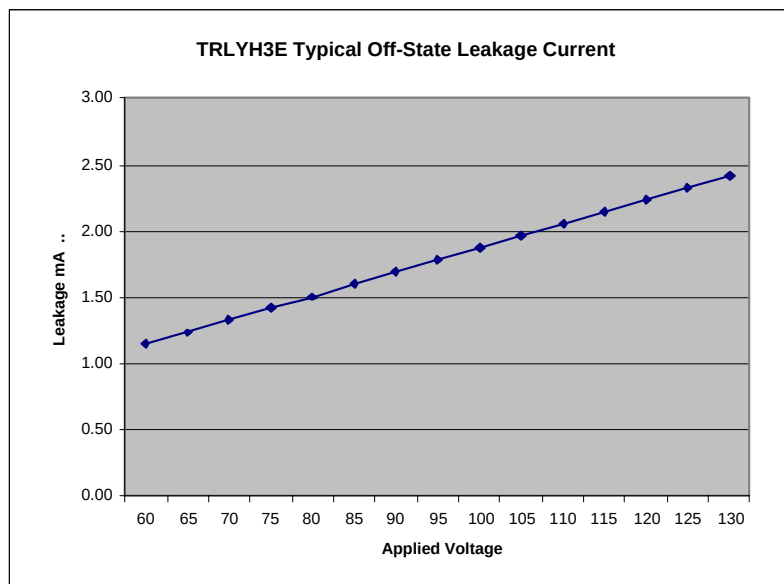


TRLYH1E Circuits, TMR System

## Contact Voltage Feedback

In TRLYH1E, isolated feedback of voltage sensing is connected to the relay outputs. This allows the control to observe the voltage across the relay outputs without a galvanic connection. One contact sensing circuit is provided with each relay. This feature is similar to the voltage sensing on TRLYH1C but with simpler hardware. The voltage sensing circuit allows a small leakage current to pass to power the isolated circuit. The typical leakage current is the sum of the leakage through the turned off solid-state relay and the current through the voltage sensing circuit. The following charts indicate the typical leakage current as a function of the applied voltage for the three board types.





Due to the permitted leakage current, the board may give false indications if used in series with a low input current load, including common contact input circuits such as those found on TBCI or STCI. To ensure correct operation, the maximum load resistances for the three board types are as follows:

- TRLYH1E: Maximum load resistance at nominal 115 V ac is 2.5 k $\Omega$ .
- TRLYH2E: Maximum load resistance at nominal 24 V dc is 4.5 k $\Omega$ .
- TRLYH3E: Maximum load resistance at nominal 125 V dc is 25 k $\Omega$ .

Load resistance may be decreased by applying a resistor in parallel with the load so the parallel combination satisfies the maximum resistance requirement.

## Contact Voltage Rating

Solid-state relays have a finite transient voltage capability and require coordinated voltage protection. TRLYH1E for ac applications uses a load control device that turns off on a current zero crossing. This turn-off characteristic ensures that no inductive energy is present in the load at turn-off time. Basic protection of the ac relay is provided on TRLYH1E using a MOV with clamp voltage coordinated with relay voltage rating. In addition, there is an R-C snubber circuit on the relay output using a 56  $\Omega$  resistor in series with a 0.25  $\mu$ F capacitor.

Both the TRLYH2E (for 24 V dc applications) and the TRLYH3E (for 125 V dc applications) can interrupt currents in large inductive loads. Because a wide range of loads may be encountered, an appropriate R-C or diode snubber circuit must be selected for each application. The snubber should be applied at the load device using common engineering practices. If the applied snubber does not fully control inductive switching voltage transients, both board versions contain an active voltage clamp circuit. This circuit activates at approximately 50-55 V dc for the H2E and at approximately 164-170 V dc for the H3E (both values below the rating of the relay). While the clamp circuit has a finite ability to absorb energy, it can handle the wiring inductance of a resistive load.

## Specifications

| Item                                                                             | Specification                                                                                                                                                                                                                                                                                                                       |
|----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of relay channels on one TRLY board                                       | 12 relays: 115 V ac operation with TRLYH1E<br>24 V dc operation with TRLYH2E<br>125 V dc operation with TRLYH3E                                                                                                                                                                                                                     |
| Maximum operating voltage and maximum load current with free convection air flow | 1E: 250 V rms at 47-63 Hz. 10 A @25°C (77 °F) maximum<br>de-rate current linearly to 6 A @ 65°C (149 °F) maximum<br>2E: 28 V dc 10 A dc @40°C (104 °F) maximum<br>de-rate current linearly to 7 A dc @65°C (149 °F) maximum<br>3E: 140 V dc 3 A dc@40°C (104 °F)maximum<br>de-rate current linearly to 2 A dc @65°C (149 °F)maximum |
| Maximum off state leakage (see charts of leakage vs. applied voltage)            | 1E: 3 mA rms<br>2E: 3 mA A dc at 55 V<br>3E: 2.5 mA A dc                                                                                                                                                                                                                                                                            |
| Max response time on                                                             | 1 ms for dc relays; ½ cycle for ac relay                                                                                                                                                                                                                                                                                            |
| Max response time off                                                            | 300 micro seconds for dc relays; ½ cycle for ac relay                                                                                                                                                                                                                                                                               |
| Relay MTBF                                                                       | 1E: 50 years<br>2E: 37 years<br>3E: 47 years                                                                                                                                                                                                                                                                                        |
| Relay contact voltage sensing threshold                                          | 1E: 115 V ac 70 V ±10% ac rms<br>2E: 24 V dc 15 V ±2 V dc<br>3E: 125 V dc 79 V ±10% dc                                                                                                                                                                                                                                              |
| Operating temperature range                                                      | -30 to 65°C (-22 to +149 °F)                                                                                                                                                                                                                                                                                                        |
| Operating humidity                                                               | 5 to 95% non-condensing                                                                                                                                                                                                                                                                                                             |
| Fault detection                                                                  | Relay current disagreement with command<br>Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost                                                                                                                                                           |
| <b>Physical</b>                                                                  |                                                                                                                                                                                                                                                                                                                                     |
| Size                                                                             | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                                                                                                                                                                                                                     |
| Temperature                                                                      | -30 to + 65°C (-22 to +149 °F)                                                                                                                                                                                                                                                                                                      |



## ***Diagnostics***

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG\_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## ***Configuration***

There are no jumpers or hardware settings on the board.

---

# ***TRL YH1F Relay Output with TMR Contact Voting***

## ***Functional Description***

The Relay Output with TMR contact voting (TRL YH1F) terminal board provides 12 contact-voted relay outputs. The board holds 12 sealed relays in each TMR section, for a total of 36 relays. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact. 24/125 V dc or 115 V ac can be applied.

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**Note** TRL YH1F and H2F do not support simplex arrangements

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TRL YH1F does not have power distribution. However, an optional power distribution board, IS200WPDFH1A, can be added so that a standard 125 V dc or 115 V ac source, or an optional 24 V dc source with individual fuses, can be provided for field solenoid power.

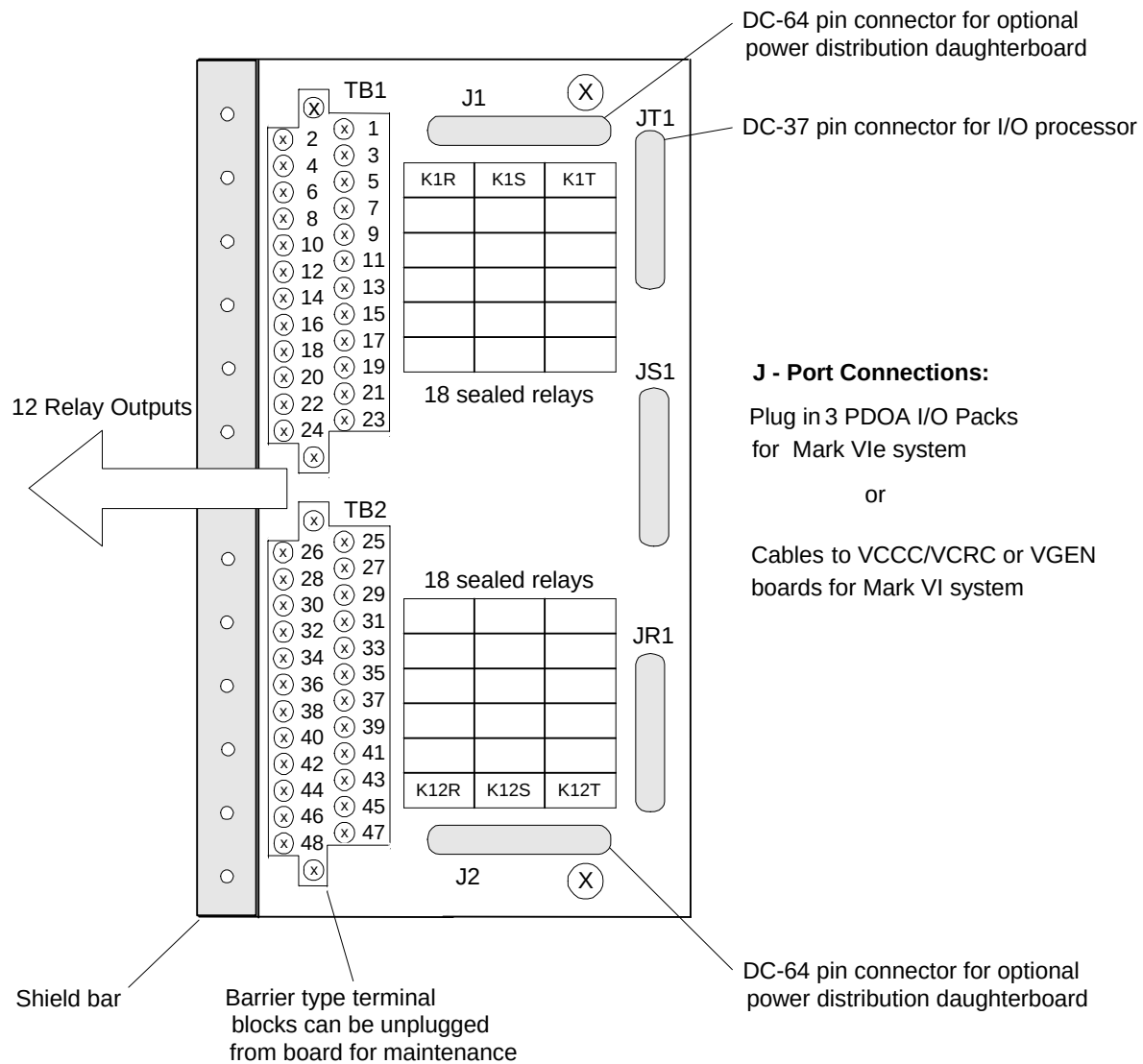
TRL YH2F is same as TRL YH1F except that the voted contacts form a Form B (NC) output. Both boards can be used in Class 1 Division 2 applications.

## ***Mark VI Systems***

In the Mark\* VI system, the TRL Y is controlled by the VCCC, VCRC, or VGEN board and only supports TMR applications. Cables with molded plugs connect JR1, JS1, and JT1 to the VME rack where the I/O boards are mounted.

## Mark VIe Systems

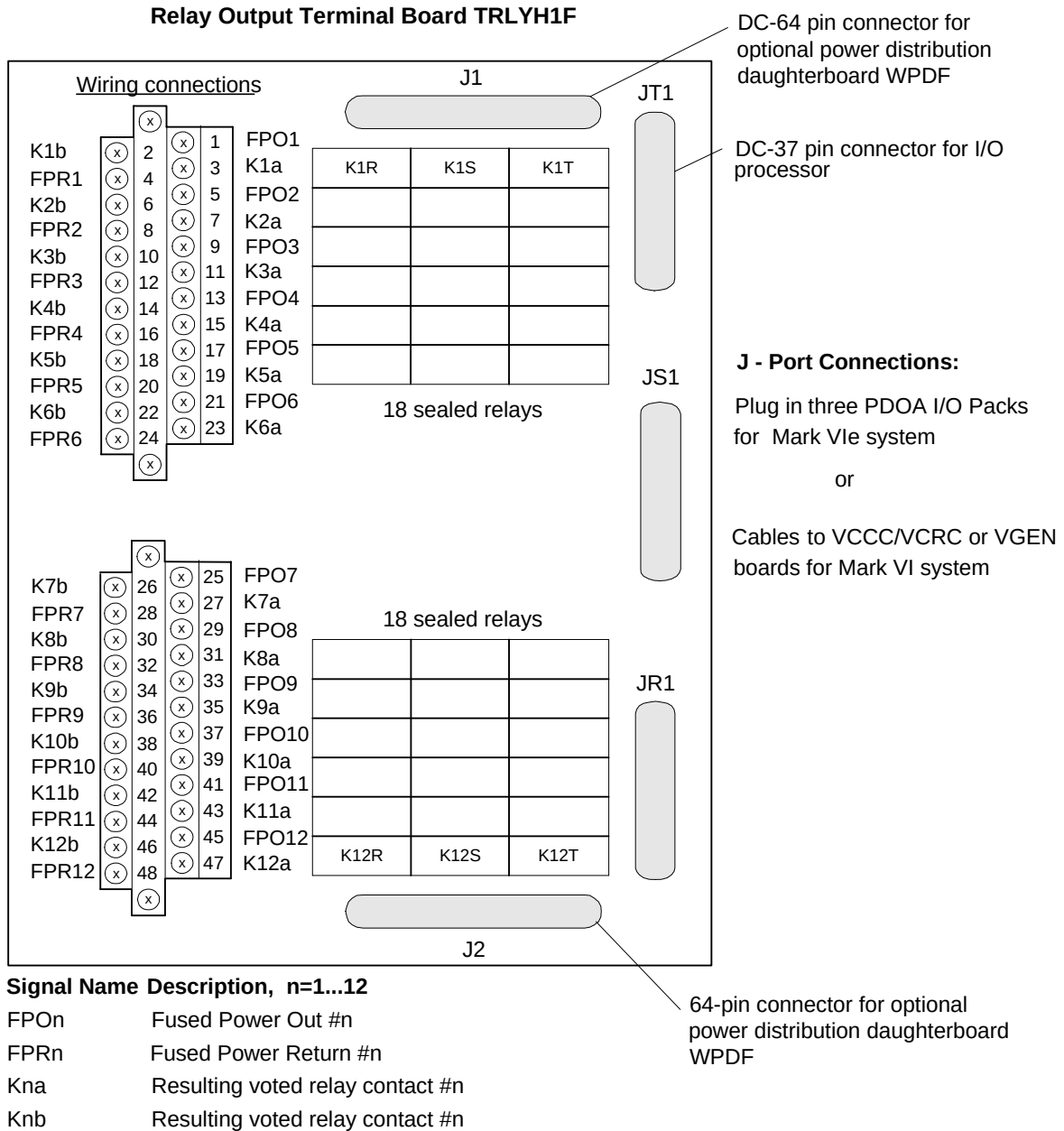
In the Mark VIe system, the TRLY works with PDOA I/O pack and only supports TMR applications. Three TMR PDOA packs plug into the JR1, JS1, and JT1 37-pin D-type connectors on the terminal board.



TRLYH1F Relay Output Terminal Board

## Installation

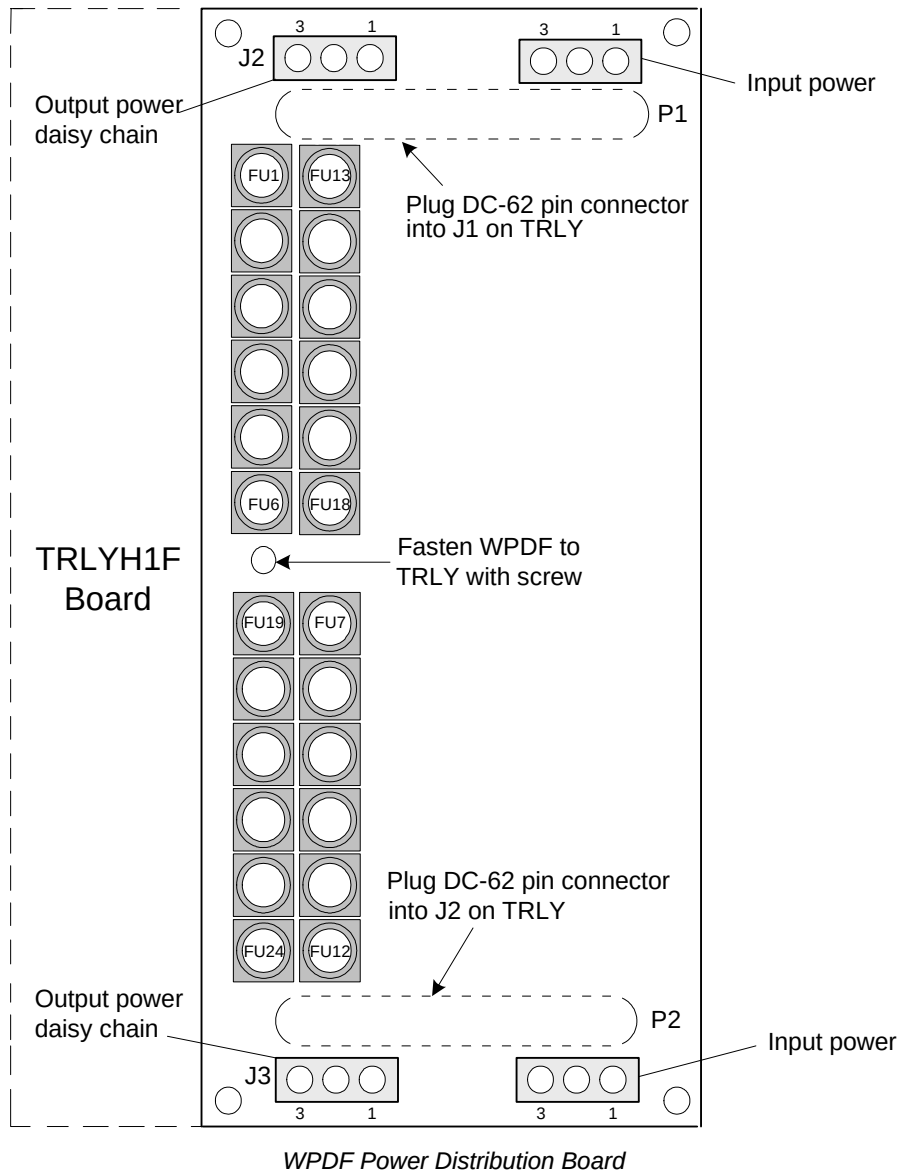
Connect the wires for the 12 solenoids directly to two I/O terminal blocks on the terminal board as shown in the following figure, *TRLYH1F Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left side of each terminal block. Solenoid power for outputs 1-12 is available if the WPDF daughterboard is used. Alternatively, power can be wired directly to the terminal block.



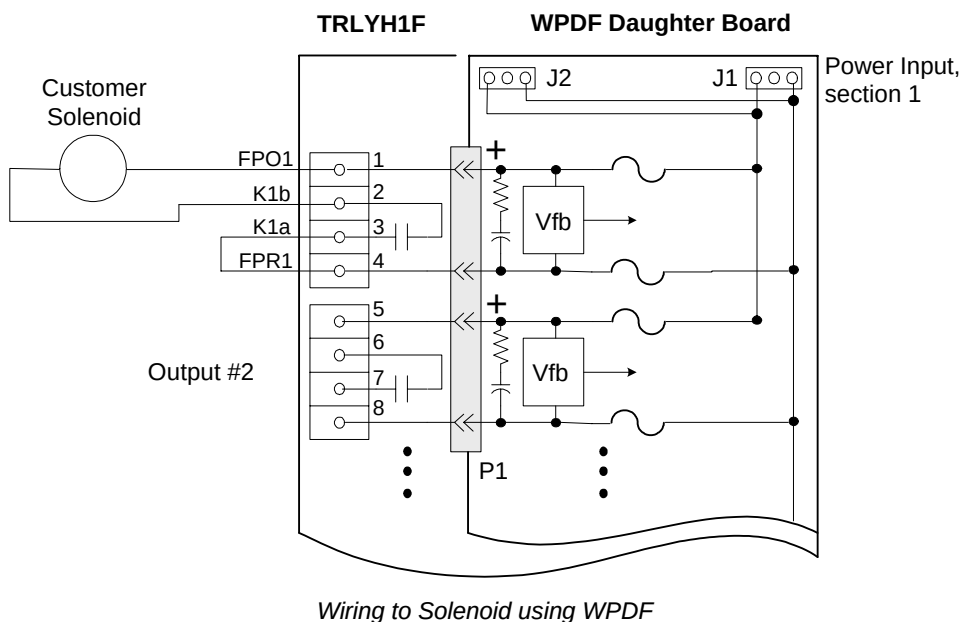
*TRLYH1F Terminal Board Wiring*

## Power Distribution Board

If using the optional WPDF power distribution board, mount it on top of TRLY on the J1 and J2 connectors. Secure WPDF to TRLY by fastening a screw in the hole located at the center of WPDF. Connect the power for the two sections of the board on the three-pin connectors J1 and J4. Power can be daisy-chained out through the adjacent plugs, J2 and J3.



The solenoids must be wired as shown in the following figure. If WPDF is not used, the customer must supply power to the solenoids.



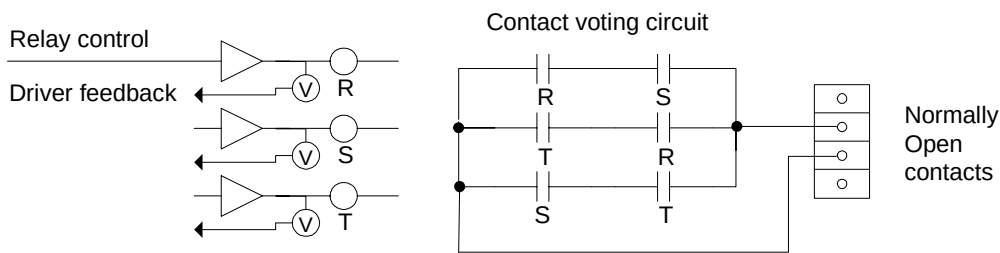
## Operation

The 28 V dc power for the terminal board relay coils and logic comes from the three I/O processors connected at JR1, JS1, and JT1. The same relays are used for ac voltages and dc voltages, as specified in the *Specifications* section. H1F and H2F use the same relays with differing circuits.

Relay drivers are mounted on the TRLYH1F and drive the relays at the frame rate. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O board or I/O pack is lost.

This board only supports TMR applications. The relay control signals are routed into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals directly control the corresponding relay driver for each TMR section R, S, and T. Power for each section's relay coils comes in from its own I/O processor and is not shared with the other sections.

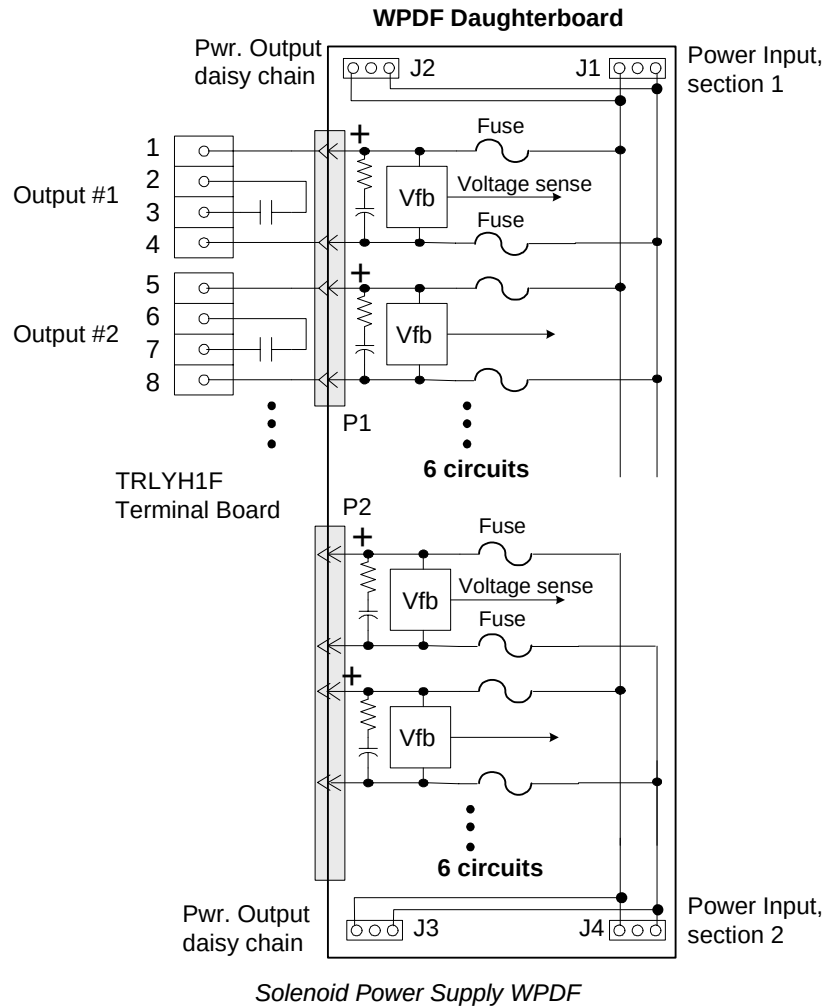
TRLYH1F features TMR contact voting. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact. 24/125 V dc or 115 V ac can be applied. TRLYH2F is the same except that the voted contacts form a Form B (NC) output. The following figure shows TMR voting contact circuit.



## Field Solenoid Power Option

The WPDFH1A daughterboard supplies power to TRLYH#F to power solenoids. WPDF holds two power distribution circuits, which can be independently used for standard 125 V dc, 115 V ac, or 24 V dc sources. Each section consists of six fused branches that provide power to TRLYH#F. Each branch has its own voltage monitor across its secondary fuse pair. Each voltage detector is fanned to three independent open-collector drivers for feedback to each of the I/O processors R, S, and T.

WPDF should not be used without TRLYH#F. Fused power flows through this board down to the TRLY terminal board points. TRLY controls the fuse power feedback. The following figure shows TRLYH1F/WPDF solenoid power circuit.



## **Specifications**

| <b>Item</b>                                   | <b>Specification</b>                                                                                                                                                                                                                |
|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of output relay channels               | 12                                                                                                                                                                                                                                  |
| Board types                                   | H1F: NO contacts<br>H2F: NC contacts                                                                                                                                                                                                |
| Rated voltage on relays                       | a: Nominal 100/125 V dc or 24 V dc<br>b: Nominal 115 V ac                                                                                                                                                                           |
| Maximum load current                          | a: 0.5/0.3 A resistive for 100/125 V dc operation<br>b: 5.0 A resistive for 24 V dc operation<br>c: 5.0 A resistive for 115 V ac                                                                                                    |
| Maximum response time on                      | 25 ms                                                                                                                                                                                                                               |
| Contact life                                  | Electrical operations: 100,000                                                                                                                                                                                                      |
| Fault detection                               | Coil Voltage disagreement with command<br>Blown fuse indication (with WPDF power daughterboard).<br>Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost. |
| <b>WPDF Solenoid Power Distribution Board</b> |                                                                                                                                                                                                                                     |
| Number of Power Distribution Circuits (PDC)   | 2: Each rated 10 A, nominal 115 V ac or 125 V dc.                                                                                                                                                                                   |
| Number of Fused Branches                      | 12: 6 for each PDC                                                                                                                                                                                                                  |
| Fuse rating                                   | 3.15 A at 25°C (77 °F)<br>2.36 A – recommended maximum usage at 65°C (149 °F)                                                                                                                                                       |
| Voltage monitor, maximum response delay       | 60 ms typical                                                                                                                                                                                                                       |
| Voltage monitor, minimum detection voltage    | 16 V dc<br>72 V ac                                                                                                                                                                                                                  |
| Voltage monitor, max current (leakage)        | 3 mA                                                                                                                                                                                                                                |
| <b>Physical</b>                               |                                                                                                                                                                                                                                     |
| Size - TRLY                                   | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                                                                                                                     |
| Size - WPDF                                   | 10.16 cm wide x 33.02 cm high (4.0 in x 13.0 in)                                                                                                                                                                                    |
| Temperature                                   | -30 to + 65°C (-22 to +149 °F)                                                                                                                                                                                                      |
| Technology                                    | Surface-mount                                                                                                                                                                                                                       |

## ***Diagnostics***

Diagnostic tests to components on the terminal boards are as follows:

- The voltage to each relay coil is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The voltage across each solenoid power supply is monitored and if it goes below 16 V ac/dc, an alarm is created.
- If any one of the outputs goes unhealthy a composite diagnostic alarm, L3DIAG\_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location.

Details of the individual diagnostics are available from the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## ***Configuration***

There are no jumpers or hardware settings on the board.

---

# ***SRLY Simplex Relay Output***

## ***Functional Description***

The Simplex Relay Output (SRLY) terminal board is a simplex S-type terminal board accepting a PDOA I/O pack and providing 12 form C relay output circuits through 48 customer terminals.

SRLY has the same physical size, customer terminal locations, and I/O pack mounting as other S-type terminal boards. There will be no components higher than an attached PDOA I/O pack, permitting double stacking of terminal boards.

SRLY has two groups:

- IS200SRLYH1 has fixed Euro-style box terminals and no ability to accept option boards.
- IS200SRLYH2 has pluggable Euro-style box terminals and two connectors that accept a variety of different option boards.

Each relay on SRLY uses an isolated contact pair as position feedback to PDOA.

There are three option boards available that plug on to SRLYH2A:

- IS200WROB turns SRLY into the functional equivalent of IS200TRLYH1B. This option provides fused and sensed power distribution to the first six relays and dedicated power to the last relay.
- IS200WROF puts a single fuse in series with each relay common connection. Fuse voltage feedback is included.
- IS200WROG distributes power from an input connector to each relay through a single fuse. Fuse voltage feedback is included.

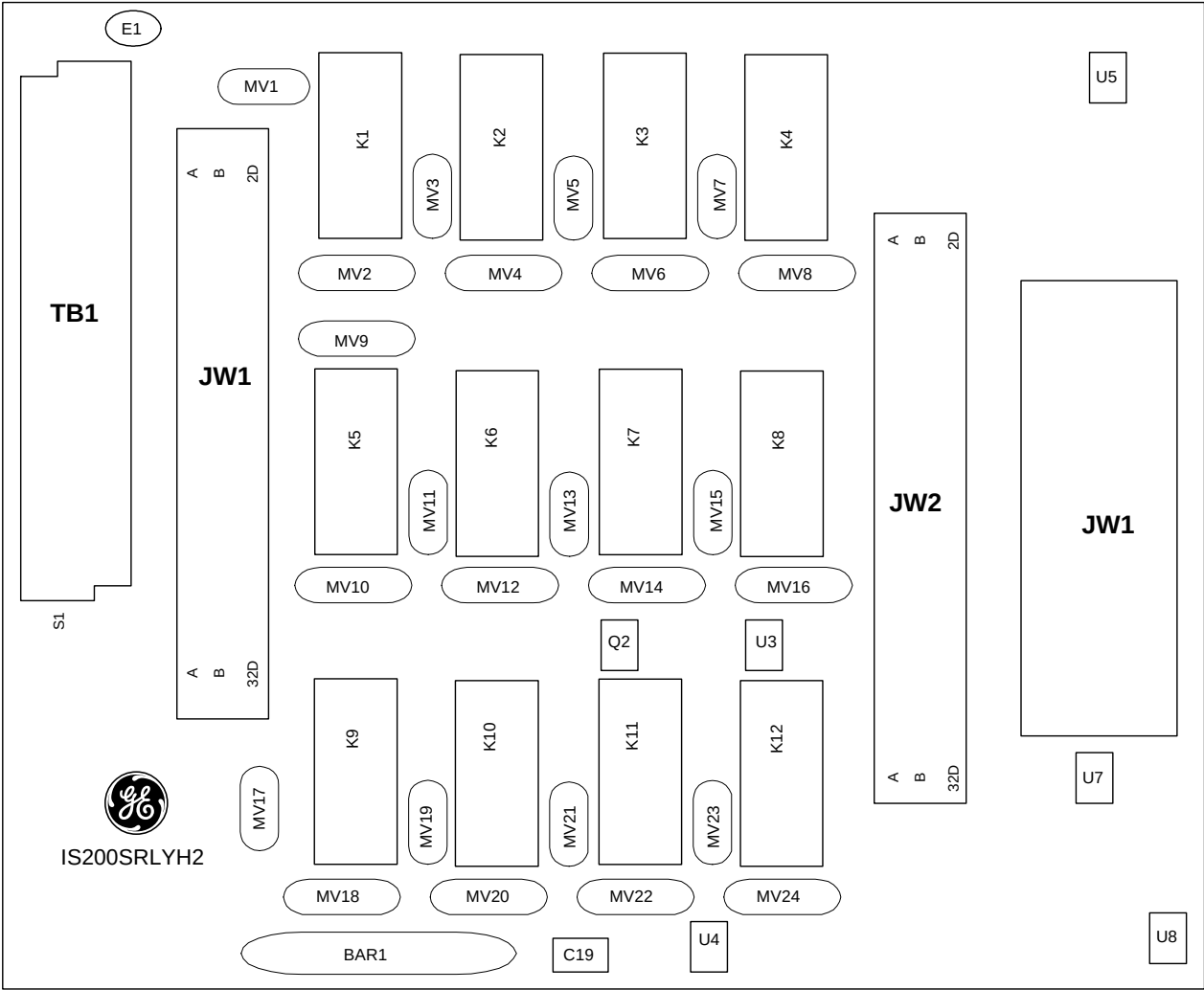


## Installation

SRLY and a plastic insulator mounts on a sheet metal carrier and is then mounted to a cabinet by screws. If an option board is used, it plugs onto SRLYH2A and is held in place by the force of the connectors. The following table identifies the function of each terminal point as it relates to the presence of an option board.

| Output Terminal | Relay | SRLY | SRLY + WROB | SRLY/WROF with Fuses | SRLY/WROF without Fuses | SRLY + WROG |
|-----------------|-------|------|-------------|----------------------|-------------------------|-------------|
| 1               | 1     | NC   | NC          | NC                   | NC                      | NC          |
| 2               |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 3               |       | NO   | NO          | NO                   | NO                      | NO          |
| 4               |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 5               | 2     | NC   | NC          | NC                   | NC                      | NC          |
| 6               |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 7               |       | NO   | NO          | NO                   | NO                      | NO          |
| 8               |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 9               | 3     | NC   | NC          | NC                   | NC                      | NC          |
| 10              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 11              |       | NO   | NO          | NO                   | NO                      | NO          |
| 12              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 13              | 4     | NC   | NC          | NC                   | NC                      | NC          |
| 14              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 15              |       | NO   | NO          | NO                   | NO                      | NO          |
| 16              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 17              | 5     | NC   | NC          | NC                   | NC                      | NC          |
| 18              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 19              |       | NO   | NO          | NO                   | NO                      | NO          |
| 20              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 21              | 6     | NC   | NC          | NC                   | NC                      | NC          |
| 22              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 23              |       | NO   | NO          | NO                   | NO                      | NO          |
| 24              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |
| 25              | 7     | NC   | NC          | NC                   | NC                      | NC          |
| 26              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 27              |       | NO   | NO          | NO                   | NO                      | NO          |
| 28              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 29              | 8     | NC   | NC          | NC                   | NC                      | NC          |
| 30              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 31              |       | NO   | NO          | NO                   | NO                      | NO          |
| 32              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 33              | 9     | NC   | NC          | NC                   | NC                      | NC          |
| 34              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 35              |       | NO   | NO          | NO                   | NO                      | NO          |
| 36              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 37              | 10    | NC   | NC          | NC                   | NC                      | NC          |
| 38              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 39              |       | NO   | NO          | NO                   | NO                      | NO          |

| Output Terminal | Relay | SRLY | SRLY + WROB | SRLY/WROF with Fuses | SRLY/WROF without Fuses | SRLY + WROG |
|-----------------|-------|------|-------------|----------------------|-------------------------|-------------|
| 40              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 41              | 11    | NC   | NC          | NC                   | NC                      | NC          |
| 42              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 43              |       | NO   | NO          | NO                   | NO                      | NO          |
| 44              |       |      |             | COM (fused)          | VSENSE                  | RETURN      |
| 45              | 12    | NC   | NC          | NC                   | NC                      | NC          |
| 46              |       | COM  | COM         | COM (unfused)        | COM                     | POWER       |
| 47              |       | NO   | NO          | NO                   | NO                      | NO          |
| 48              |       |      | SOL         | COM (fused)          | VSENSE                  | RETURN      |

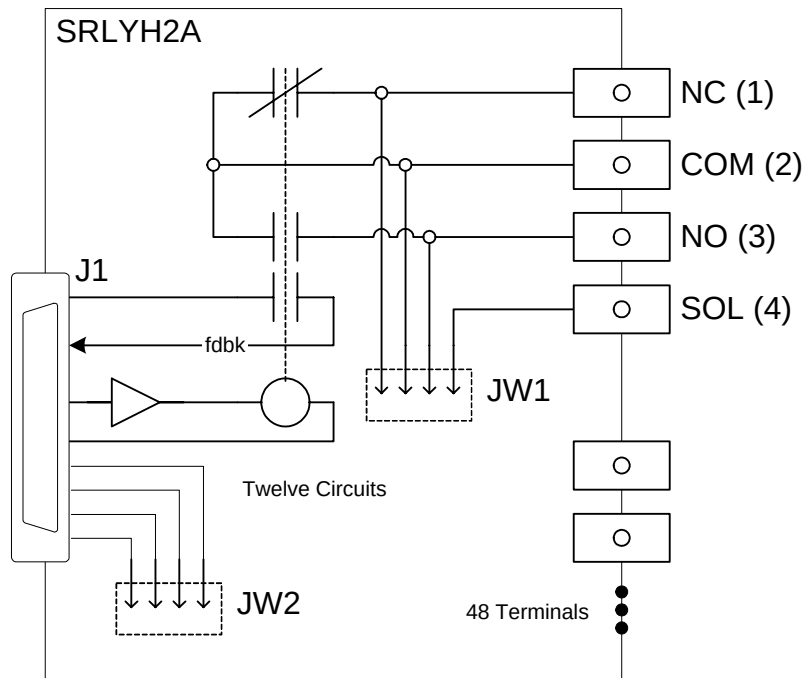


SRLY Terminal Board Layout

## Operation

### Board Groups

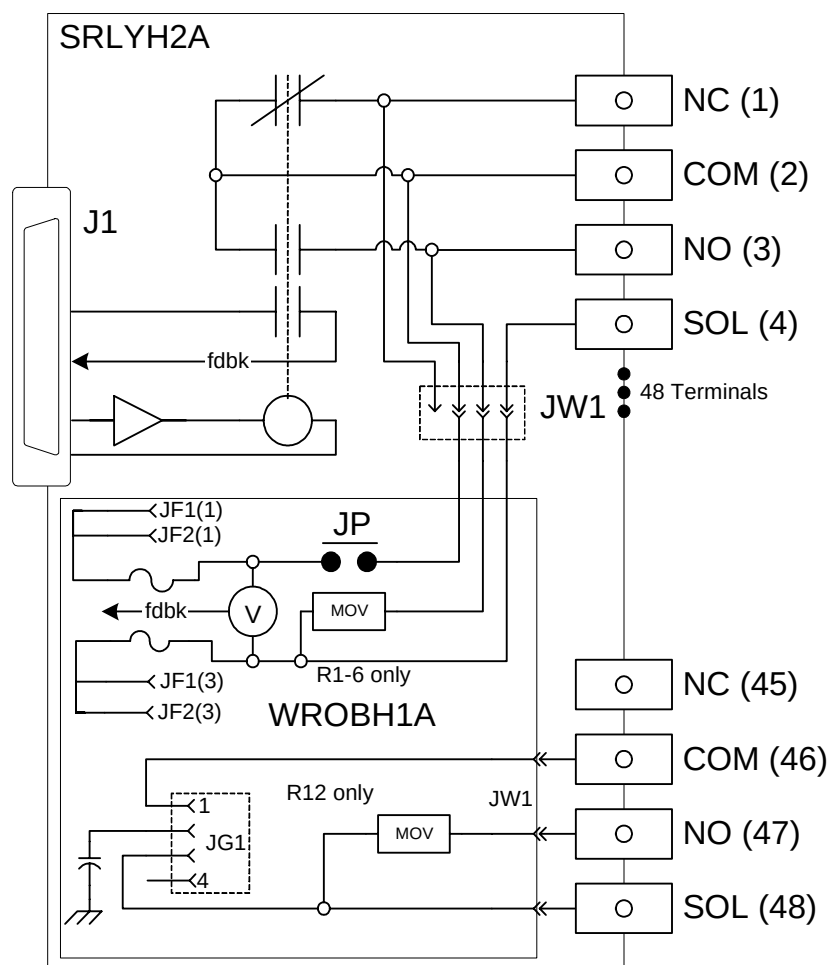
SRLY is available in two groups. SRLYH1 comes with fixed box terminals and omits option board connectors JW1 and JW2. SRLYH2 uses pluggable type terminals and has connectors JW1 and JW2 supporting option board connection. Electrically SRLYH2 has the following circuit for each of the 12 relays:



Without an option board, the SOL terminal associated with each relay has no connection. SRLY is designed to support a current rating of 5 A and voltage clearance greater than is needed for 250 V ac on all customer screw and JW1 circuits. The relay rating is the limiting item for each application.

## SRLY + WROB

Option board IS200WROBH1A adds capability to SRLYH2 to yield a combination that has the same functionality as an IS200TRLYH1B terminal board when used simplex. Included are fused sensed power distribution to the first six relays and dedicated power to the last relay. Electrically IS200SRLYH2 plus IS200WROBH1 has the following circuit. IS200WROBH1 has default fuse values of 3.15 A. Connector JW2 and its connections to J1 are omitted for clarity.



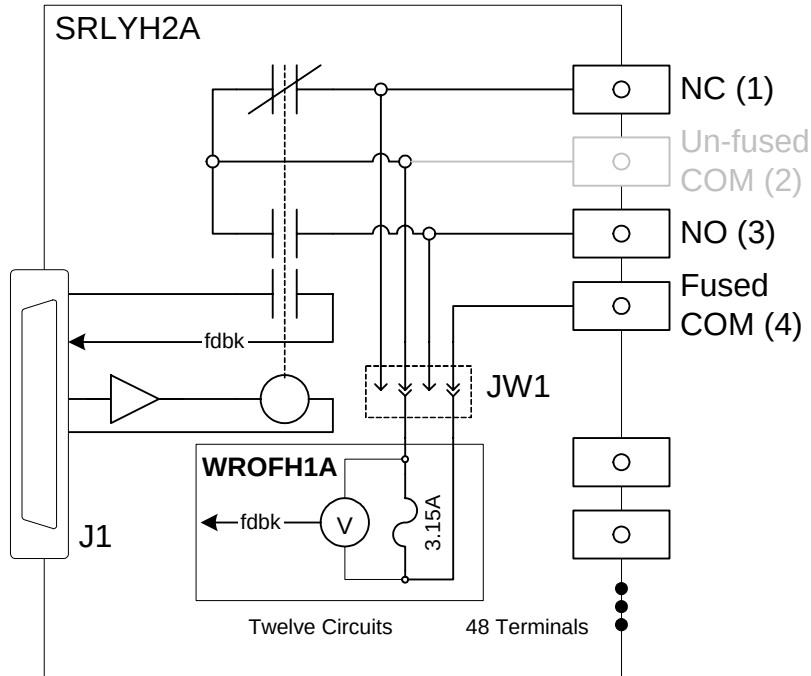
Both sides of the power distribution on relays 1-6 are fused allowing the board to be used in systems where dc power is floating with respect to earth. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications as well as 120 V and 240 V ac applications.

The following table lists the relationship between fuses, jumpers, relays, and terminals.

| Relay | +Fuse | -Fuse | Jumper | Terminals |
|-------|-------|-------|--------|-----------|
| 1     | FU7   | FU1   | JP1    | 1-4       |
| 2     | FU8   | FU2   | JP2    | 5-8       |
| 3     | FU9   | FU3   | JP3    | 9-12      |
| 4     | FU10  | FU4   | JP4    | 13-16     |
| 5     | FU11  | FU5   | JP5    | 17-20     |
| 6     | FU12  | FU6   | JP6    | 21-24     |

## SRLY + WROF

Option board IS200WROFH1A adds an optional fuse in series with the COM connection for each relay by using the SOL terminal in place of COM. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications as well as 120 V and 240 V ac applications. IS200WROFH1 has default fuse values of 3.15 A. Electrically IS200SRLYH2 plus IS200WROFH1 has the following circuit. Connector JW2 and its connections to J1 are omitted for clarity.

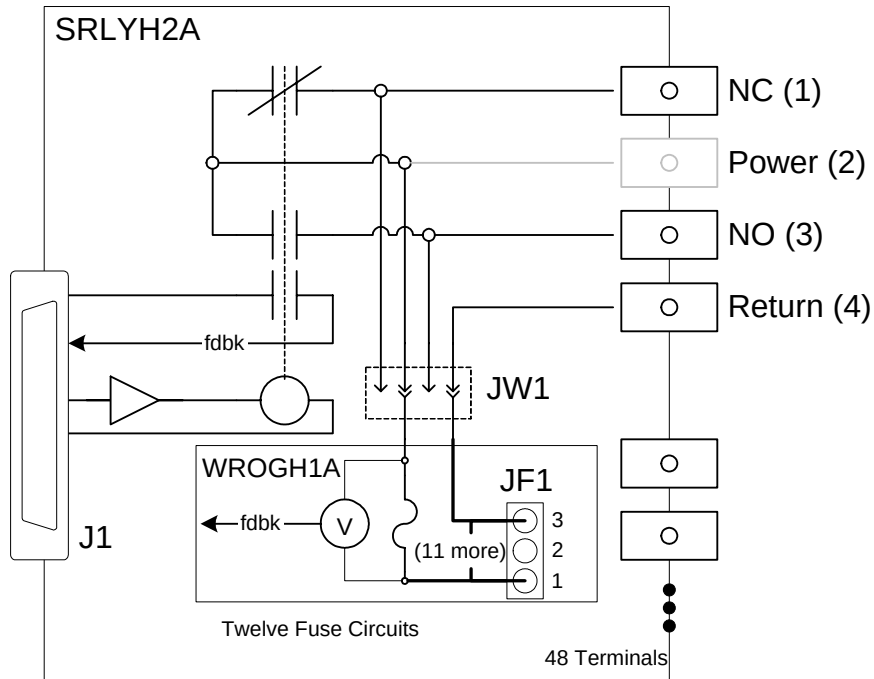


The normal application for this board is when it is desired that each relay have a fuse in series and power applied from an external source. The board has a second potential application. If the fuse is removed from a circuit, the isolated voltage detector remains. The fourth terminal (called Fused COM above) may now be wired to either the NC or NO terminal to provide isolated contact voltage feedback. PDOA I/O pack firmware has a configuration option to turn off fuse blown alarm generation for a given relay if it is being used in this fashion. The terminal table identifies this application as making the fourth screw Vsense.

Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively.

## SRLY + WROG

Option board IS200WROGH1A adds fused power distribution for all twelve relays. Isolated voltage sensing that is not polarity sensitive is provided for each fuse. Fuse voltage feedback is compatible with 24 V, 48 V, and 125 V dc applications, as well as 120 V and 240 V ac applications. IS200WROGH1 has default fuse values of 3.15 A. Electrically IS200SRLYH2 plus IS200WROGH1 has the following circuit. Connector JW2 and its connections to J1 are omitted for clarity.



Fuses FU1 through FU12 are associated with relay circuits 1 through 12 respectively.

## Specification

| Item                                       | Specification                                                                                                                                                                                           |
|--------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of relay channels on one SRLY board | 12:                                                                                                                                                                                                     |
| Rated voltage on relays                    | a: Nominal 24 V dc, 48 V dc, or 125 V dc<br>b: Nominal 120 V ac or 240 V ac                                                                                                                             |
| Max load current                           | a: 0.4 A for 125 V dc operation<br>b: 1.2 A for 48 V dc operation<br>c: 3.15 A for 24 V dc operation<br>d: 3.15 A for 120/240 V ac, 50/60 Hz operation                                                  |
| Max response time on                       | 25 ms typical                                                                                                                                                                                           |
| Max response time off                      | 25 ms typical                                                                                                                                                                                           |
| Contact material                           | Silver cad-oxide                                                                                                                                                                                        |
| Contact life                               | Electrical operations: 100,000<br>Mechanical operations: 10,000,000                                                                                                                                     |
| Fault detection                            | Relay position feedback using contact pair separate from load contacts.                                                                                                                                 |
| <b>WROBH1 Option Board</b>                 |                                                                                                                                                                                                         |
| Powered Output Circuits                    | 6 fused, associated with relays 1-6, fed from parallel connectors JF1 and JF2. Both sides of the power source are fused for each output.<br>1 unfused, associated with relay 12, fed from connector JG1 |

| Item                       | Specification                                                                                                                                                                        |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>WROFH1 Option Board</b> |                                                                                                                                                                                      |
| Fused Output Circuits      | 12 fused circuits, one per relay.                                                                                                                                                    |
| <b>WROGH1 Option Board</b> |                                                                                                                                                                                      |
| Powered Output Circuits    | 12 fused circuits, one associated with each relay. Single side fusing of the power is associated with the power input on JF1 pin 1. Return power path through JF1pin 3 is not fused. |
| <b>Physical</b>            |                                                                                                                                                                                      |
| Size                       | 15.9 cm high x 17.8 cm wide (6.25 in. x 7.0 in.)                                                                                                                                     |
| Technology                 | Surface-mount.                                                                                                                                                                       |
| Temperature                | Operating -30 to 65°C (-22 to +149 °F)                                                                                                                                               |
| Humidity                   | Operating humidity is 5 to 95% non-condensing                                                                                                                                        |
| Cooling                    | Free air convection                                                                                                                                                                  |

## ***Diagnostics***

Terminal board connectors have their own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by PDOA and a mismatch is encountered, a hardware incompatibility fault is created. Each of the option boards also contains an ID device that uniquely identifies the board.

The SRLY provides diagnostic feedback to PDOA indicating each relay position by monitoring an isolated set of contacts on each relay. When WROB is used with SRLY isolated voltage feedback is used to detect fuse status for the six fuse pairs on the board. When WROF is used with SRLY isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open a diagnostic is generated. The diagnostic may be disabled in PDOA configuration should it be desired to use the feedback circuit with the fuse removed. When WROG is used with SRLY isolated voltage feedback is used to monitor each fuse. If voltage is present and the fuse is open a diagnostic is generated.

## ***Configuration***

There are no jumpers associated with the SRLY terminal board.

Option board WROBH1 includes six jumpers that are used to apply or remove power from a relay. Boards are produced with all six jumpers in place. The jumper is removed from the board when a relay is to be used as dry contacts and power distribution is not desired.

There are no jumpers associated with the WROFH1 board. For each relay the inclusion or exclusion of a series fuse is determined by the terminal point used as the relay common. In addition for each relay the associated WROF fuse may be removed to allow direct use of the fuse voltage sensing circuit as a voltage detector.

There are no jumpers associated with the WROGH1 board. For each relay the corresponding fuse may be removed if the relay is to be used to provide dry contacts.

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## ***Notes***



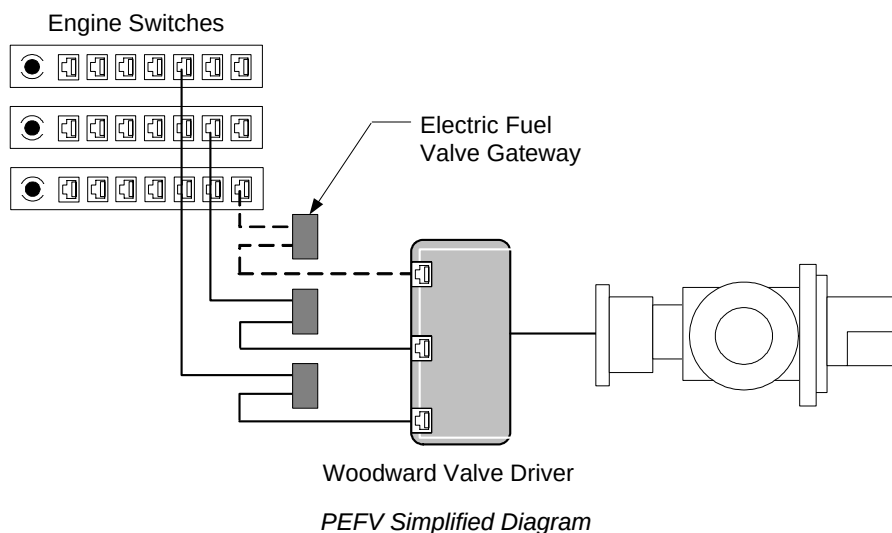
# PEFV Electrical Fuel Valve Gateway

## PEFV/TEFV Electric Fuel Valve Gateway

### Functional Description

The Electric Fuel Valve Gateway (PEFV) is an Ethernet gateway between the Mark\* VIe I/O Ethernet network and an electric fuel valve interface module. The module communicates through the Ethernet Global Data (EGD). The fuel valve interface module is called a Digital Valve Positioner (DVP). It is made by Woodward® Controls.

The PEFV contains a processor board common to all Mark VIe I/O packs. One of the dual RJ45 Ethernet connectors connects to the I/O Ethernet network. The other RJ45 Ethernet connector connects directly to the DVP. A 3-pin connector supplies power to the pack.



### Compatibility

The Electric Fuel Valve Terminal board (TEFVH1A), in this configuration, is used to mount the PEFV only. The connections on the board are for electronic ID only. It uses no other connections. Visual diagnostics are provided through indicator LEDs on the PEFV. An infrared port provides local diagnostic serial communication.

| Terminal Board | TEFVH1A |
|----------------|---------|
|----------------|---------|

|              |             |            |         |
|--------------|-------------|------------|---------|
| Control mode | Simplex-yes | Dual – yes | TMR-yes |
|--------------|-------------|------------|---------|

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one network connection on each.
- Dual uses two I/O packs with one network connections on each.
- TMR uses three I/O packs with one network connection on each.

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**Note** PEFV can be configured as simplex, dual, or TMR. By design, PEFV works specifically with the Woodward Controls DVP. The DVP has three Ethernet connections and must use all three to function properly.

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## ***Installation***

### **➤ To install the PEFV pack**

- 1 Securely mount the TEFVH1A terminal board.
- 2 Directly plug three PEFVs, for triple modular redundancy (TMR), into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded inserts adjacent to the Ethernet ports. The inserts connect to a mounting bracket specific to the terminal board type. The bracket should be adjusted so there is no right angle force applied to the DC-37 pin connector between the pack and the terminal board. This adjustment is required once during the life of the product.
- 4 Plug one Ethernet cable into the I/O Ethernet network. Connect the other Ethernet cable to the corresponding network connector on the Woodward DVP. The pack will operate with connections made to either port. The pack must reboot if the connections are modified. Standard practice is to connect ENET1 to the network associated with the I/O Ethernet network.
- 5 Power is applied to the connector on the side of the pack. It is not necessary to insert the connector with power removed from the cable. PEFV has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the PEFV as necessary.

## ***Operation***

### ***Processor***

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

### ***Electric Fuel Valve Gateway Hardware***

The PEFV links the Woodward DVP to the Mark VIe through the two network connections on the processor board. The associated terminal board provides a unique board ID identifying PEFV to the Mark VIe system. The terminal board is not used for any I/O connections. Data from the Mark VIe goes to the PEFV through the Ethernet connection to the I/O Ethernet network. Next, the data is passed to the DVP through the other Ethernet connection to the DVP. The IP addresses for these networks must be configured correctly for the communication link to be valid.

### ***ID Line***

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

### ***Power Management***

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

Each serial channel has two indicator LEDs. The TX LED flashes when PEFV transmits from a port.

The RX LED flashes when a port is receiving data.

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Specifications

| Item            | PEFV Specification                                                                                                                                                                                                        |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Transmit time   | Data from Mark VIe is transmitted once per frame, up to 100 times per second.                                                                                                                                             |
| Receive time    | Data from DVP is received asynchronously from the Woodward DVP at a rate up to 100 times per second. This data is transmitted to the Mark VIe synchronous to the frame at the frame rate. The PEFV will timeout in 50 ms. |
| Fault detection | Ethernet link ok to/from DVP<br>Data link ok to/from DVP<br>EGD Packet diagnostics<br>IP configuration error                                                                                                              |
| <b>Physical</b> |                                                                                                                                                                                                                           |
| Size            | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in. x 1.65 in. x 4.78 in.)                                                                                                                                               |
| Technology      | Surface mount                                                                                                                                                                                                             |
| Temperature     | Operating: -30 to 65°C (-22 to +149 °F)                                                                                                                                                                                   |

## Configuration

| Parameter       | Description                                                                                                                                                                                                                                                                                                                             | Selections                                      |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|
| WGC_IP_Addr     | Valve Driver (DVP) IP addresses on TMR networks should identify defaults.<br><br>Note: IP address of R network given. For S and T networks, the subnet is incremented by 1 and 2 respectively.<br><br>For example, the default R value is 192.168.128.20.<br>The S IP address is 192.168.129.20.<br>The T IP address is 192.168.130.20. | 192.168.128.20 (Default)<br>Specify IP address  |
| WGC_Subnet      | DVP network subnet mask                                                                                                                                                                                                                                                                                                                 | 255.255.255.0 (Default)<br>Specify subnet mask. |
| Gateway_IP_Addr | Gateway IP addresses on TMR should identify defaults (PEFV non-IO-net IP address).<br>Follows the same conventions as WGC_IP_Addr for the S and T network IP addresses                                                                                                                                                                  | 192.168.128.1 (Default)<br>Specify IP address   |

## Alarms

### PEFV Specific Alarms

| Alarm ID | Alarm Description                                              | Possible Cause                                                                                                                                                                   | Solution                                                                                                                                                                                                      |
|----------|----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32       | No ethernet ports could be setup for WGC valve driver.         | Both networks have already received an IP address through DHCP. Both ports may be connected to the I/O Ethernet network.                                                         | Verify that network connections are correct.                                                                                                                                                                  |
| 33       | Problem with the WGC driver ethernet port.                     | Could not set up Ethernet port.                                                                                                                                                  | Redownload base flash load and firmware.                                                                                                                                                                      |
| 34       | EGD packet mismatch.                                           | EGD data is incorrect.<br>Possible causes:<br>- Incorrect PDU Type<br>- Incorrect EGD version<br>- Incorrect Producer ID<br>- Incorrect Exchange ID<br>- Incorrect EGD Signature | Verify that network addresses are configured correctly.<br>Verify that the WGC_IP_Addr is set to IP address of the DVP.<br>Verify that the Gateway_IP_Addr is set to the IP address of the PEFV gateway port. |
| 35       | Experiencing delay in reception of data from WGC valve driver. | Not receiving EGD Ethernet data from the Woodward Governor Controls DVP for 5 frames (50 ms).                                                                                    | Verify that network connections are correct.                                                                                                                                                                  |
| 36       | Egd packet out of order. Cur ID: {0:F0} Prev ID: {1:F0}        | Reserved fault will not occur                                                                                                                                                    |                                                                                                                                                                                                               |
| 37       | Egd packet missed. Cur ID: {0:F0} Prev ID: {1:F0}              | Reserved fault will not occur                                                                                                                                                    |                                                                                                                                                                                                               |
| 38       | Problem with WGC driver ethernet port while receiving          | Not receiving EGD Ethernet data from the Woodward Governor Controls DVP for 3 seconds.                                                                                           |                                                                                                                                                                                                               |
| 39       | Config Error: WGC and Gateway IP address subnet mismatch       | Subnet of configured IP addresses WGC_IP_Addr and Gateway_IP_Addr do not match.                                                                                                  |                                                                                                                                                                                                               |
| 42       | Logic Signal \$V Voting Mismatch                               |                                                                                                                                                                                  |                                                                                                                                                                                                               |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ]P_Id= [ ], =Expctd= [ ], Rcvd= [ ]  | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

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## ***Notes***



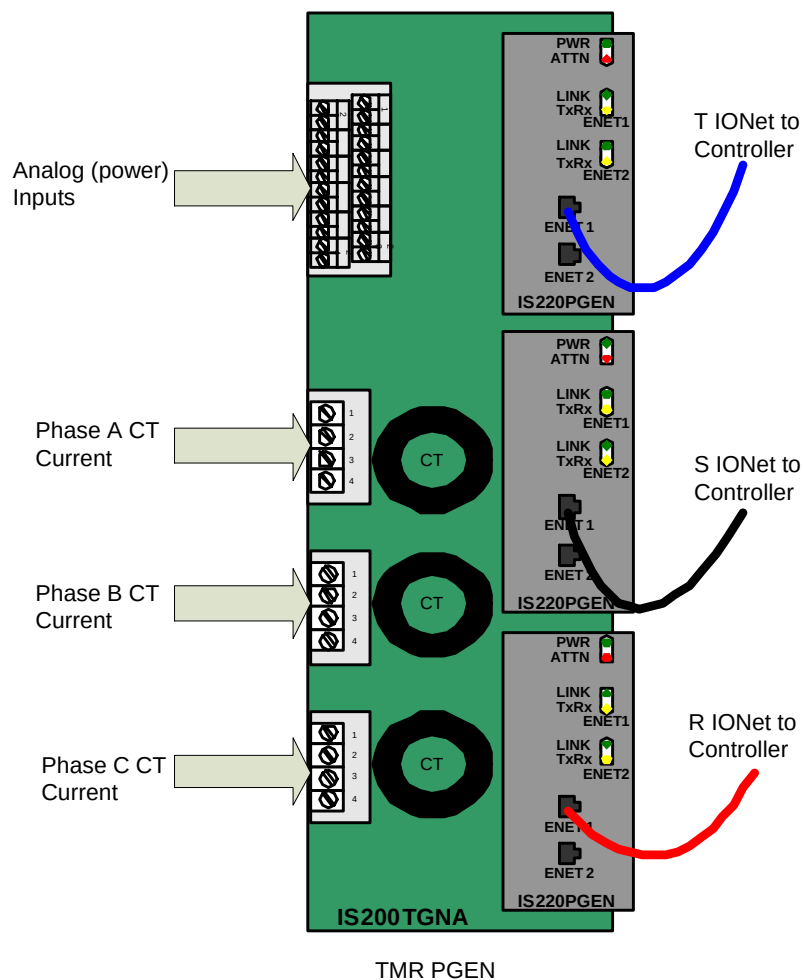
# PGEN Turbine-Generator Monitor Pack

## PGEN Turbine-Generator Monitor Pack

### Functional Description

The Mark VIe\* Turbine-Generator Monitor pack (PGEN) provides the electrical interface between one I/O Ethernet network and the TGNA turbine-generator terminal board. The pack contains a processor board common to all Mark\*VIe distributed I/O packs and an acquisition board. The pack uses 3 analog channels to monitor turbine mechanical power from voltage or 4-20 mA sensors. Each phase of generator armature current is monitored using a current transformer input.

Input to the pack is through dual RJ45 Ethernet connectors and a 3-pin power input. The PGEN supports single Ethernet networks for simplex or TMR applications. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



## Compatibility

PGENH1A is compatible with the turbine-generator Terminal Board (TGNA). The following table describes the compatibility:

| Terminal Board | TGNA        |         |         |
|----------------|-------------|---------|---------|
| Control mode   | Simplex=yes | Dual=no | TMR=yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one network connection only
- TMR uses three I/O packs with one network connection on each

## Installation

### ➤ To install the PGEN pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PGEN I/O pack for simplex or three PGEN I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-37 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one Ethernet cable only. The pack operates over either port.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

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**Note** The PGEN mounts directly to a Mark VIe terminal board. TMR-capable terminal boards have three DC-37 pin connectors, and can also be used in simplex mode if only one PGEN is installed. The PGEN directly supports all of these connections.

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## **Operation**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Local ambient temperature sensor
- Status indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The ToolboxST\* configuration of the PGEN does not allow the pack to operate redundantly from the two Ethernet inputs. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

### ***Turbine-Generator Monitoring Hardware***

The PGEN application-specific hardware consists of an analog filter acquisition board (BPAIH3). The analog filter acquisition board provides the signal conditioning to center and amplify the signal to improve analog-to-digital resolution.

The PGEN accepts analog input signals from the terminal board for three mechanical power sensors and three CT currents. The analog input section consists of an analog multiplexer block, several gain and scaling sections, and a 16-bit, analog-to-digital converter (ADC).

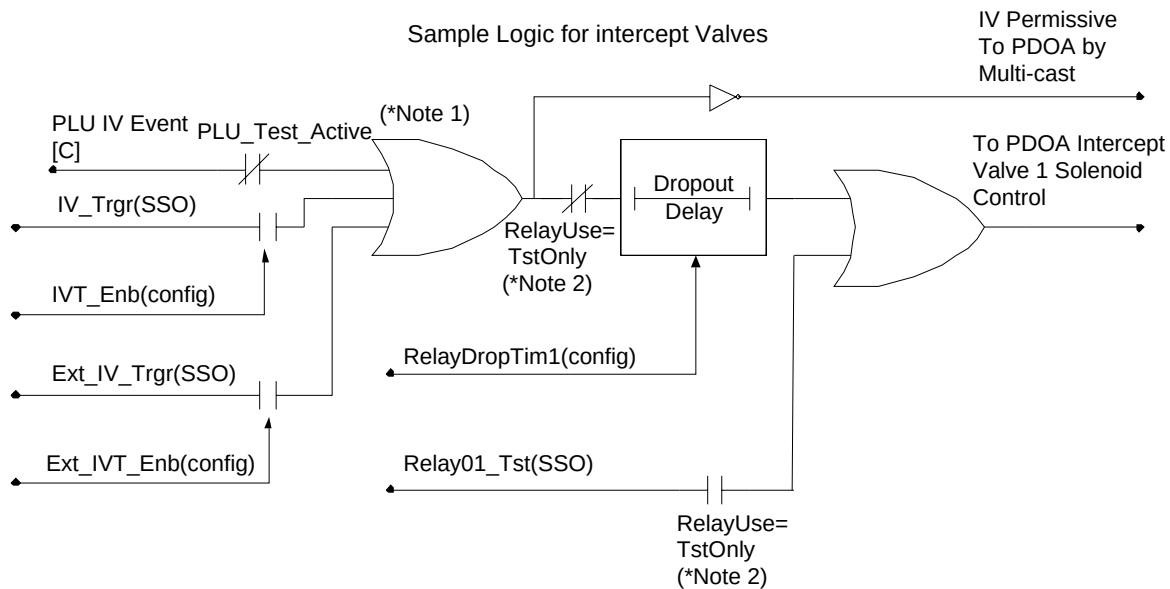
The three analog mechanical power inputs can be individually configured as +5 V, +/-10 V, or 4-20 mA scaled signals, depending on the input configuration. If configured as 4-20 mA signals, the three current inputs are brought through 250  $\Omega$  burden resistors on the terminal board. This resistance generates a 5 V signal at 20 mA. The terminal board provides a 250  $\Omega$  burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a passive, low pass filter network with a pole at 75.15 Hz. Voltage signal feedbacks from calibration voltages are also sensed by the PGEN input section.

## Power Load Unbalance Overspeed Control

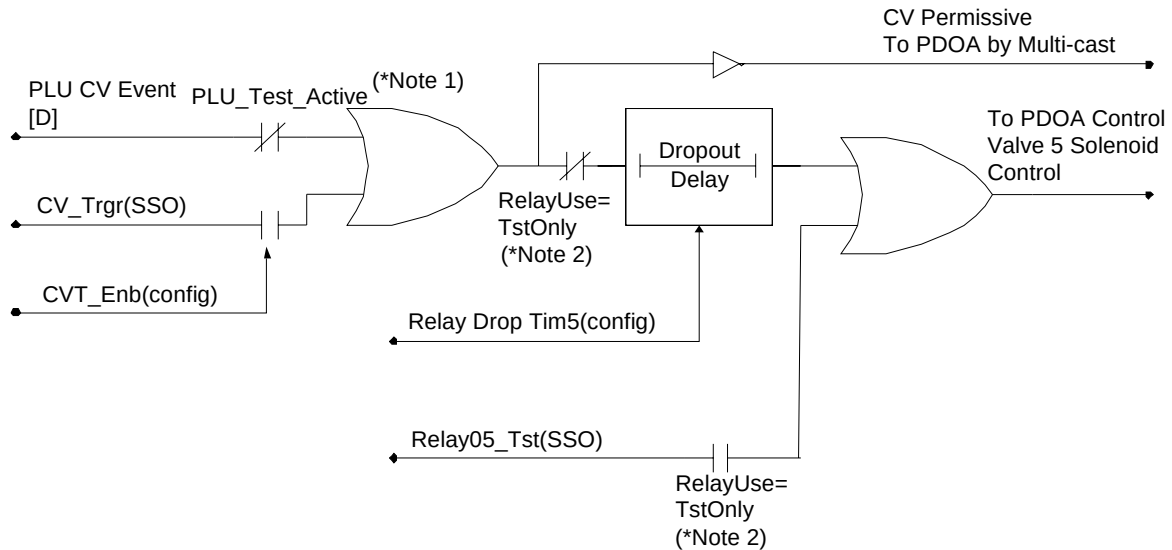
The Power Load Unbalance (PLU) function monitors the difference between the per unit steam turbine power based on steam pressure and the per unit generator power based on the generator current. A PLU event occurs when turbine per unit power is 40% greater than the generator power and the difference meets both a specified rate of change and a specified duration. When a PLU event is sensed, the steam turbine control valves (CVs) and Intercept valves (IVs) are closed to reduce the power.

The PLU monitoring is performed by the IS220PGENH#A Iopack (PGEN) and the IS200TGNAH#A (TGNA) terminal board. The PLU function supports either a TMR or Simplex configuration. The Mark VIe Digital Output IOPack, IS220PDOA and the IS200TRLYH1B(Simplex, H1F TMR) (TRLY) or terminal board controls the steam turbine CV and IV valves. The PGEN commands the state of the relays on the PDOA. The control of the relays in the PDOA is enhanced by a peer-to-peer multicast packet that provides a fast communication path. The fast communication path is in parallel with the normal pack-to-pack communication that is routed through the signal space using the controller to transfer relay commands. The multicast path is only used for the initiating command to the relays.

PLU events that are detected in firmware generate logic signals PLU\_IV\_Event to energize IV relays and PLU\_CV\_Event to energize CV relays. An additional relay communication paths is provided through PGEN signal space to allow controller application code to control the CV and IV relays. Each relay has a configurable dropout time so that relays can be dropped out in a staggered sequence. The actual dropout time may vary + one Ionet frame time (typically 40 msec) due to the asynchronous interaction of the Ionet communications and PGEN PLU processing. The following Control Valve and Intercept Valve Control Logic diagram depicts this logic.



### Sample Logic for Control Valves



### Control Valve and Intercept Valve Control Logic

**Note 1** Relay activation is blocked when signal space output PLU\_Test is True, so the signal space logicals PLU\_Event and PLU\_IV\_Event can be forced True without activating relays. This is a test mode designed for commissioning tests if needed and should not be used during normal operation.

**Note 2** When relays are configured as Test Only, the relay state can only be changed by the corresponding signal space out logical RelayxTest, where x = relay number.

### Power Management

The PGEN includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power systems.

### Status LEDs

A green LED labeled PWR is lit to show the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating. Critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded
- LED flashing quickly ( $\frac{1}{4}$  second) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code.
- LED flashing at medium speed ( $\frac{3}{4}$  second) - the pack is not online

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Connectors

The pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the turbine generator terminal board. The connector contains six input signals and an ID signal.
- An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the side of the pack can be used as an alternate to ENET1.

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**Note** The ToolboxST configuration of the PGEN does not allow the pack to operate from two Ethernet inputs simultaneously.

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- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

## Specifications

| Item                       | Specification                                                                        |                                                                |                             |                    |
|----------------------------|--------------------------------------------------------------------------------------|----------------------------------------------------------------|-----------------------------|--------------------|
| Number of channels         | TGNA: 6 inputs total consisting of 3 pressure inputs and 3 CT current inputs<br>PGEN |                                                                |                             |                    |
|                            | Measurement                                                                          | Range                                                          | Noise Suppression           | Accuracy           |
|                            |                                                                                      | (V dc + V ac)                                                  |                             |                    |
| Analog Inputs              |                                                                                      |                                                                |                             |                    |
| (channels 1-3)             | Pressure                                                                             | +/- 5 V dc<br>+/- 10 V dc<br>4-20 mA<br>All with 5% over range | 76 Hz single pole low pass  | 0.1% of full scale |
| Current Inputs             |                                                                                      |                                                                |                             |                    |
| (CT channels 1-3)          | Current                                                                              | 0 to 1 A rms<br>0 to 5 A rms<br>All with 100% over range       | 507 Hz single pole low pass | 0.1% of full scale |
| Input converter resolution | 16-bit analog-to-digital converter                                                   |                                                                |                             |                    |
| Common mode voltage range  | ±5 V (±2 V CMR for the ±10 V inputs)                                                 |                                                                |                             |                    |
| Physical                   |                                                                                      |                                                                |                             |                    |
| Size                       | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in. x 1.65 in. x 4.78 in.)          |                                                                |                             |                    |
| Temperature                | -30 to +65°C (-22 to +149 °F)                                                        |                                                                |                             |                    |
| Technology                 | Surface mount                                                                        |                                                                |                             |                    |

## ***Diagnostics***

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- Each analog or current input has hardware limit checking based on preset (configurable) high and low levels near the end of the operating range. If this limit is exceeded, a logic signal is set to Unhealthy in signal space, then the unhealthy signal is forced to zero volts or mA. The signal state returns to Healthy if the signal returns to its limits. If any signal is unhealthy, logic signal L3DIAG-PGEN is set.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital circuits.

Details of the individual diagnostics are available from the ToolboxST.application. I/O block SYS\_OUTPUTS, input RSTDIAg can be used to direct all I/O modules to clear from the alarm queue all diagnostics in the normal healthy state.

## Configuration

**Note** The following information extracted from the ToolboxST application represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter    | Description                                                                                               | Sections                                              |
|--------------|-----------------------------------------------------------------------------------------------------------|-------------------------------------------------------|
| SystemLimits | Enable or disable All system limit checking                                                               | Enable, disable (default-enable)                      |
| PLU_DeI_Enab | Enable the PLU delay                                                                                      | Enable, disable (default-enable)                      |
| IVT_Enab     | Enable the turbine control-driven IV trigger function                                                     | Enable, disable (default-enable)                      |
| PLU_DiagEnab | Enable voting disagreement diagnostic for PLU_Event                                                       | Enable, disable (default-enable)                      |
| Ext_IVT_Enb  | Enable customer-driven IV trigger function                                                                | Enable, disable (default-disable)                     |
| MechPwrInput | Mech power through: TMR(median of 3),dual(max of first two), single Xducer, or signal space               | DualXducer, Signal Space, TMRXducer, Xducer1, Xducer2 |
| PLU_Unbal    | PLU unbalance threshold, percent                                                                          | 20 to 80 (default-40)                                 |
| PLU_Delay    | PLU delay, seconds                                                                                        | 0 to 0.5 (default-0)                                  |
| PressRatg    | Reheat pressure equivalent to 100 % mech power (engineering units)                                        | 5 to 1500 (default-200)                               |
| CurrentRatg  | Generator current equivalent to 100 % elect power (amps RMS)                                              | 1 to 2E6 (default-20000)                              |
| PowerScale   | Scale factor that multiplies time per unit current to equate generator power to per unit mechanical power | 0 to 2 (default 1.0)                                  |
| Min_MA_Input | Minimum MA for healthy 4/20 mA Input                                                                      | 0 to 22.5 (default-4)                                 |
| Max_MA_Input | Maximum MA for healthy 4/20 mA Input                                                                      | 0 to 22.5 (default-20.40)                             |
| SystemFreq   | System frequency in Hz                                                                                    | 60Hz, 50Hz (default-60Hz)                             |
| CT_Primary   | Generator CT primary in amperes RMS                                                                       | 1 to 1.2E+06 Arms (default- 20000)                    |
| CT_Secondary | Generator CT secondary in amperes RMS (TGNA CT input)                                                     | 1 to 5 Arms<br>0 to 1 Arms (default: 0 to 5 Arms)     |
| CVT_Enab     | Enable the turbine control-driven CV trigger function                                                     | Enable, disable (default-Disable)                     |

All other I/O configuration parameters are defined under the specific pack or terminal board variables variables in the following sections.

### PGEN Variable Definitions

| Name                              | Description                                                                               | Direction/Type                   |
|-----------------------------------|-------------------------------------------------------------------------------------------|----------------------------------|
| L3DIAG_PGEN                       | PGEN diagnostics                                                                          | (Input non-voted Boolean-3 bits) |
| Cap1_Ready                        | Capture buffer 1 ready for upload-not used                                                | (Input non-voted Boolean-3 bits) |
| Cap2_Ready                        | Capture buffer 2 ready for upload-not used                                                | (Input non-voted Boolean-3 bits) |
| SysLim2analogInx where x = 1 to 3 | Boolean set TRUE if System Limit 1 exceeded for analog input x (Vgen has only 3, 4th TBD) | (Input Boolean)                  |
| SysLim2AnalogInx where x = 1 to 3 | Boolean set TRUE if system limit 2 exceeded for analog input x                            | (Input Boolean)                  |
| SysLim1GenCTa                     | Boolean set TRUE if system limit 1 exceeded for phase A generator current                 | (Input Boolean)                  |
| SysLim1GenCTb                     | Boolean set TRUE if system limit 1 exceeded for phase B generator current                 | (Input Boolean)                  |
| SysLim1GenCTc                     | Boolean set TRUE if system limit 1 exceeded for phase C generator current                 | (Input Boolean)                  |
| SysLim2GenCTa                     | Boolean set TRUE if system limit 2 exceeded for phase A generator current                 | (Input Boolean)                  |



| <b>Name</b>                | <b>Description</b>                                                                                                                                               | <b>Direction/Type</b> |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| SysLim2GenCTb              | Boolean set TRUE if system limit 2 exceeded for phase B generator current                                                                                        | (Input Boolean)       |
| SysLim2GenCTc              | Boolean set TRUE if system limit 2 exceeded for phase C generator current                                                                                        | (Input Boolean)       |
| PLU_Diff_Value             | Equal to the steam turbine per unit power based on the reheat pressure minus the generator per unit power (corrected by power scale) based on generator current. | (Input FLOAT)         |
| PLU_Event                  | Boolean set TRUE if a PLU has occurred.                                                                                                                          | (Input Boolean)       |
| PLU_IV_Event               | Boolean set TRUE if a PLU intercept valve event has occurred.                                                                                                    | (Input Boolean)       |
| PLU_Current                | Generator current (amps rms) scaled by power scale                                                                                                               | (Input Float)         |
| SteamPressure              | Steam pressure (EUs)                                                                                                                                             | (Input Float)         |
| CV_Permissive              | Boolean set TRUE to leave CV relays de-energized                                                                                                                 | (Input Boolean)       |
| IV_Permissive              | Boolean set TRUE to leave IV relays de-energized                                                                                                                 | (Input Boolean)       |
| Relay01Test to Relay12Test | Solenoid 1 test                                                                                                                                                  | (Output Boolean)      |
| PLU_Tst                    | Boolean to command PLU test.                                                                                                                                     | (Output Boolean)      |
| IV_Trgr                    | Turbine control-driven IV trigger                                                                                                                                | (Output Boolean)      |
| Ext_IV_Trgr                | Customer-driven IV trigger                                                                                                                                       | (Output Boolean)      |
| MechPower                  | Mechanical power (percent) when configured through signal space                                                                                                  | (Output Float)        |

*IS200TGNA Variable Definitions*

| <b>AnalogInputOx</b>      | <b>Analog input x - Card Point</b>                                                                                                                         | <b>Point Edit (Input FLOAT)</b>                                   |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| <b>where x = 1 thru 3</b> |                                                                                                                                                            |                                                                   |
| InputUse                  | Defines analog input as either as $\pm 10$ volt, $\pm 5$ volt, 4-20 mA or unused.                                                                          | $\pm 5$ volt $\pm 10$ volt<br>4-20 mA unused<br>(Default- unused) |
| Low_Input                 | Defines point 1 x-axis value in volts or mA for the TGNA terminal point used in calculating the gain and offset for the conversion to engineering units.   | 0 to 10 volts or<br>-10 to 20 mA<br>(Default- 4.0)                |
| High_Input                | Defines point 2 x-axis value in volts or mA for the TGNA terminal point used in calculating the gain and offset for the conversion to engineering units.   | 0 to 10 volts or<br>-10 to 20 mA<br>(Default- 20.0)               |
| Low_Value                 | Defines point 1 Y-axis value in engineering units for the TGNA terminal point used in calculating the gain and offset for the conversion from volts to EUs | $\pm 3.402820 \text{ E}+38$ EUs<br>(Default- 0.0)                 |
| High_Value                | Defines point 2 Y-axis value in engineering units for the TGNA terminal point used in calculating the gain and offset for the conversion from volts to EUs | $\pm 3.402820 \text{ E}+38$ EUs<br>(Default- 100.0)               |
| InputFilter               | Filter bandwidth in Hz (pressure inputs)                                                                                                                   | 0.75 Hz, 1.5 Hz, 3 Hz, 6 Hz, 2 Hz or unused (Default- 12Hz)       |
| SysLim1Enabl              | Enable system Limit 1 fault check                                                                                                                          | Enable, disable<br>(Default- disable)                             |
| SysLim1Latch              | Latch system Limit 1 fault                                                                                                                                 | Latch, Not Latch<br>(Default- Latch)                              |
| SysLim1Type               | System Limit 1 check type                                                                                                                                  | $\geq$ or $\leq$<br>(Default- $\geq$ )                            |

| <b>AnalogInputOx</b><br><b>where x = 1 thru 3</b> | <b>Analog input x - Card Point</b>                                   | <b>Point Edit (Input FLOAT)</b>        |
|---------------------------------------------------|----------------------------------------------------------------------|----------------------------------------|
| SysLimit1                                         | System Limit 1 – EUs                                                 | ±3.402820 E+38 EUs<br>(Default- 0.0)   |
| SysLim2Enabl                                      | Enable system Limit 2 (same configuration as for Limit 1)            | Enable, disable<br>(Default- disable)  |
| SysLim2Latch                                      | Latch system Limit 2 fault                                           | Latch, Not Latch<br>(Default- Latch)   |
| SysLim2Type                                       | System Limit 2 check type                                            | >= or <=<br>(Default- <=)              |
| SysLimit2                                         | System Limit 2 – EUs                                                 | +/-3.402820 E+38 EUs<br>(Default- 0.0) |
| TMR_DiffLmt                                       | Difference limit for voted TMR inputs in percent                     | 0 to 100 percent<br>(Default- 5)       |
| DiagHighEnab                                      | Enable high input limit diag                                         | Enable, Disable<br>(Default-Enable)    |
| DiagLowEnab                                       | Enable low input limit diag                                          | Enable, Disable<br>(Default-Enable)    |
| GenCTInputOx<br>where x = 1, 2 or 3               | Total generator line current x to neutral (amps rms)<br>- Card Point | Point Edit (Input FLOAT)               |
| SysLim1Enabl                                      | Enable system limit 1 fault check                                    | Enable, Disable<br>(Default- Disable)  |
| SysLim1Latch                                      | Latch system Limit 1 Fault                                           | Latch, Not Latch<br>(Default- Latch)   |
| SysLim1Type                                       | System limit 1 check type                                            | >= or <=<br>(Default- >=)              |
| SysLimit1                                         | System limit 1 – EUs                                                 | +/-3.402820 E+38 EUs<br>(Default- 0.0) |
| SysLim2Enabl                                      | Enable system limit 2 (same configuration as for limit 1)            | Enable, Disable<br>(Default- Disable)  |
| SysLim2Latch                                      | Latch system limit 2 fault                                           | Latch, Not Latch<br>(Default- Latch)   |
| SysLim2Type                                       | System limit 2 check Type                                            | >= or <=<br>(Default- <=)              |
| SysLimit2                                         | System limit 2 – EUs                                                 | +/-3.402820 E+38 Eus<br>(Default- 0.0) |
| TMR_DiffLmt                                       | Difference limit for voted TMR inputs in EUs                         | +/-3.402820 E+38 EUs<br>(Default- 100) |
| Relayx<br>where x = 1 thru 12                     | Solenoid x state - card point                                        | Boolean                                |

| <b>AnalogInputOx</b>      | <b>Analog input x - Card Point</b>                                                                                                                                                     | <b>Point Edit (Input FLOAT)</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>where x = 1 thru 3</b> |                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| RelayUse                  | Defines relay type.                                                                                                                                                                    | CV_FASV_Type (1-4): control valve<br>IV_FASV_Type (5-10): intercept valve TstOnly : test driven<br>Unused<br>Spare CV_Fas_Type(11 only)<br>Spare IV_Fas_Type(12 only)<br>(Default Relay1 – CV 1)<br>(Default Relay2 – CV 2)<br>(Default Relay3 – CV 3)<br>(Default Relay4 – CV 4)<br>(Default Relay5 – IV 1)<br>(Default Relay6 – IV 2)<br>(Default Relay7 – IV 3)<br>(Default Relay8 – IV 4)<br>(Default Relay9 – IV 5)<br>(Default Relay10 – IV 6)<br>(Default Relay11 – Spare CV)<br>(Default Relay12 – Spare IV) |
| RelayDropTim              | Relay dropout time - The actual dropout time may vary + 1 lonet frame time (typically 40 msec) due to the asynchronous interaction of the lonet communications and PGEN PLU processing | 0.0 to 5.0 seconds<br>(Default Relay1 – 1.10)<br>(Default Relay2 – 2.00)<br>(Default Relay3 – 3.00)<br>(Default Relay4 – 4.00)<br>(Default Relay5 – 0.35)<br>(Default Relay6 – 0.50)<br>(Default Relay7 – 0.75)<br>(Default Relay8 – 0.35)<br>(Default Relay9 – 0.75)<br>(Default Relay10 – 0.50)<br>(Default Relay11 – 0.00)<br>(Default Relay12 – 0.00)                                                                                                                                                            |

## PLU Configuration

If an IS220PGEN is to connect to an IS220PDOA module to perform a coordinated PLU Speed Control function, the two modules need to be linked in the ToolboxST configuration. This link is configured in the text block that displays when the module is double-clicked. The PGEN should be configured first by selecting the *PLU Function Enabled* check box.

**Modify : PGEN-21**

☐ Module Required    I/O pack Redundancy: TMR    Hardware Group: Distributed I/O

**Terminal Board**

| TBRef | Type | H/W Form | Bar Code | Position |
|-------|------|----------|----------|----------|
| TB1   | TGNA | H1A      | S23Y03K  | 21       |

**I/O Pack Configurations**

| PackRef | H/W Form | TB Connector | Connection A | Connection B |
|---------|----------|--------------|--------------|--------------|
| PackR   | H1A      | JR1          | IoNet1       |              |
| PackS   | H1A      | JS1          | IoNet2       |              |
| PackT   | H1A      | JT1          | IoNet3       |              |

☒ PLU Function Enabled

OK    Cancel

After the PGEN is configured, link the PDOA to the PLU-configured PGEN by selecting the *PLU-enabled PGEN* from the *I/O Module Trip From* drop-down list.

**Modify : PDOA-22**

☐ Module Required    I/O pack Redundancy: TMR    Hardware Group: Distributed I/O

**Terminal Board**

| TBRef | Type | H/W Form | Bar Code | Position |
|-------|------|----------|----------|----------|
| TB1   | TRLY | H1F      | 00YUI4F  | 22       |

**I/O Pack Configurations**

| PackRef | H/W Form | TB Connector | Connection A | Connection B |
|---------|----------|--------------|--------------|--------------|
| PackR   | H1A      | JR1          | IoNet1       |              |
| PackS   | H1A      | JS1          | IoNet2       |              |
| PackT   | H1A      | JT1          | IoNet3       |              |

I/O Module Trip From: PGEN(PLU) - 21

OK    Cancel

Additionally, the relay commands in the PGEN signal space must be connected to the relay outputs in the PDOA signal space by using common connected variables.

# Alarms

## PGEN Specific Alarms

| Alarm ID | Alarm Description                                            | Possible Cause                                                                                                                         | Solution                                                                                                                                                                                                                                                                                                                    |
|----------|--------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32       | Unallowed VarIOCompatCode Change: Old - {0:F0}; New - {0:F0} | A .dll file (ToolboxST support file) has been installed that is incompatible with the firmware loaded on the I/O processor.            | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                                                                                                                                         |
| 33-35    | Analog Input {0:F0} Unhealthy                                | Analog input 1-3 signal strength is outside of limits for sensor type.                                                                 | For 4-20 mA analog inputs: Check configuration parameters MaxMAInput and MinMAINput for proper values.<br>For voltage analog inputs: Inputs voltage magnitude is greater than 9.24 V.<br>Check analog inputs 1-3 at terminal points for in range values.<br>Replace PGEN IO pack or TGNA terminal board if inputs in range. |
| 36-39    | Generator Current Input {0:F0} Unhealthy                     | CT input current exceeds configured CT input by 200%.                                                                                  | Check configuration parameter CT_Secondary for correct setting.<br>Check CT input currents for currents exceeding 200% of configured (5 or 1 A).<br>Replace PGEN IO pack or TGNA terminal board if inputs in range.                                                                                                         |
| 40-46    | Channel {0:F0} ADC Conversion Error                          | The analog to digital conversion for the specified input failed to complete.                                                           | Replace the PGEN IO pack.                                                                                                                                                                                                                                                                                                   |
| 47       | ADC Conversion Not Completed                                 | The analog to digital conversion of terminal board signals failed to complete before the next conversion cycle was scheduled to start. | Replace the PGEN IO pack. Contact factory if persists after pack replacement.                                                                                                                                                                                                                                               |
| 51       | Reference Input Out Of Range                                 | Reference calibration voltage exceeds 5% of expected.                                                                                  | Check terminal board grounding for noise or poor connections.<br>Replace PGEN IO pack if grounding OK.                                                                                                                                                                                                                      |
| 52       | Null Input Out Of Range                                      | Null calibration voltage exceeds 150 mV.                                                                                               | Check terminal board grounding for noise or poor connections.<br>Replace PGEN IO pack if grounding OK.                                                                                                                                                                                                                      |
| 53       | Multicast communication initialization failure               | The peer-to-peer communication link between the PGEN and the PDOA failed to initialize.                                                | Replace the PGEN IO pack.                                                                                                                                                                                                                                                                                                   |
| 54       | FPGA Interrupt Time Out                                      | Interrupt to read terminal board signals failed to occur at the designated time.                                                       | Replace PGEN IO pack.<br>Contact factory if persists after pack replacement.                                                                                                                                                                                                                                                |
| 55       | Logic Signal \$V Voting Mismatch                             | A problem with the input. This could be the device, the wire to the terminal board, or the terminal board.                             |                                                                                                                                                                                                                                                                                                                             |
| 56-64    | Input Signal \$V Voting Mismatch, Local={0:F3}, Voted={1:F3} | A problem with the input. This could be the device, the wire to the terminal board, or the terminal board.                             |                                                                                                                                                                                                                                                                                                                             |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                           |
|-------|-----------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                              |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                         |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                              |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                              |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                              |
| 7     | I/O pack – The I/O pack has gone to the Offline state                       | Lost communication with controller                                                                                                                       |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                            |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A dll file has been installed that is incompatible with the firmware on the I/O board. Either the dll file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A dll file has been installed that is incompatible with the firmware on the I/O board. Either the dll file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                           |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                             |
| 258   | I/O pack Temperature [ ] ° F is out of range [ ] to [ ] ° F                 | Temperature went outside -20°C to +85 °C (-4° F to +185° F)                                                                                              |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                               |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                           |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                    |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                               |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                               |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                 |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                          |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start                                                                                                                     |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                 |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                         |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                            |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                             |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                     |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                             |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                 |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ]P_Id= [ ], =Expctd= [ ], Rcvd= [ ]  | Message version mismatch                                                                                                                                 |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ].got [ ]                     | Exchange message wrong length                                                                                                                            |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                              |
| 301   | IO pack - XML files are missing                                             | I/O pack IO configuration files missing                                                                                                                  |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ].                          | I/O pack outputs not received from controller                                                                                                            |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                              |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                          |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received I/O pack        | SSO data is not being updated                                                           |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

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## ***TGNA Turbine-Generator Monitor Pack***

### ***Functional Description***

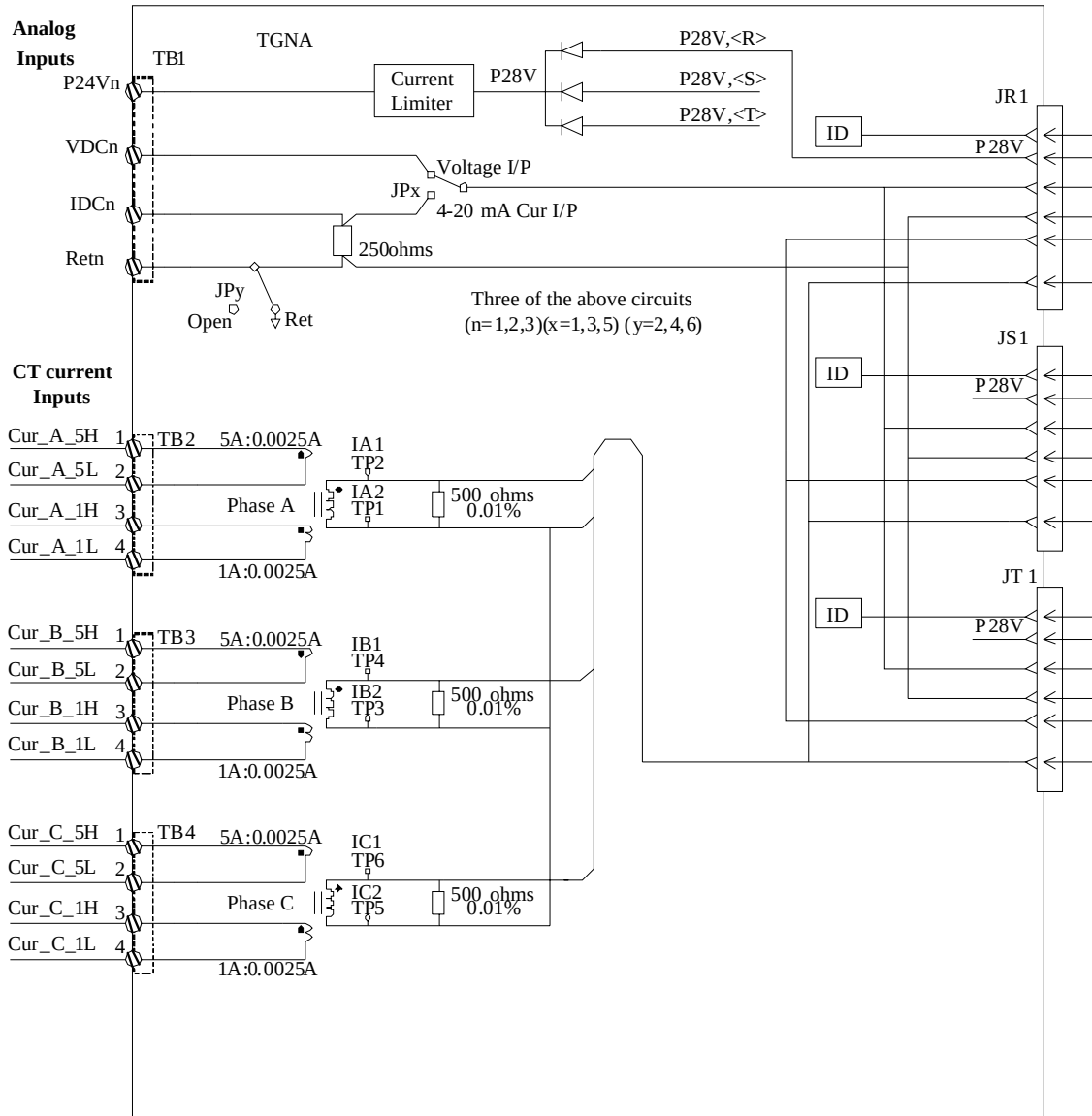
The Turbine-Generator terminal board (TGNA) acts as a signal interface board for the Mark VIe I/O pack PGEN. In the Mark VI system, the VGEN board works with TGEN. The TGNA provides a direct interface to three analog inputs for sensing turbine steam pressure and three current transformer (CT) feedbacks for sensing generator current.

The three analog inputs are configurable to be 4-20 mA, +/- 5 V, or +/-10 V inputs. There are two jumpers for each analog input. One jumper is used to select either current (4-20 mA) or voltage feedback. The other jumper can optionally ground the return path for the inputs.

The three CT inputs can be fed from 1 A or 5 A rated CT outputs. A separate terminal board point is provided for the two different amp rated inputs. Configuration parameter CT\_Secondary designates which terminal board points are used.

The signals are passed on to the Mark VIe I/O packs through a 37-pin connector. The TGNA can be used for either simplex or TMR applications. TMR applications fan the signal to three I/O packs.

In the Mark VIe system, the PGEN I/O pack works with the TGNA. Simplex and TMR systems are supported. In TMR systems, three PGEN packs plug into the TGNA.



TGNA Turbine-Generator Terminal Board

## Installation

The TGNA accepts three analog inputs (voltage or current) and three CT inputs.

Analog input channels 1 through 3:

- Supports voltage or 4-20 mA current turbine pressure inputs
- Current-limited 24 V power supply per channel
- JP1(3,5) jumper for selecting current or voltage inputs
- JP2(4,6) configures the return as Open for true differential input or connects return to PCOM for a 24 V return.

Connect the analog pressure sensors to the variables identified in the table *Terminal Variable Definitions*.



Voltage-output sensors should use VDCx and Retx as signal connection points. Jumper JP1(3,5) should be in the voltage I/P position. JP2(4,6) should be in differential input position for differential feedback and in the Return to GND position for sensors supplied with the 24 V output. Configuration parameter InputUse for the analog inputs should be set according to the type of sensor being used, +/-10 V, +/-5 V, or 4-20 mA.

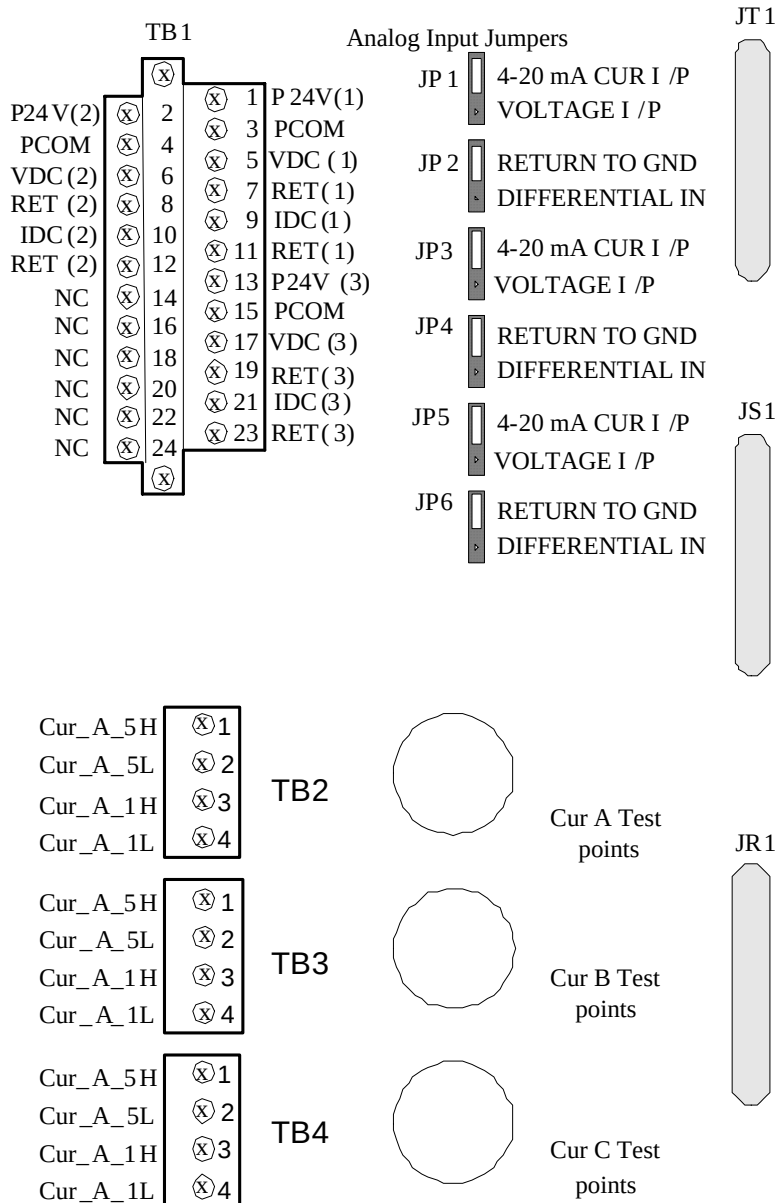
Current-based sensors should use IDCx and Retx as signal connection points. Jumper JP1(3,5) should be in the 4-20 mA I/P position. JP2(4,6) should be in differential input position.

CT current Phase A, B, C

- Supports 0 to 1 A or 0 to 5 A CT secondary currents
- Separate terminal points for 0 to 1 A or 0 to 5 A CT secondary currents

Connect the secondary of the generator current CT sensors to the points identified in the table, *Terminal Point Definitions*. The CT sensors should use the pair of signal points corresponding to the secondary rating of the CT sensors, 1 A or 5 A. The configuration parameter CT\_Secondary should be set to the rating of the CT secondary.

## Generator Terminal Board TGNA



Terminal block 1 can be unplugged from terminal board for maintenance TB2, TB3, TB4 are not pluggable

*TGNA Turbine-Generator Monitoring Terminal Board*

| CH #            | Point  | Signal   | Description                               |
|-----------------|--------|----------|-------------------------------------------|
| Analog 1        | TB1-1  | P24V1    | +24 V output feed for pressure sensor     |
|                 | TB1-3  | PCOM1    | Power supply return for the P24 V         |
|                 | TB1-5  | VDC1     | Turbine pressure voltage, signal          |
|                 | TB1-7  | Ret1     | Turbine pressure voltage/current , return |
|                 | TB1-9  | IDC1     | Turbine pressure 4-20 mA, signal          |
| Analog 2        | TB1-2  | P24V2    | +24 V output feed for pressure sensor     |
|                 | TB1-4  | PCOM2    | Power supply return for the P24 V         |
|                 | TB1-6  | VDC2     | Turbine pressure voltage, signal          |
| Analog 3        | TB1-8  | Ret2     | Turbine pressure voltage/current , return |
|                 | TB1-10 | IDC2     | Turbine pressure 4-20 mA, signal          |
|                 | TB1-13 | P24V3    | +24 V output feed for pressure sensor     |
|                 | TB1-15 | PCOM3    | Power supply return for the P24 V         |
|                 | TB1-17 | VDC3     | Turbine pressure voltage, signal          |
|                 | TB1-19 | Ret3     | Turbine pressure voltage/current , return |
| Phase A current | TB1-21 | IDC3     | Turbine pressure 4-20 mA, signal          |
|                 | TB2-1  | CUR_A_5H | 5 A CT current , high                     |
|                 | TB2-2  | CUR_A_5L | 5 A CT current, low                       |
| Phase B current | TB2-3  | CUR_A_1H | 1 A CT current, high                      |
|                 | TB2-4  | CUR_A_1L | 1 A CT current, low                       |
|                 | TB3-1  | CUR_B_5H | 5 A CT current , high                     |
|                 | TB3-2  | CUR_B_5L | 5 A CT current, low                       |
| Phase C current | TB3-3  | CUR_B_1H | 1 A CT current, high                      |
|                 | TB3-4  | CUR_B_1L | 1 A CT current, low                       |
|                 | TB4-1  | CUR_C_5H | 5 A CT current , high                     |
|                 | TB4-2  | CUR_C_5L | 5 A CT current, low                       |
|                 | TB4-3  | CUR_C_1H | 1 A CT current, high                      |
|                 | TB4-4  | CUR_C_1L | 1 A CT current, low                       |

## Operation

PGEN monitors generator 3-phase current and turbine mechanical power to provide the PLU over-speed control for large steam turbines.

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**Note** Test points are provided for all CT inputs to verify the phase in the field.

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Three single-phase CT inputs are provided with a normal current range of 0 to 5 A continuous or 0 to 1 A continuous. The CTs are magnetically isolated on TGNA. CTs connect to non-pluggable terminal blocks with captive lugs accepting up to #10 AWG wires. The total generator current is calculated from these inputs.

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**Note** High frequency and 50/60 Hz noise is reduced with an analog hardware filter.

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The three analog inputs accept 4-20 mA inputs or  $\pm 5$ ,  $\pm 10$  V dc inputs. A +24 V dc source is available for all three circuits with individual current limits for each circuit. The 4-20 mA transducers can use the +24 V dc source from the turbine control or a self-powered source. A jumper on TGNA selects between current and voltage inputs for each circuit. In a TMR system, analog inputs fan out to the three I/O packs (PGEN). The 24 V dc power to the transducers comes from all three PGEN packs, and is diode-shared on the TGNA.

## Specifications

| Item                     | Specification                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Inputs to TGNA and PGEN  | 3 one-phase generator CTs<br>3 analog inputs (4-20 mA, $\pm 5$ , $\pm 10$ V dc)                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Generator current inputs | Normal current range is 0 to 5 A with over-range to 10 A or<br>0 to 1 A with over-range to 2 A<br>Nominal frequency 50/60 Hz with range of interest 45 to 66 Hz<br>Magnetic isolation to 1,500 V rms<br>Input accuracy 0.5% of full scale (5 A or 1A) with resolution of 0.1% FS<br>Input burden less than 0.5 $\Omega$ per circuit                                                                                                                                                               |
| Analog inputs            | Current inputs: 4-20 mA<br>Voltage inputs: $\pm 5$ V dc or $\pm 10$ V dc<br>Transducers can be up to 300 m (984 ft) from the control cabinet with a two-way cable resistance of 15 $\Omega$ .<br>Input burden resistor on TGNA is 250 $\Omega$ .<br>Jumper selection of single ended or self powered inputs<br>Jumper selection of voltage or current inputs<br>Analog Input Filter: Breaks at 72 and 500 rad/sec<br>Ac common mode rejection (CMR) 60 dB<br>Dc common mode rejection (CMR) 80 dB |
| Conversion accuracy      | Sampling type 16-bit A/D converter, 14 bit resolution<br>Accuracy 0.1% overall                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Frame rate               | 720 or 600 Hz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Calculated values        | Total current<br>Mechanical power                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides out of sensor limits checks for each Turbine-Generator input. The I/O processor creates a diagnostic alarm (fault) if any one of the inputs has an out-of-range voltage/current.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

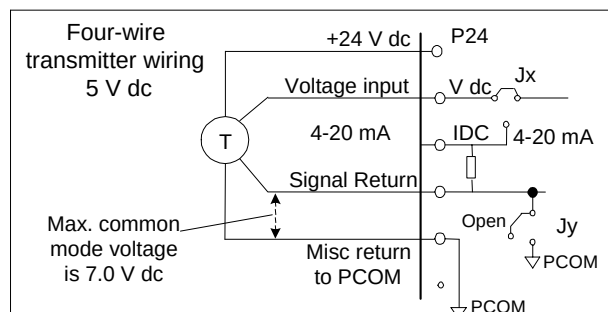
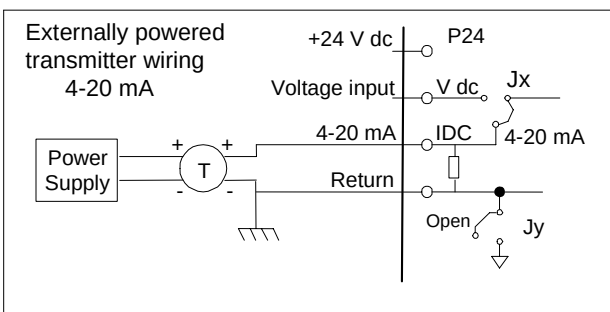
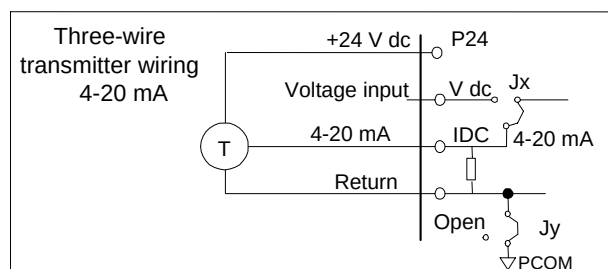
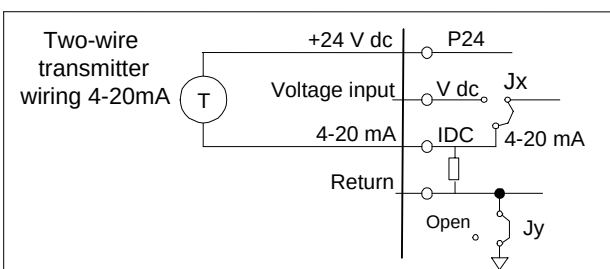
## Configuration

The terminal board is configured with jumpers. For location of these jumpers, refer to the installation diagram. The jumper choices are as follows:

- Jumpers JP1, JP3, and JP5 select either current (4-20 mA) input or voltage input
- Jumpers JP2, JP4, and JP6 select whether the return is connected to common (Return to GND) or is left open (differential input)

The following diagrams illustrate connections for common analog inputs.

All other configuration for PGEN is done from the ToolboxST. For the location of these jumpers, refer to the installation diagram.



For jumpers Jx and Jy:

x = 1, 3, 5

y = 2, 4, 6

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## ***Notes***

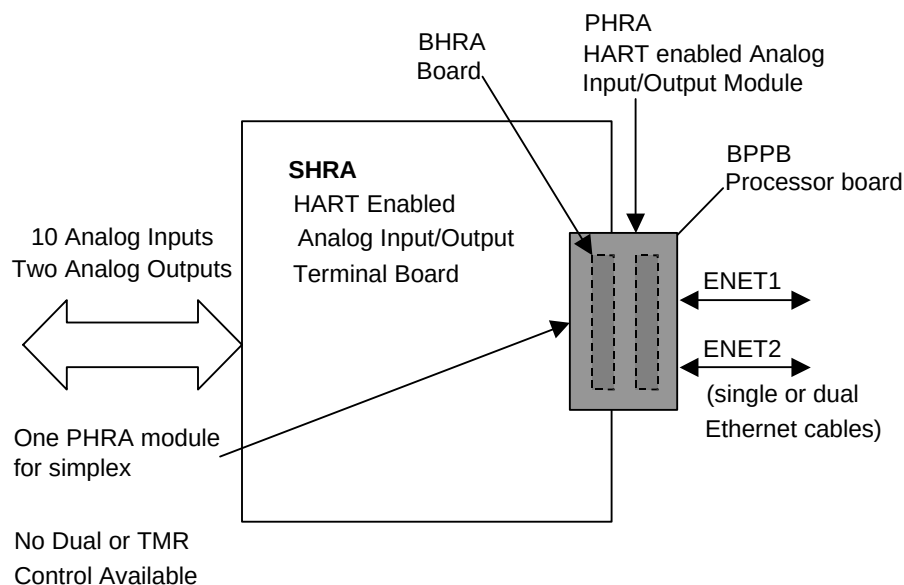
# PHRA HART Enabled Analog Input/Output

## PHRA HART Enabled Analog Input/Output

### Functional Description

The Highway Addressable Remote Transducer (HART<sup>®</sup>) Enabled Analog Input/Output (PHRA) pack provides the electrical interface between one or two I/O Ethernet networks and an analog input/output terminal board. This pack contains a processor board common to all Mark\* V1e distributed I/O packs and an acquisition board specific to the analog input function. The pack is capable of handling up to 10 analog inputs, the first eight of which can be configured as  $\pm 5$  V inputs, or 4-20 mA current loop inputs. The last two inputs may be configured as  $\pm 1$  mA or 4-20 mA current inputs. The load termination resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the PHRA. The PHRA also includes support for two 4-20 mA current loop outputs. In addition, in 4-20 mA mode the PHRA can relay HART messages between HART enabled field devices and an Asset Management System (AMS). These HART enabled field devices can be connected through any of the inputs or outputs.

Input to the pack is through dual RJ45 Ethernet connectors and a 3-pin power input. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



PHRA Block Diagram

## Compatibility

PHRA is compatible with the HART Enabled Analog Input Terminal Board (SHRA).

| Terminal Board | SHRA        |         |        |
|----------------|-------------|---------|--------|
| Control mode   | Simplex=yes | Dual=no | TMR=no |

Control mode refers to the number of I/O packs used in a signal path. Simplex uses one I/O pack with one or two network connections.

## Installation

### ➤ To install the PHRA pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PHRA I/O pack into the terminal board connector.
- 3 Mechanically secure the pack using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

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**Note** The PHRA mounts directly to a Mark VIe terminal board. Simplex terminal boards have a single DC-62 pin connector that receives the PHRA.

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## Operation

### Processor

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring



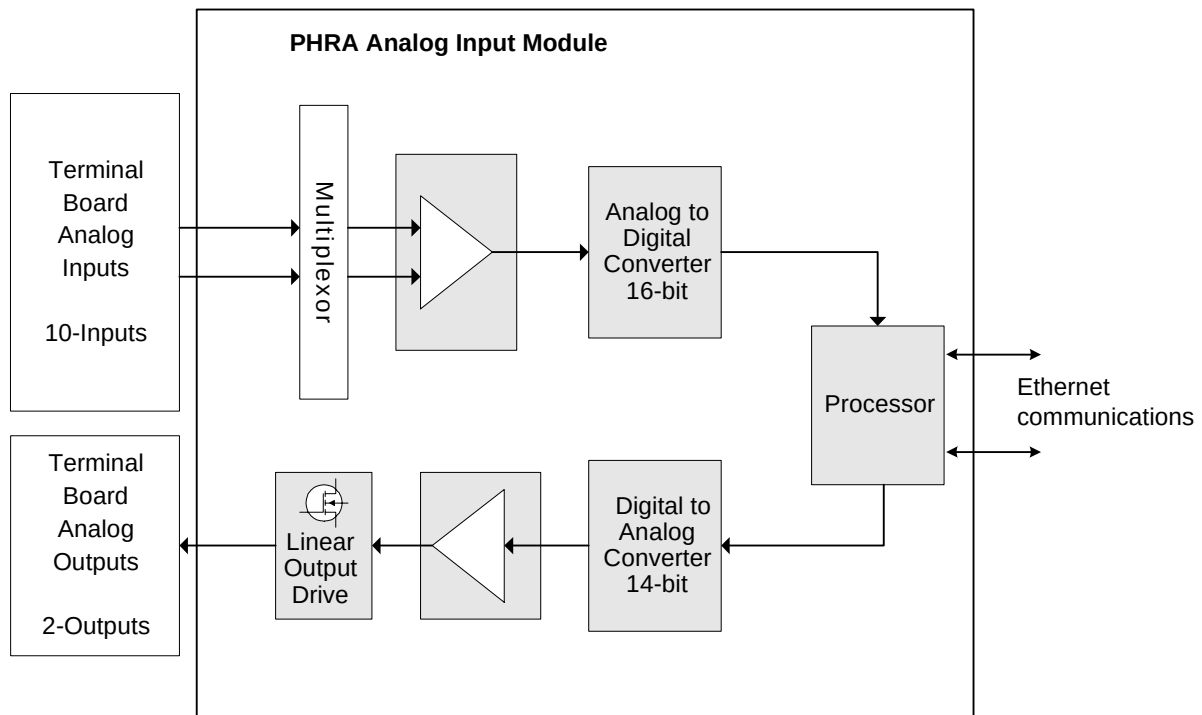
The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

### **Analog Input Hardware**

The PHRA accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an analog multiplexer block, several gain and scaling selections, and a 16-bit analog-to-digital converter (DAC).

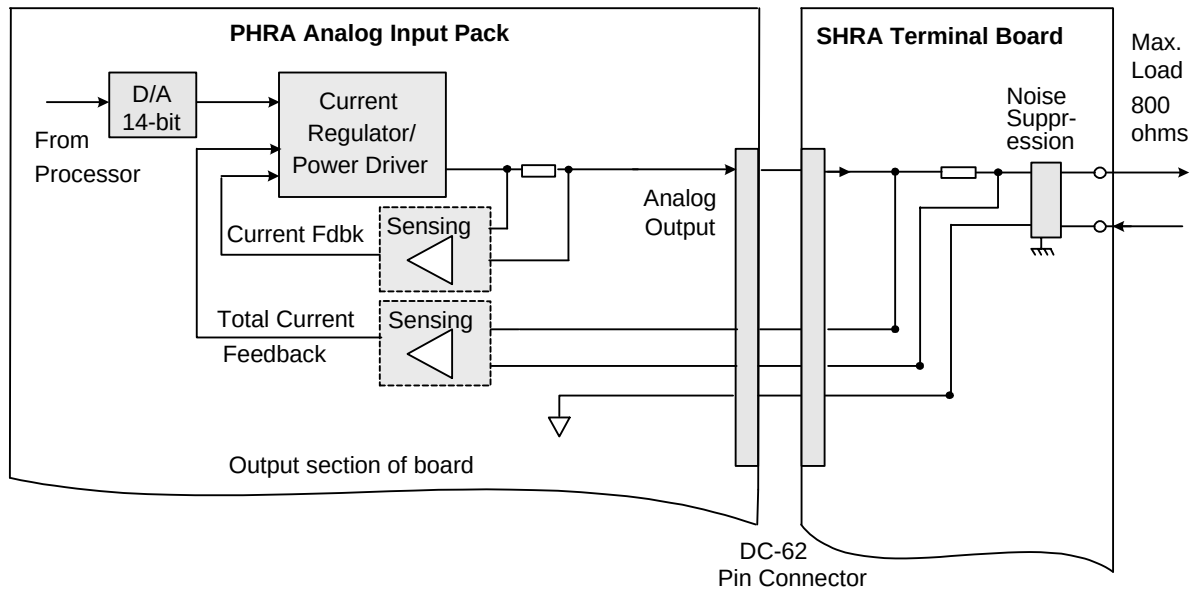


The inputs can be individually configured as  $\pm 5$  V scale signals, depending on the input configuration. The terminal board provides a  $250\ \Omega$  burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a second order, passive, low pass filter network with poles at 12.5 Hz and 48.3 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the PHRA analog input section.

### Analog Output

The PHRA includes two 4-20 mA analog outputs capable of 18 V compliance. A 14-bit DAC commands a current reference to the current regulator loop in the PHRA that senses current both in the PHRA pack and on the terminal board. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the PHRA)
- Total current (as sensed from the terminal board)



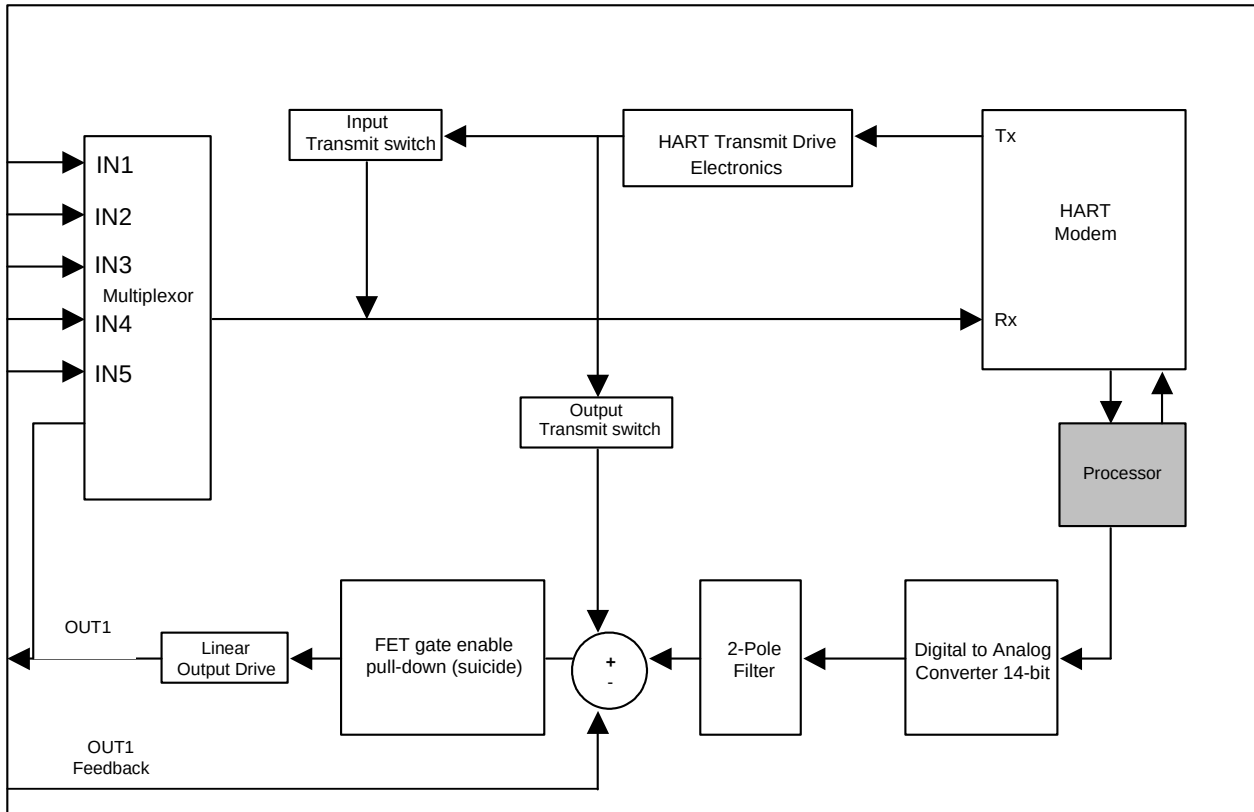
## ***HART Hardware***

All inputs and outputs on the BHRA are HART enabled. This means there are 12 individual HART channels, with 10 channels for the analog inputs and two channels for the outputs. These 12 channels are served by a pair of HART modems so that each modem is associated with six HART channels. Inputs 1 through 5 and output 1 are multiplexed down to HART modem A. Inputs 6 through 10 and output 2 are multiplexed down to HART modem B.

### *HART Modem Associations*

| <b>HART channel</b> | <b>PHRA I/O Analog</b> | <b>Served by Modem</b> |
|---------------------|------------------------|------------------------|
| 1                   | Input #1               | A                      |
| 2                   | Input #2               | A                      |
| 3                   | Input #3               | A                      |
| 4                   | Input #4               | A                      |
| 5                   | Input #5               | A                      |
| 6                   | Output #1              | A                      |
| 7                   | Input #6               | B                      |
| 8                   | Input #7               | B                      |
| 9                   | Input #8               | B                      |
| 10                  | Input #9               | B                      |
| 11                  | Input #10              | B                      |
| 12                  | Output #2              | B                      |

The number of active channels a modem is serving greatly impacts the HART data update time. If one of the six channels served by a HART modem is active, the modem is dedicated to a single field device and, under normal operating conditions, ToolboxST data associated with this device is updated roughly once per second. If all six channels are in use, roughly eight seconds will pass between updates. For more HART networking information refer to the *Network* section of *GEH-6721 Vol. I*.



*Analog I/O HART Interface – Quantity 2*

### **ID Line**

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-62 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

### **Power Management**

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

There are two yellow LEDs, HART TxA and HART TxB, that illuminate when a HART message is sent from the PHRA to a field device. The TxA serves inputs channels 1-5 and output channel 1, while the TxB serves inputs 6-10 and output channel 2.

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly (¼ cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed (¾ cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Specifications

| Item                        | Specification                                                                                                                                                                               |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels          | 12 channels per terminal board (10 AI, 2 AO)                                                                                                                                                |
| Input span                  | 4-20 mA dc, $\pm 5$ V dc, (Inputs 1-8)<br>4-20 mA or $\pm 1$ mA (Inputs 9-10)                                                                                                               |
| Input converter resolution  | 16-bit analog-to-digital converter                                                                                                                                                          |
| Scan time                   | Normal scan 5 ms (200 Hz). Note that controller frame rate is 100 Hz.                                                                                                                       |
| Measurement accuracy        | Better than 0.1% full scale over the temperature range 0 to 60°C. Typical accuracy at 25°C is 0.007% full scale.                                                                            |
| Noise suppression on inputs | The ten circuits have a hardware filter with two poles at 12.5 Hz and 48.3 Hz. A software filter, using a two-pole, low-pass filter, is configurable for: 0, .75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz |
| Common mode rejection       | Ac common mode rejection 60 dB @ 60 Hz, with up to $\pm 5$ V common mode voltage.<br>Dc common mode rejection 80 dB with -5 to +7 peak V common mode voltage                                |
| Common mode voltage range   | $\pm 5$ V                                                                                                                                                                                   |
| Output converter            | 14-bit D/A converter with 0.5% accuracy                                                                                                                                                     |
| Output load                 | 800 $\Omega$ for 4-20 mA output                                                                                                                                                             |
| <b>Physical</b>             |                                                                                                                                                                                             |
| Size                        | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)                                                                                                                    |
| Technology                  | Surface-mount                                                                                                                                                                               |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on preset (non-configurable) high and low levels near the end of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. The logic signal, L3DIAG\_xxxx, refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limits.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

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**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

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| Parameter               | Description                                                                                                                     | Choices          |
|-------------------------|---------------------------------------------------------------------------------------------------------------------------------|------------------|
| Configuration           |                                                                                                                                 |                  |
| System Limits           | Enable or disable system limits                                                                                                 | Enable, disable  |
| Min_ MA_Input           | Select minimum current for healthy 4-20 mA input                                                                                | 0 to 21 mA       |
| Max_ MA_Input           | Select maximum current for healthy 4-20 mA input                                                                                | 0 to 21 mA       |
| AMS_Msg_Priority        | AMS messages have priority over controlled messages,                                                                            | Enable, Disabled |
| AMS_Msgs_Only           | AMS messages only, do not send any control messages. Generates alarm 160 when enabled.                                          | Enable, Disabled |
| AMS_Mux_Scans_Permitted | Allow AMS scan commands for Hart message 1 and 2. Hart message 3 is always allowed                                              | Enable, Disable  |
| Max_MA_HART_Output      | Minimum current sent to a HART enabled port. HART COMM will not be possible during offline modes if value is set less than 4 mA | 0-22.5           |

| Parameter       | Description                                                                                                                                                                                                                                                                     | Choices                                        |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|
| :IS200SHRA      | Terminal board connected to PHRA                                                                                                                                                                                                                                                | Connected, not connected                       |
| AnalogIn1-10    | First of 10 Analog Inputs – board point                                                                                                                                                                                                                                         | (Input FLOAT)                                  |
| Input Type      | Current or voltage input type                                                                                                                                                                                                                                                   | Unused, 4-20 mA, $\pm 5$ V                     |
| Low_Input       | Value of current at the low end of scale                                                                                                                                                                                                                                        | -10 to +20                                     |
| Low_Value       | Value of input in engineering units at low end of scale                                                                                                                                                                                                                         | -3.4082 e + 038 to 3.4028 e + 038              |
| High_Input      | Value of current at the high end of scale                                                                                                                                                                                                                                       | -10 to +20                                     |
| High_Value      | Value of input in engineering units at high end of scale                                                                                                                                                                                                                        | -3.4082 e + 038 to 3.4028 e + 038              |
| Input_Filter    | Bandwidth of input signal filter                                                                                                                                                                                                                                                | Unused, 0.75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz        |
| Hart_Enable     | Allow the Hart Protocol on this IO point. This must be set to true if Hart messages are needed from this field device                                                                                                                                                           | Enable, Disable                                |
| Hart_Ctrl       | Number of variables to read from the device. Set to zero if not used.                                                                                                                                                                                                           | 0-5                                            |
| Hart_ExStatus   | Number of extended status bytes to read from the device. Set to zero if not needed for control.                                                                                                                                                                                 | 0-26                                           |
| Hart_MfgID      | Hart field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PHRA if the field device is connected. (Right-click on device name and select Update HART IDS) | 0-255                                          |
| Hart_DevType    | Hart Field Device – Type of device. (See Hart_MfgID)                                                                                                                                                                                                                            | 0-255                                          |
| Hart_DevID      | Hart Field Device – Device ID. (See Hart_MfgID)                                                                                                                                                                                                                                 | 0-116777215                                    |
| Sys Lim 1 Enabl | Input fault check                                                                                                                                                                                                                                                               | Enable, disable                                |
| Sys Lim 1 Latch | Input fault latch                                                                                                                                                                                                                                                               | Latch, unlatch                                 |
| Sys Lim 1 Type  | Input fault type                                                                                                                                                                                                                                                                | Greater than or equal Less than or equal       |
| Sys Lim 1       | Input limit in engineering units                                                                                                                                                                                                                                                | -3.4082 e + 038 to 3.4028 e + 038              |
| Sys Lim 2 Enabl | Input fault check                                                                                                                                                                                                                                                               | Enable, disable                                |
| Sys Lim 2 Latch | Input fault latch                                                                                                                                                                                                                                                               | Latch, unlatch                                 |
| Sys Lim 2 Type  | Input fault type                                                                                                                                                                                                                                                                | Greater than or equal. Less than or equal      |
| Sys Lim 2       | Input limit in engineering units                                                                                                                                                                                                                                                | -3.4082 e + 038 to 3.4028 e + 038              |
| DiagHighEnab    | Enable high input limit                                                                                                                                                                                                                                                         | Enable, disable                                |
| DiagLowEnab     | Enable low input limit                                                                                                                                                                                                                                                          | Enable, disable                                |
| AnalogOut1-2    | First of two analog outputs - board point                                                                                                                                                                                                                                       | Point edit (Output FLOAT)                      |
| Output_MA       | Type of output current, mA selection                                                                                                                                                                                                                                            | Unused, 0-20 mA                                |
| Output_State    | State of the outputs when offline                                                                                                                                                                                                                                               | PwrDownMode<br>Hold Last Value<br>Output_Value |
| Output_Value    | Pre-determined value for the outputs                                                                                                                                                                                                                                            |                                                |
| Low_MA          | Output mA at low value                                                                                                                                                                                                                                                          | 0 to 20 mA                                     |
| Low_Value       | Output in engineering units at low mA                                                                                                                                                                                                                                           | -3.4082 e + 038 to 3.4028 e + 038              |
| High_MA         | Output mA at high value                                                                                                                                                                                                                                                         | 0 to 20 mA                                     |
| High_Value      | Output value in engineering units at high mA                                                                                                                                                                                                                                    | -3.4082 e + 038 to 3.4028 e + 038              |
| D/A Err Limit   | Difference between D/A reference and output, in %                                                                                                                                                                                                                               | 0 to 100 %                                     |
| Hart_Enable     | Allow the Hart Protocol on this IO point. This must be set to true if Hart messages are needed from this field device                                                                                                                                                           | Enable, Disable                                |
| Hart_Ctrl       | Number of variables to read from the device. Set to zero if not needed for control.                                                                                                                                                                                             | 0-5                                            |

| Parameter       | Description                                                                                                                                                                                                             | Choices     |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Hart_ExStatus   | Number of extended status bytes to read from the device. Set to zero if not needed for control.                                                                                                                         | 0-26        |
| Update HART IDS | Hart field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the PHRA if the field device is connected. | 0-255       |
| Hart_DevType    | Hart Field Device – Type of device. (See Hart_MfgID)                                                                                                                                                                    | 0-255       |
| Hart_DevID      | Hart Field Device – Device ID. (See Hart_MfgID)                                                                                                                                                                         | 0-116777215 |

| Board Points (Signals) | Description - Point Edit (Enter Signal Connection) | Direction | Type  |
|------------------------|----------------------------------------------------|-----------|-------|
| L3DIAG_PHRA            | Board diagnostic                                   | Input     | BIT   |
| LINK_OK_PHRA           | Link diagnostic input                              | Input     | BIT   |
| ATTN_PHRA              | Module diagnostic                                  | Input     | BIT   |
| IOPackTmp              | I/O pack temperature                               | Input     | FLOAT |
| PS18V_PHRA_R           | I/O 18 V power supply indication                   | Input     | BIT   |
| PS28V_PHRA_R           | I/O 28 V power supply indication                   | Input     | BIT   |
| MuxHealth1             | Health bit for PHRA Hart multiplexer               | Input     | BIT   |
| SysLimit1_1            | System Limit 1                                     | Input     | BIT   |
| :                      | :                                                  | Input     | BIT   |
| SysLimit1_10           | System Limit 1                                     | Input     | BIT   |
| SysLimit2_1            | System Limit 2                                     | Input     | BIT   |
| :                      | :                                                  | Input     | BIT   |
| SysLimit2_10           | System Limit 2                                     | Input     | BIT   |
| Out1MA                 | Feedback, Total output current, mA                 | Input     | FLOAT |
| Out2MA                 | Feedback, Total output current, mA                 | Input     | FLOAT |



## Hart Signal Definitions

Each Hart field device has a set of HART signals that are read from the field device. These signals are prefixed with either HIx\_ or HOx\_ where x is 1-10 for input channels and 1-2 for output channels.

| Signal       | Type                | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Hxx_CommCnt  | Integer             | Number of times the CommStat signal was not zero after a HART message                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Hxx_CommStat | Bit encoded integer | Hart Communication status<br>Bit 1 – RX buffer overflow<br>Bit 3 – Checksum error<br>Bit 4 – Framing error<br>Bit 5 – Overrun error<br>Bit 6 – Parity error                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Hxx_DevCnt   | Integer             | Number of times the DevStat signal was not zero after a HART message.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Hxx_DevStat  | Bit encoded integer | Field Device Status: bits 0-7<br>Bit 0 – Primary variable out of limits<br>Bit 1 – Non primary var out of limits<br>Bit 2 – Analog output saturated<br>Bit 3 – Analog output current fixed<br>Bit 4 – More status available (ExStat)<br>Bit 5 – Cold start<br>Bit 6 – Configuration changed<br>Bit 7 – Field device malfunction<br><br>Command response byte: bits 8-15<br>2: Invalid selection requested<br>3: Passed parameter too large<br>4: Passed parameter too small<br>5: Too few bytes received<br>6: Device specific device error<br>7: In write protect mode<br>8-15: Device specific<br>16: Access restricted<br>32: Device is busy<br>64: Command not implemented |
| Hxx_DevRev   | Integer             | Field Device - Device revision code as read from the device.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Hxx_HwSwRev  | Integer             | Byte 0 - Field device software revision<br>Byte 1 - Field device hardware revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Hxx_mA       | Float               | Field Parm 1 – current reading of the primary signal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Hxx_PV       | Float               | Field Device Specific Control Parm 2 - Primary field device value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Hxx_SV       | Float               | Field Device Specific Control Parm 3 - Secondary value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Hxx_TV       | Float               | Field Device Specific Control Parm 4 -Third value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Hxx_FV       | Float               | Field Device Specific Control Parm 5 -Fourth value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Hxx_ExStat_1 | Bit Encoded         | Extended Status Bytes 1-4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Hxx_ExStat_2 | Bit Encoded         | Extended Status Bytes 5-8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Hxx_ExStat_3 | Bit Encoded         | Extended Status Bytes 9-12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Hxx_ExStat_4 | Bit Encoded         | Extended Status Bytes 13-16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Hxx_ExStat_5 | Bit Encoded         | Extended Status Bytes 17-20                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Hxx_ExStat_6 | Bit Encoded         | Extended Status Bytes 21-24                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Hxx_ExStat_7 | Bit Encoded         | Extended Status Bytes 25-26                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

The extended status bits are device-specific, and can be interrogated by using an AMS system. In general, the status bits are grouped as follows:

Bytes 0-5: Device specific status

Bytes 6-7: Operational modes

Bytes 8-10: Analog output saturation

Bytes 11-13: Analog output current fixed

Bytes 14-26: Device-specific

Each field device supports a specific number of control parameters and extended status bits. Refer to the *Field Device* documentation to determine the correct number and configure the ToolboxST application accordingly. A diagnostic alarm message will be generated if the Field Device and ToolboxST configuration do not match.

## Alarms

### PHRA Specific Alarms

| Alarm ID | Alarm Description         | Possible Cause                                                                               | Solution                                                                     |
|----------|---------------------------|----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| 32       | Analog Input 1 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 33       | Analog Input 2 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 34       | Analog Input 3 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 35       | Analog Input 4 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 36       | Analog Input 5 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 37       | Analog Input 6 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 38       | Analog Input 7 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 39       | Analog Input 8 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 40       | Analog Input 9 unhealthy  | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |
| 41       | Analog Input 10 unhealthy | Analog input [ ] is not within proper operating limits indicating a problem with the signal. | Check field wiring and configuration for the indicated analog input channel. |

| Alarm ID | Alarm Description                                              | Possible Cause                                                                                                                                                                                                      | Solution                                                                                                                            |
|----------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 42       | Analog Reference unhealthy                                     | Every scan the I/O pack reads the value of an internal precision voltage reference using an analog/digital converter. If the value does not fall within defined limits it indicates a hardware problem in the pack. | Replace I/O pack                                                                                                                    |
| 43       | Analog Null unhealthy                                          | Every scan the I/O pack reads a ground reference with the analog/digital converter. If the value does not fall within defined limits it indicates a hardware problem in the pack.                                   | Replace I/O pack                                                                                                                    |
| 44       | Analog Output 1 individual unhealthy                           | A problem has been detected on analog output [ ] indicating it is not tracking the commanded value.                                                                                                                 | Confirm correct field wiring and load.<br>Check output configuration.<br>Replace I/O pack                                           |
| 45       | Analog Output 2 individual unhealthy                           | A problem has been detected on analog output [ ] indicating it is not tracking the commanded value.                                                                                                                 | Confirm correct field wiring and load.<br>Check output configuration.<br>Replace I/O pack                                           |
| 46       | Analog Output 1 total unhealthy                                | Output current feedback [ ] as read from a sensor on the terminal board does not equal the commanded value.                                                                                                         | Confirm correct field wiring and load.<br>Check output configuration.<br>Replace SHRA, I/O pack                                     |
| 47       | Analog Output 2 total unhealthy                                | Output current feedback [ ] as read from a sensor on the terminal board does not equal the commanded value.                                                                                                         | Confirm correct field wiring and load.<br>Check output configuration.<br>Replace SHRA, I/O pack                                     |
| 48       | Analog Output 1 reference unhealthy                            | Internal read-back of the current command within the I/O pack does not agree with the expected value.                                                                                                               | Replace I/O pack                                                                                                                    |
| 49       | Analog Output 2 reference unhealthy                            | Internal read-back of the current command within the I/O pack does not agree with the expected value.                                                                                                               | Replace I/O pack                                                                                                                    |
|          | Logic Signal [ ] Voting Mismatch                               |                                                                                                                                                                                                                     |                                                                                                                                     |
|          | Input Signal [ ] Voting Mismatch, Local = [ ], Voted=[ ]       |                                                                                                                                                                                                                     |                                                                                                                                     |
| 66       | Output 1 Individual current too high relative to total current | A disagreement has been detected between the output current sensing inside the I/O pack and the current sensing on SHRA.                                                                                            | Check I/O pack mounting on SHRA.<br>Confirm correct field wiring and load.<br>Check output configuration.<br>Replace SHRA, I/O pack |
| 67       | Output 2 Individual current too high relative to total current | A disagreement has been detected between the output current sensing inside the I/O pack and the current sensing on SHRA.                                                                                            | Check I/O pack mounting on SHRA.<br>Confirm correct field wiring and load.<br>Check output configuration.<br>Replace SHRA, I/O pack |
| 70       | Output 1 Total current varies from reference current           | A disagreement has been detected between the output command sensing inside the I/O pack and the current sensing on SHRA.                                                                                            | Check I/O pack mounting on SHRA.<br>Confirm correct field wiring and load.<br>Check output configuration.<br>Replace SHRA, I/O pack |
| 71       | Output 2 Total current varies from reference current           | A disagreement has been detected between the output command sensing inside the I/O pack and the current sensing on SHRA.                                                                                            | Check I/O pack mounting on SHRA.<br>Confirm correct field wiring and load.<br>Check output configuration.<br>Replace SHRA, I/O pack |

| Alarm ID | Alarm Description                     | Possible Cause                                                                                        | Solution                                                                                                                                                        |
|----------|---------------------------------------|-------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 74       | Output 1 Reference current error      | Internal read-back of the current command within the I/O pack does not agree with the expected value. | Replace I/O pack                                                                                                                                                |
| 75       | Output 1 Reference current error      | Internal read-back of the current command within the I/O pack does not agree with the expected value. | Replace I/O pack                                                                                                                                                |
| 78       | Output 1 Individual current unhealthy | Output current feedback [ ] as read inside I/O pack does not equal the commanded value.               | Confirm correct field wiring and load.<br>Check output configuration.<br>Replace I/O pack                                                                       |
| 79       | Output 2 Individual current unhealthy | Output current feedback [ ] as read inside I/O pack does not equal the commanded value.               | Confirm correct field wiring and load.<br>Check output configuration.<br>Replace I/O pack                                                                       |
| 99       | Hart Input Channel 1 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 100      | Hart Input Channel 2 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 101      | Hart Input Channel 3 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 102      | Hart Input Channel 4 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 103      | Hart Input Channel 5 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 104      | Hart Output Channel 1 not initialized | Hart output channel 1 that was enabled does not respond.                                              | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 105      | Hart Input Channel 6 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 106      | Hart Input Channel 7 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 107      | Hart Input Channel 8 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 108      | Hart Input Channel 9 not initialized  | A Hart input channel [ ] that was enabled does not respond.                                           | Verify that the field device is attached to the correct IO point.<br>Independently confirm that the field device is operating correctly and should communicate. |

| Alarm ID | Alarm Description                      | Possible Cause                                                | Solution                                                                                                                                                         |
|----------|----------------------------------------|---------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 109      | Hart Input Channel 10 not initialized  | A Hart input channel [ ] that was enabled does not respond.   | Verify that the field device is attached to the correct I/O point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 110      | Hart Output Channel 2 not initialized  | Hart output channel 2 that was enabled does not respond.      | Verify that the field device is attached to the correct I/O point.<br>Independently confirm that the field device is operating correctly and should communicate. |
| 111      | Hart Input Channel 1 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 112      | Hart Input Channel 2 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 113      | Hart Input Channel 3 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 114      | Hart Input Channel 4 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 115      | Hart Input Channel 5 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 116      | Hart Output Channel 1 address mismatch | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 117      | Hart Input Channel 6 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 118      | Hart Input Channel 7 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 119      | Hart Input Channel 8 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 120      | Hart Input Channel 9 address mismatch  | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 121      | Hart Input Channel 10 address mismatch | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |
| 122      | Hart Output Channel 2 address mismatch | The device ID in the toolbox does not match the field device. | Verify that the correct field device is connected to the I/O point. If so, either set the ID field to 0s or upload the device ID from the field device.          |

| Alarm ID | Alarm Description                                            | Possible Cause                                                                                            | Solution                                                                                                   |
|----------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| 123      | Hart Multiplexer Modified                                    | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 124      | Hart Input Channel 1 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 125      | Hart Input Channel 2 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 126      | Hart Input Channel 3 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 127      | Hart Input Channel 4 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 128      | Hart Input Channel 5 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 129      | Hart Output Channel 1 Field Device Modified                  | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 130      | Hart Input Channel 6 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 131      | Hart Input Channel 7 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 132      | Hart Input Channel 8 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 133      | Hart Input Channel 9 Field Device Modified                   | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 134      | Hart Input Channel 10 Field Device Modified                  | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 135      | Hart Output Channel 2 Field Device Modified                  | Someone has modified the configuration of the field device with either AMS or a hand held monitor.        | Determine change and if OK, issue a system diagnostic reset to acknowledge the change and clear the fault. |
| 136      | Hart Input Chan 1 Control Parm Mismatch: cfg: [ ] found: [ ] | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration. | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.       |
| 137      | Hart Input Chan 2 Control Parm Mismatch: cfg: [ ] found: [ ] | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration. | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.       |

| Alarm ID | Alarm Description                                                        | Possible Cause                                                                                                 | Solution                                                                                             |
|----------|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| 138      | Hart Input Chan 3<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 139      | Hart Input Chan 4<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 140      | Hart Input Chan 5<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 141      | Hart Output Chan 1<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]   | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 142      | Hart Input Chan 6<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 143      | Hart Input Chan 7<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 144      | Hart Input Chan 8<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 145      | Hart Input Chan 9<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 146      | Hart Input Chan 10<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]   | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 147      | Hart Output Chan 2<br>Control Parm<br>Mismatch: cfg: [ ]<br>found: [ ]   | The number of dynamic variables returned in Hart Message 3 does not agree with the toolbox configuration.      | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 148      | Hart Input Chan 1<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ] | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration. | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 149      | Hart Input Chan 2<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ] | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration. | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 150      | Hart Input Chan 3<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ] | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration. | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 151      | Hart Input Chan 4<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ] | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration. | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |
| 152      | Hart Input Chan 5<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ] | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration. | Verify that the correct device is attached and set the toolbox value to either 0 or the value found. |

| Alarm ID | Alarm Description                                                            | Possible Cause                                                                                                        | Solution                                                                                                                                                                                         |
|----------|------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 153      | Hart Output Chan 1<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration.        | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.                                                                                             |
| 154      | Hart Input Chan 6<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ]     | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration.        | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.                                                                                             |
| 155      | Hart Input Chan 7<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ]     | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration.        | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.                                                                                             |
| 156      | Hart Input Chan 8<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ]     | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration.        | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.                                                                                             |
| 157      | Hart Input Chan 9<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ]     | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration.        | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.                                                                                             |
| 158      | Hart Input Chan 10<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration.        | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.                                                                                             |
| 159      | Hart Output Chan 2<br>Extended Status<br>Mismatch: cfg: [ ]<br>found: [ ]    | The number of extended status bytes returned in Hart Message 48 does not agree with the toolbox configuration.        | Verify that the correct device is attached and set the toolbox value to either 0 or the value found.                                                                                             |
| 160      | Hart Control<br>Messages disabled.<br>AMS Hart messages<br>only              | The AMS Messages Only parameter is enabled.                                                                           | Set the parameter to false and set each channels Hart_Ctrl and Hart_ExStatus to zero to get rid of the fault.                                                                                    |
| 161      | Hart Input Chan 1 -<br>Field device not write<br>protected in locked<br>mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 162      | Hart Input Chan 2 -<br>Field device not write<br>protected in locked<br>mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 163      | Hart Input Chan 3 -<br>Field device not write<br>protected in locked<br>mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 164      | Hart Input Chan 4 -<br>Field device not write<br>protected in locked<br>mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 165      | Hart Input Chan 5 -<br>Field device not write<br>protected in locked<br>mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |



| Alarm ID | Alarm Description                                                       | Possible Cause                                                                                                        | Solution                                                                                                                                                                                         |
|----------|-------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 166      | Hart Output Chan 1 -<br>Field device not write protected in locked mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 167      | Hart Input Chan 6 -<br>Field device not write protected in locked mode  | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 168      | Hart Input Chan 7 -<br>Field device not write protected in locked mode  | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 169      | Hart Input Chan 8 -<br>Field device not write protected in locked mode  | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 170      | Hart Input Chan 9 -<br>Field device not write protected in locked mode  | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 171      | Hart Input Chan 10 -<br>Field device not write protected in locked mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 172      | Hart Output Chan 2 -<br>Field device not write protected in locked mode | The field device for this channel is not in a write protected or secured mode while the controller is in locked mode. | Refer to the field device manual to determine how to place the device in the write protected mode. All devices used in a safety protected system must be able to be placed in a write only mode. |
| 173      | Reference Voltage out of limits                                         | The Reference voltage for the analog inputs is more than +5% from the expected value.                                 | Verify that the acquisition card for the pack is still functional. Replace I/O pack                                                                                                              |
| 174      | Null voltage out of limits                                              | The Null voltage for the analog inputs is more than 5% from the expected value.                                       | Verify that the acquisition card for the pack is still functional. Replace I/O pack                                                                                                              |

### ***I/O Pack Alarms***

| Fault | Fault Description                                     | Possible Cause                                                   |
|-------|-------------------------------------------------------|------------------------------------------------------------------|
| 2     | Flash memory CRC failure                              | Board firmware programming error (board will not go online)      |
| 3     | CRC failure override is active                        | Board firmware programming error (board is allowed to go online) |
| 4     | I/O pack in stand alone mode                          | Invalid command line option                                      |
| 5     | I/O pack in remote I/O mode                           | Invalid command line option                                      |
| 6     | Special user mode active. Now [ ]                     | Invalid command line option                                      |
| 7     | I/O pack – The I/O pack has gone to the offline state | Lost communication with controller                               |
| 16    | System limit checking is disabled                     | System checking was disabled by configuration                    |

| <b>Fault</b> | <b>Fault Description</b>                                                    | <b>Possible Cause</b>                                                                                                                                     |
|--------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30           | ConfigCompatCode mismatch; Firmware: [ ]                                    | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31           | IOCompatCode mismatch; Firmware: [ ]                                        | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256          | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                            |
| 257          | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                              |
| 258          | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                |
| 261          | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                |
| 262          | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                            |
| 263          | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                     |
| 264          | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                 |
| 265          | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                |
| 266          | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                |
| 267          | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                  |
| 268          | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                           |
| 269          | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                     |
| 270          | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                  |
| 271          | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                          |
| 272          | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                             |
| 273          | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                              |
| 274          | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                      |
| 275          | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                              |
| 276          | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                  |
| 277          | IONet-EGD – Signature mismatch E_Id= [ ]P_Id= [ ], =Expctd= [ ], Rcvd= [ ]  | Message version mismatch                                                                                                                                  |
| 278          | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                             |
| 293          | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                               |
| 301          | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                  |
| 314          | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                             |
| 315          | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                               |
| 316          | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                           |
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with minor signature different than expected                                                                           |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ]             | I/O pack outputs exchange received with configuration timestamp different than expected                                                                   |
| 335          | Code Segment CRC mismatch                                                   | Process Code Segment CRC mismatch                                                                                                                         |
| 338          | I/O pack Mapper SSI signals are not being updated                           | I/O pack SSI data is not being updated                                                                                                                    |
| 339          | I/O pack App SSO signals are not being received                             | I/O pack SSO data is not being updated                                                                                                                    |
| 340          | I/O pack Mapper static data structure CRC mismatch                          | Mapper static data CRC does not match                                                                                                                     |
| 341          | I/O pack Mapper I/O compatibility code mismatch                             | I/O pack mapper I/O Compat does not match firmware                                                                                                        |
| 342          | I/O pack App compatibility code mismatch                                    | I/O pack App I/O Compat does not match firmware                                                                                                           |
| 343          | I/O pack App BOPLIB static data CRC mismatch                                | I/O pack application data structure CRC changed                                                                                                           |

| <b>Fault</b> | <b>Fault Description</b>                        | <b>Possible Cause</b>                           |
|--------------|-------------------------------------------------|-------------------------------------------------|
| 344          | I/O pack process code segment CRC mismatch      | I/O pack process - code seg CRC bad             |
| 345          | I/O pack App static config data CRC mismatch    | I/O pack application data structure CRC changed |
| 351          | I/O pack App Periodic thread [ ] timing overrun | An I/O pack application thread over/under run   |
| 353          | Sys Config Shmem CRC mismatch                   | Config Shmem CRC changed                        |

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## ***SHRA HART Enabled Analog Input/Output***

### ***Functional Description***

The Highway Addressable Remote Transducer (HART<sup>®</sup>) Enabled Analog Input/Output (SHRA) terminal board is a compact analog input terminal board that accepts 10 analog inputs and two analog outputs, and connects to the PHRA pack. It allows HART messages to pass between the PHRA and a HART enabled field device. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The two analog outputs are 4-20 mA. Only a simplex version of the board is available.

High-density Euro-block type terminal blocks are used. An on-board ID chip identifies the board to the PHRA for system diagnostic purposes.

### ***Mark VI Systems***

The SHRA board is not compatible with Mark\* VI systems. These systems use a 37-pin D-type connector, which will not mate with the 62-pin connector found on the SHRA board.

### ***Mark VIe Systems***

In Mark VIe systems, the PHRA I/O pack works with the SHRA. The I/O pack plugs into the D-type connector and communicates with the controller over Ethernet. Only simplex systems are supported. All revisions of SHRA are compatible with all PHRAs.

## ***Installation***

The SHRA plus a plastic insulator mounts on a sheet metal carrier that then mounts on a DIN-rail. Optionally, the SHRA plus insulator mounts on a sheet metal assembly and then bolts directly to a cabinet. There are two types of Euro-block terminal blocks available as follows:

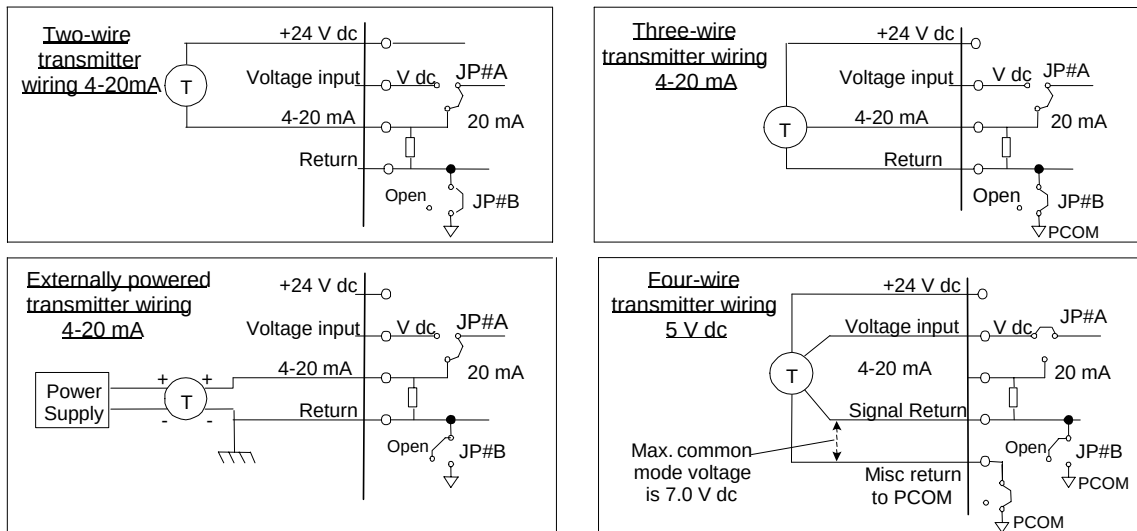
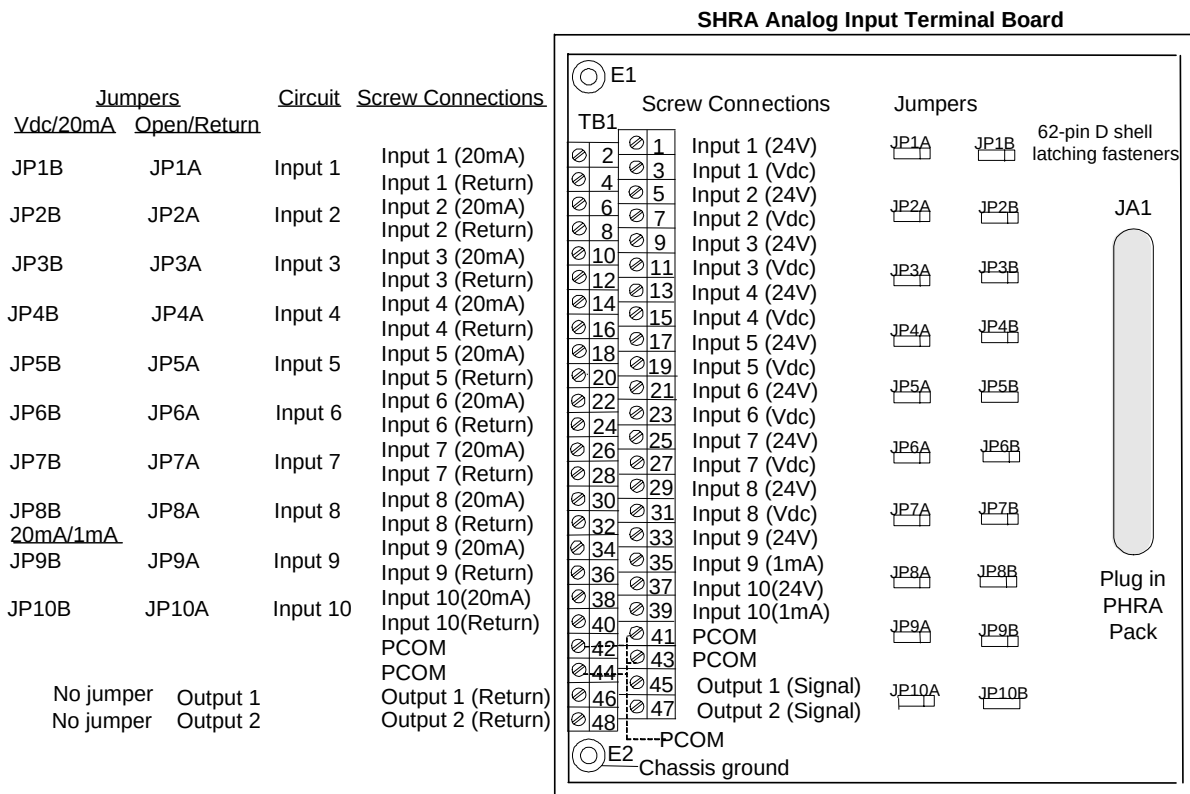
- SHRAH1 has a permanently mounted terminal block with 48 terminals.
- SHRAH2 has a right angle header accepting a range of commercially available pluggable terminal blocks, with 48 terminals.

Typically #18 AWG wires (shielded twisted-pair) are used. I/O cable shield termination is provided adjacent to the terminal blocks.

The following types of analog inputs/outputs can be used:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage  $\pm 5$  V dc
- Analog output, 4-20 mA current

Wiring, jumper positions, and cable connections appear on the wiring diagram.



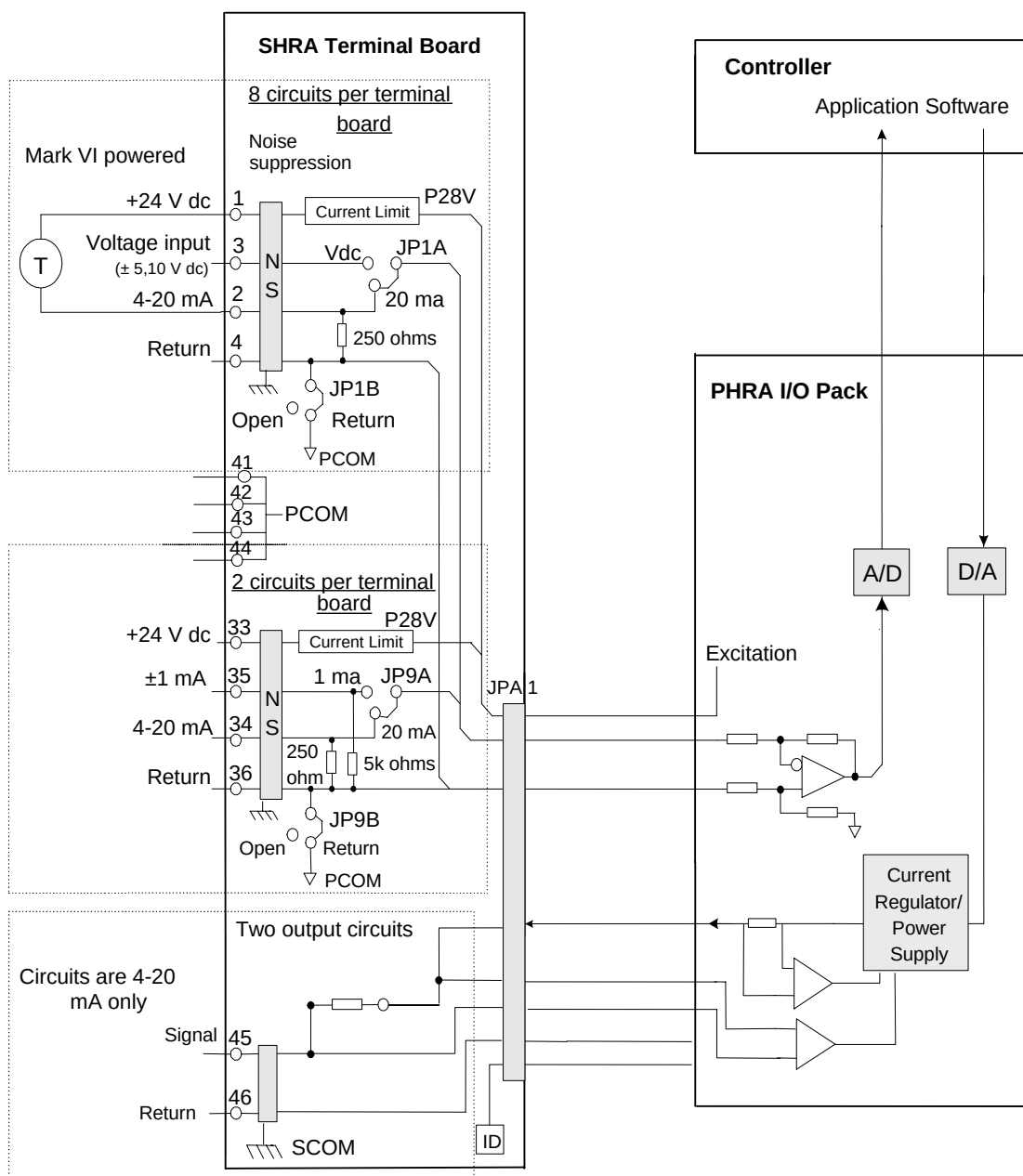
SHRA Wiring, Cabling, and Jumper Positions

## Operation

24 V dc power is available on the terminal board for all the transmitters (transducers). There is a choice of current or voltage inputs using jumpers. HART communication is only possible with the inputs set as 4-20 mA inputs, it will not take place on an input set as  $\pm 5$  V dc or  $\pm 1$  mA. The two analog output circuits are 4-20 mA. There is only one cable connection, so the terminal board cannot be used for TMR applications.

The following table displays the analog input/output capacity of the SHRA terminal board.

| Quantity | Analog Input Types       | Quantity | Analog Output Types |
|----------|--------------------------|----------|---------------------|
| 8        | $\pm 5$ V dc, or 4-20 mA | 2        | 4-20 mA             |
| 2        | 4-20 mA, or $\pm 1$ mA   |          |                     |



SHRA Terminal Board and PHRA I/O Pack

## Specifications

| Item                                    | Specification                                                                                                                   |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| Number of channels                      | 12 channels (10 AI, 2 AO)                                                                                                       |
| Input span, transmitters                | 1 - 5 V dc across a precision resistor (usually 250 $\Omega$ )                                                                  |
| Maximum lead resistance to transmitters | 15 $\Omega$ maximum two-way cable resistance, cable length up to 300 m (984 ft), 24 V outputs provide 21 mA for each connection |
| Outputs                                 | 24 V dc outputs rated at 21 mA each                                                                                             |
| Load on output currents                 | 800 $\Omega$ burden for 4-20 mA output with PHRA pack                                                                           |
| Physical                                |                                                                                                                                 |
| Size                                    | 15.9 cm high x 17.8 cm wide (6.25 in. x 7.0 in.)                                                                                |
| Technology                              | Surface-mount                                                                                                                   |

## Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

Configuration of the terminal board is by means of jumpers. For location of these jumpers refer to the installation diagram. The jumper choices are as follows:

- Jumpers JP1A through JP8A select either current input or voltage input
- Jumpers JP1B through JP8B select whether the return is connected to common or is left open
- Jumpers JP9A and JP10A select either 1 mA or 20 mA input current
- Jumpers JP9B and JP10B select whether the return is connected to common or is left open

All other configuration is for the PHRA and is done from the ToolboxST application.

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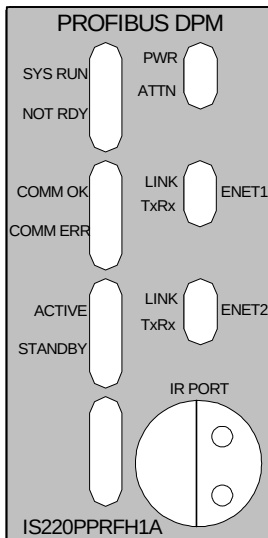
## ***Notes***



# PPRF PROFIBUS Master Gateway

## PPRF PROFIBUS Master Gateway

### Functional Description



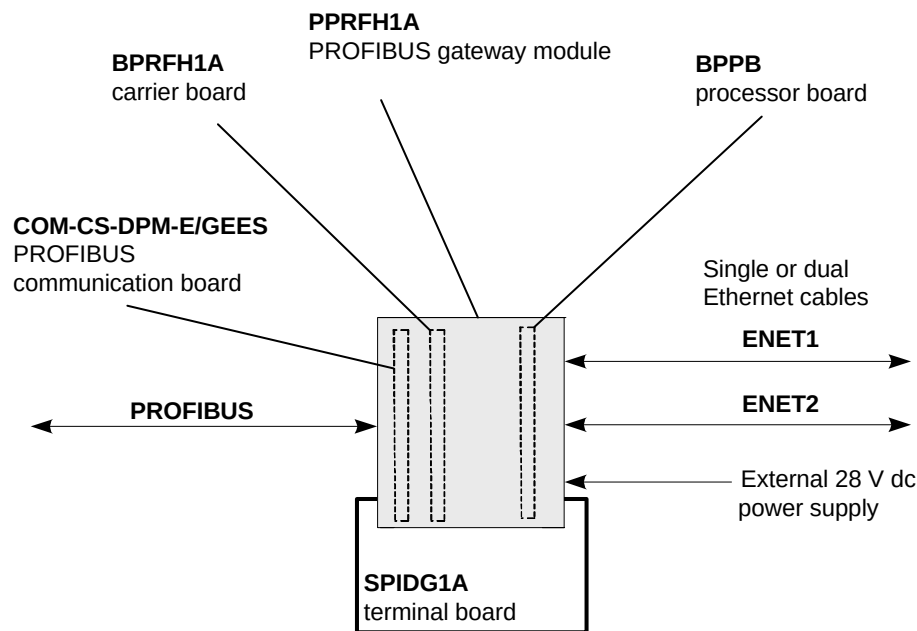
The PROFIBUS Master Gateway (PPRF) pack is a PROFIBUS DPV0, Class 1 master that maps I/O from PROFIBUS slave devices to Mark\* VIE controllers on the I/O Ethernet.

The module contains a processor board common to all Mark VIE distributed I/O modules and an acquisition carrier board fitted with a COM-C PROFIBUS communication module supplied by Hilscher GmbH. The COM-C module provides a PROFIBUS RS-485 interface through a DE-9 D-sub receptacle connector. It serves as a PROFIBUS DP master supporting transmission rates from 9.6 KBaud to 12 MBaud and up to 125 slaves with 244 bytes of inputs and outputs per slave.

The PPRF supports the following redundancy options:

- Single I/O pack with single I/O Ethernet connection (no redundancy)
- Single I/O pack with dual I/O Ethernet connections
- Hot-backup I/O pack with dual I/O Ethernet connections

The dual I/O Ethernet connection configuration is common to other IO packs. However, in the hot-backup two PPRFs are employed, one operating as the active PROFIBUS master communicating with slave devices, and the other operating in a passive, stand-by mode, ready to become the active master in the event of an active master failure



PPRF Simplified Diagram

## Compatibility

The PROFIBUS Master Gateway Terminal board (SPIDG1A) is used to mount the PPRF and to supply an electronic ID. Its only connection is the interface to the PPRF itself, as the PROFIBUS connection is made to the DE-9 D-sub receptacle connector exposed on the side of the PPRF. Visual diagnostics are provided through indicator LEDs on the PPRF. An infrared port provides local diagnostic serial communication.

### Terminal Board SPIDG1A

|              |             |          |        |                |
|--------------|-------------|----------|--------|----------------|
| Control mode | Simplex=yes | Dual =no | TMR=no | Hot-backup=yes |
|--------------|-------------|----------|--------|----------------|

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections
- Hot-backup uses two I/O packs with two network connections each

## Installation

### ➤ To install the PPRF pack

- 1 Securely mount the SPID terminal board.
- 2 Directly plug the PPRF into the terminal board connector. For hot-backup configurations, repeat steps 1 and 2 with a second SPID and PPRF.
- 3 Mechanically secure the packs using the threaded inserts adjacent to the Ethernet ports. The inserts connect to a mounting bracket specific to the terminal board type. The bracket should be adjusted so there is no right angle force applied to the DC-37 pin connector between the pack and the terminal board. This adjustment is required once during the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack operates over either port. If dual connections are used, standard practice is to hook ENET1 to the network associated with the R controller; however, the PPRF is not sensitive to Ethernet connections and will negotiate proper operation over either port.
- 5 Connect and secure the PROFIBUS cable into the DE-9 D-sub receptacle connector. As per PROFIBUS requirements, the PROFIBUS must be terminated on either end.
- 6 Apply power to the connector on the side of the pack. It is not necessary to insert the connector with power removed from the cable. The PPRF has inherent soft-start capability that controls current inrush on power application.
- 7 Using the ToolboxST\* application, configure the PPRF and PROFIBUS as necessary.

# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## ***PROFIBUS Gateway Hardware***

The PPRFs COM-C module, built on a PROFIBUS core based on Siemens ASPC2 technology, contains firmware that implements the PROFIBUS DP (Decentralized Periphery) functionality. Though the COM-C module is DPV1 capable, the PPRF only provides the basic DPV0 functionality, which includes configuring slave devices, cyclically exchanging I/O data with them, and obtaining PROFIBUS diagnostics.

The COM-C's firmware, residing in a flash memory, is released as part of the PPRF firmware and downloaded to the COM-C's flash at I/O pack startup time only if necessary (for instance when the PPRF firmware is released with an updated COM-C firmware).

The COM-C module requires a PROFIBUS configuration file that is created by the ToolboxST application. This file, specifying the DP master parameter set, is loaded from the ToolboxST application along with the other standard I/O pack configuration files, and, if changed, requires a PPRF reboot following the load. As is the case with the COM-C firmware file, the PROFIBUS configuration file is stored in COM-C flash and only downloaded from PPRF flash if necessary.

### ***Data Flow between PPRF and Controller***

Data flow between the PPRF and the controller is of two types, fixed I/O and PROFIBUS I/O. The limited amount of fixed I/O includes the inputs that are common to all I/O packs, for example L3DIAG and IOPackTmpr, but no application-driven outputs. The set of fixed I/O is pre-defined in the PPRF firmware. PROFIBUS I/O consists of the data exchanged with PROFIBUS slave devices, and its definition varies according to hardware configuration specified by the application.

The PPRF is guaranteed to handle 500 inputs and 500 outputs, half Boolean and half analog, at a 40 ms frame rate. The Boolean inputs may have input event detection enabled, and the analogs may be configured such that point-to-variable data type conversion and scaling take place. The PPRF does not place an architectural limit on the number of I/O points; the 500 input/output value is not a limit but a guarantee.

### ***Parameters and Online Loads***

In general, I/O pack parameters may be changed online, without restarting the system. PPRF parameters consist of I/O transfer scaling values and whether Boolean input event detection is enabled or not for given points. However, the PPRF also handles changes in point data type conversion and the addition and removal of variables attached to points through online loads, as long as the ToolboxST application command, Compress Variables is not done, which would rearrange the EGD exchange.

### ***PROFIBUS Diagnostics***

The PPRF receives and stores all PROFIBUS diagnostics generated by slave devices. In addition to any portion of the diagnostic data (including the standard and extended portions), controller applications receive an input Boolean that is set to True when PROFIBUS diagnostics have been received from one or more slave devices (diagnostics presence) and also receive input Booleans set to True to identify specific slave devices that have generated diagnostics (station diagnostics presence).

The ToolboxST application provides an Advanced Diagnostics command, as part of the Troubleshoot Module, which can be used to display any PROFIBUS diagnostics that are generated by slave devices.

## **Health**

Each PROFIBUS input has an associated health bit allocated in the inputs EGD exchange. The PPRF sets input health to unhealthy when any of the following conditions occur:

- Loss of communication between the associated slave device and the PROFIBUS master.
- Loss of COM-C module READY/RUN status.
- Standard I/O Ethernet input validation error.

PROFIBUS diagnostics other than the station diagnostics presence inputs, the Station\_Non\_Existent diagnostic, and the diagnostics presence input become unhealthy if any of the following conditions occur:

- The Station\_Non\_Existent diagnostic is True.
- Loss of COM-C module READY/RUN status.
- The slave is not configured in the master.

The station diagnostic presence inputs and Station\_Non\_Existent diagnostic inputs become unhealthy if either of the following conditions occur:

- Loss of COM-C module READY/RUN status.
- The slave is not configured in the master.

The diagnostics presence input becomes unhealthy when the following condition occurs:

- Loss of COM-C module READY/RUN status.

## **Input Events**

The PPRF optionally supports input Boolean sequence of event logging referred to as *input event* detection. PPRF input event time tagging has a 10 ms resolution.

## **Hot-backup Redundancy**

The PPRF supports a hot-backup redundancy configuration in which two PPRFs operate in tandem, one being the active master and the other retaining a standby status. The active master exchanges I/O with the PROFIBUS slaves and receives generated diagnostics. The backup master operates in standby mode, not communicating with the slave devices but ready to automatically assume the active role if any of the following occur:

- The active master loses communication connectivity with the PROFIBUS slaves (such as, the PROFIBUS cable is disconnected)
- The active master loses communication connectivity on both I/O Ethernet (such as, both Ethernet cables are disconnected or Ethernet switch connection, Ethernet cable disconnection combinations, and such, occur. Redundant Ethernet connections are required for each PPRF, and losing a single Ethernet does not cause a switch.)
- The active master is powered down or *fails*.

Since the switchover time is less than 200 ms, slave watchdog timeout values should not be set to less than that value so that the slaves do not timeout during the portion of the interval in which no PROFIBUS communication takes place. Given that the slave watchdog timeout is set sufficiently large, PROFIBUS I/O values should not spike or drop-out during the switchover period. They may, however, flat-line momentarily.

Unlike what is done in dual or TMR-pack cases, in the PPRF hot-backup configuration, the two PPRFs are assigned different producer IDs. Different controller application variables may be assigned to the fixed Class 1 inputs that are received from each pack (such as, L3Diag). The fixed inputs include an active/backup status Boolean from each PPRF (PROFI\_BACKUP\_PPRF\_R and PROFI\_BACKUP\_PPRF\_S, respectively).

Single application variables are assigned to the PROFIBUS I/O, and data exchange to and from those variables takes place regardless of which PPRF is active. When a backup-to-active switch occurs, the controller automatically switches data exchange between its variables and the newly active PPRF. The controller application takes no part in backup switching and does not have to supply PPRF-specific, separate variables for each PROFIBUS I/O point.

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**Note** If there is a partial PROFIBUS network failure, where both packs are able to communicate with different subsets of slave devices, I/O is only transferred with the slave devices that the primary master has access to. At the same time, the backup master does not try to transfer I/O to the slave devices it is connected to, unless a backup-to-active master switch is initiated. However, if this is done, transfers take place only with the slave devices connected to the newly active pack.

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## Specifications

| Item                         | PPRF Specification                                                                                                                                                                                                                                                                                                                 |
|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PROFIBUS Master type         | DPV0 Class 1 master                                                                                                                                                                                                                                                                                                                |
| PROFIBUS connection          | RS-485 interface through DE-9 D-sub receptacle connector                                                                                                                                                                                                                                                                           |
| Transmit time                | PROFIBUS output data from Mark VIe is received once per frame, up to 100 times per second and is asynchronously transmitted by the COM-C module to PROFIBUS slaves as fast as possible, governed by the PROFIBUS network baud rate, number of slaves, amount of I/O, and slave response time.                                      |
| Receive time                 | PROFIBUS inputs are asynchronously received by the PPRF COM-C module as fast as possible, governed by the PROFIBUS network baud rate, number of slaves, amount of I/O, and slave response time, then scanned by the PPRF firmware 100 times per second and transmitted to the Mark VIe once per frame, up to 100 times per second. |
| PROFIBUS transmission speeds | 9.6 KBaud to 12 MBaud                                                                                                                                                                                                                                                                                                              |
| Number of slaves             | 125 slaves with 255 bytes of inputs and outputs per slave                                                                                                                                                                                                                                                                          |
| I/O throughput               | 500 inputs and 500 outputs, half Boolean and half analog, at a 40 ms frame rate (Note: this is a requirement, not a hard limit)                                                                                                                                                                                                    |
| Input Event detection        | Available on input Booleans, 10 ms resolution                                                                                                                                                                                                                                                                                      |
| Size                         | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in. x 1.65 in. x 4.78 in.)                                                                                                                                                                                                                                                        |
| Technology                   | Surface mount                                                                                                                                                                                                                                                                                                                      |
| Temperature                  | Operating: -20 to 55°C (-4 to +131 °F)                                                                                                                                                                                                                                                                                             |

## ***Diagnostics***

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

If the following two LEDs (SYS RUN and NOT RDY) are off at the same time, either power is not applied or the COM-C module is being reset (which happens during an active to backup redundant PPRF transition). In all other conditions, one or the other LED will be on (though maybe flashing). The SYS RUN LED lights when the COM-C module's SYS LED is green; the NOT RDY LED lights when the COM-C module's SYS LED is yellow.

A green LED labeled SYS RUN indicates three different conditions as follows:

- LED solid on – the COM-C module has established communication with at least one PROFIBUS slave device
- LED flashing fast cyclically (5 Hz) – PROFIBUS master is configured and ready to communicate with slaves but is not connected or otherwise unable to communicate
- LED flashing non-cyclically (3 times at 5 Hz then 8 times between 0.5 Hz and 1 Hz) – the COM-C module is either missing a PROFIBUS configuration or its watchdog timer maintained with the I/O pack firmware has timed out (120 ms timeout)

A yellow LED labeled NOT RDY indicates three different conditions as follows:

- LED flashing slowly cyclically (1 Hz) – COM-C module is waiting for a firmware load
- LED flashing fast cyclically (5 Hz) – COM-C firmware download in progress
- LED flashing non-cyclically (3 times at 5 Hz then 8 times between 0.5 Hz and 1 Hz) – serious COM-C hardware for firmware error

A green LED labeled COMM OK mimics the COM-C COM LED when it is yellow:

- LED solid on – the COM-C module is holding the PROFIBUS token and is able to transmit PROFIBUS telegrams to slave devices
- LED flashing non-cyclically (between 0.5 Hz and 100 Hz) – the COM-C module is sharing the PROFIBUS token with other master devices on the network. This takes place in hot-backup configurations
- LED out – the COM-C is not communicating on the PROFIBUS network

A red LED labeled COMM ERR mimics the COM-C COM LED when it is red:

- LED solid on – the COM-C module has encountered a communication
- LED out – check COMM OK LED for communication status

Green LEDs labeled ACTIVE and STANDBY that are lit solidly in a mutually exclusive fashion:

- ACTIVE LED solid on – PPRF is the active master
- STANDBY LED solid on – PPRF is the backup master

## Alarms

### PPRF Specific Alarms

| Alarm ID | Alarm Description                                             | Possible Cause                                                                                                                                                                                                                                                 | Solution |
|----------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 32       | Unallowed VarIOCompatCode Change: Old - {0:F0}; New - {0:F0}. | An online load was attempted on a configuration change that requires a reboot.                                                                                                                                                                                 |          |
| 33       | VarIOCompatCode Mismatch: Pcode - {0:F0}; XML - {0:F0}.       |                                                                                                                                                                                                                                                                |          |
| 34       | Hilscher firmware downloaded to COM-C module.                 | PPRF firmware loaded with an updated COM-C firmware file that was loaded to the COM-C module                                                                                                                                                                   |          |
| 35       | Unable to download Hilscher firmware to COM-C module.         | A malfunction occurred when a new COM-C module firmware file was being loaded to the COM-C module                                                                                                                                                              |          |
| 36       | Unable to download configuration to Hilscher COM-C module.    | A malfunction occurred when a new PROFIBUS configuration was being loaded to the COM-C module                                                                                                                                                                  |          |
| 37       | Bad PROFIBUS configuraiton loaded to Hilscher COM-C module.   | An invalid PROFIBUS configuration file was downloaded to the COM-C module                                                                                                                                                                                      |          |
| 38       | Unable to activate/service COM-C HOST/DEVICE watchdog.        | The COM-C host watchdog (a ping between the host BPPB and COM-C device) could not be activated                                                                                                                                                                 |          |
| 39       | COM-C HOST/DEVICE watchdog timed out.                         | From the PPRF firmware perspective, the COM-C watchdog timed out (indicating failure of the COM-C firmware)                                                                                                                                                    |          |
| 40       | COM-C shutdown due to loss of READY/RUN or state < STANDBY.   | COM-C module shutdown by the PPRF firmware after a loss of its READY or RUN status or the I/O pack state falling below STANDBY. COM-C READY indicates firmware is running, and RUN indicates a valid configuration has been processed. Shutting down the COM-C |          |
| 41       | COM-C module unable to become active master.                  | Malfunction occurred in PPRF becoming the active PROFIBUS master                                                                                                                                                                                               |          |



| Alarm ID | Alarm Description                                            | Possible Cause                                                                                                                                                                                                             | Solution |
|----------|--------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 42       | COM-C module unable to become backup master.                 | Malfunction occurred in PPRF becoming the backup PROFIBUS master                                                                                                                                                           |          |
| 43       | Unable to obtain COM-C task state for diagnostic indication. | Unable to obtain slave diagnostic message status from COM-C module                                                                                                                                                         |          |
| 44       | PROFIBUS diagnostic present.                                 | A PROFIBUS diagnostic has been received from a slave device                                                                                                                                                                |          |
| 45       | Error obtaining PROFIBUS diagnostic.                         | Malfunction occurred obtaining a PROFIBUS diagnostic message from the COM-C module                                                                                                                                         |          |
| 46       | Error serializing PROFIBUS diagnostic message.               | A malformed PROFIBUS diagnostic was received from the COM-C module                                                                                                                                                         |          |
| 47       | Hilscher Firmware failed verification, download required.    | The firmware versions in redundant PPRFs do not match; startup prohibited                                                                                                                                                  |          |
| 48       | Firmware version mismatch in redundant PPRF's.               | Applicable to redundant configurations only, the I/O pack has remained in its WAIT startup state an inordinately long time, not able to detect the partner pack or detecting a firmware mismatch between the two I/O packs |          |
| 49       | Redundant PPRF pack not heard or f/w rev mismatch detected.  | Applicable to redundant configurations only, the I/O pack has not heard from its partner over the I/O Ethernet (on which it continually exchanges peer-to-peer status messages)                                            |          |
| 50       | Redundant PPRF pack peer-to-peer communication timeout.      | The active master has lost COM, indicating that it is not able to communicate with any PROFIBUS slave devices                                                                                                              |          |
| 51       | Active master PPRF COM lost.                                 | Applicable to redundant configurations only, the backup I/O pack is not able to communicate with the active master over the PROFIBUS network (on which it continually exchanges a status message)                          |          |
| 52       | Backup master PPRF COM lost.                                 | Applicable to redundant configurations only, the backup I/O pack is not able to communicate with the active master over the PROFIBUS network (on which it continually exchanges a status message)                          |          |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

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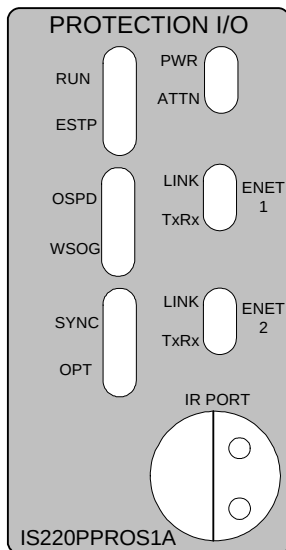
## ***Notes***

# PPRO Turbine Protection

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## PPRO Emergency Turbine Protection

### Functional Description



The Emergency Turbine Protection (PPRO) pack, and associated terminal boards provide an independent backup overspeed protection system with a backup check for generator Synchronization to a utility bus. They also provide an independent watchdog function for the primary control. A typical protection system consists of three triple modular redundant (TMR) PPRO I/O packs mounted to a separate simplex protection (SPRO) terminal board. A cable, with DC-37 pin connectors on each end, connects each SPRO to the designated emergency trip board:

- TREG: Gas Turbine Emergency Trip Terminal Board
- TREL: Large Steam Turbine Emergency Trip Terminal Board
- TRES: Small/Medium Steam Turbine Emergency Trip Terminal Board
- TREA: Turbine Emergency Trip Terminal Board

An alternate arrangement puts three PPRO I/O packs directly on TREA for a single-board TMR protection system.

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**Note** PPRO also has an Ethernet connection for IONet communications with the control modules.

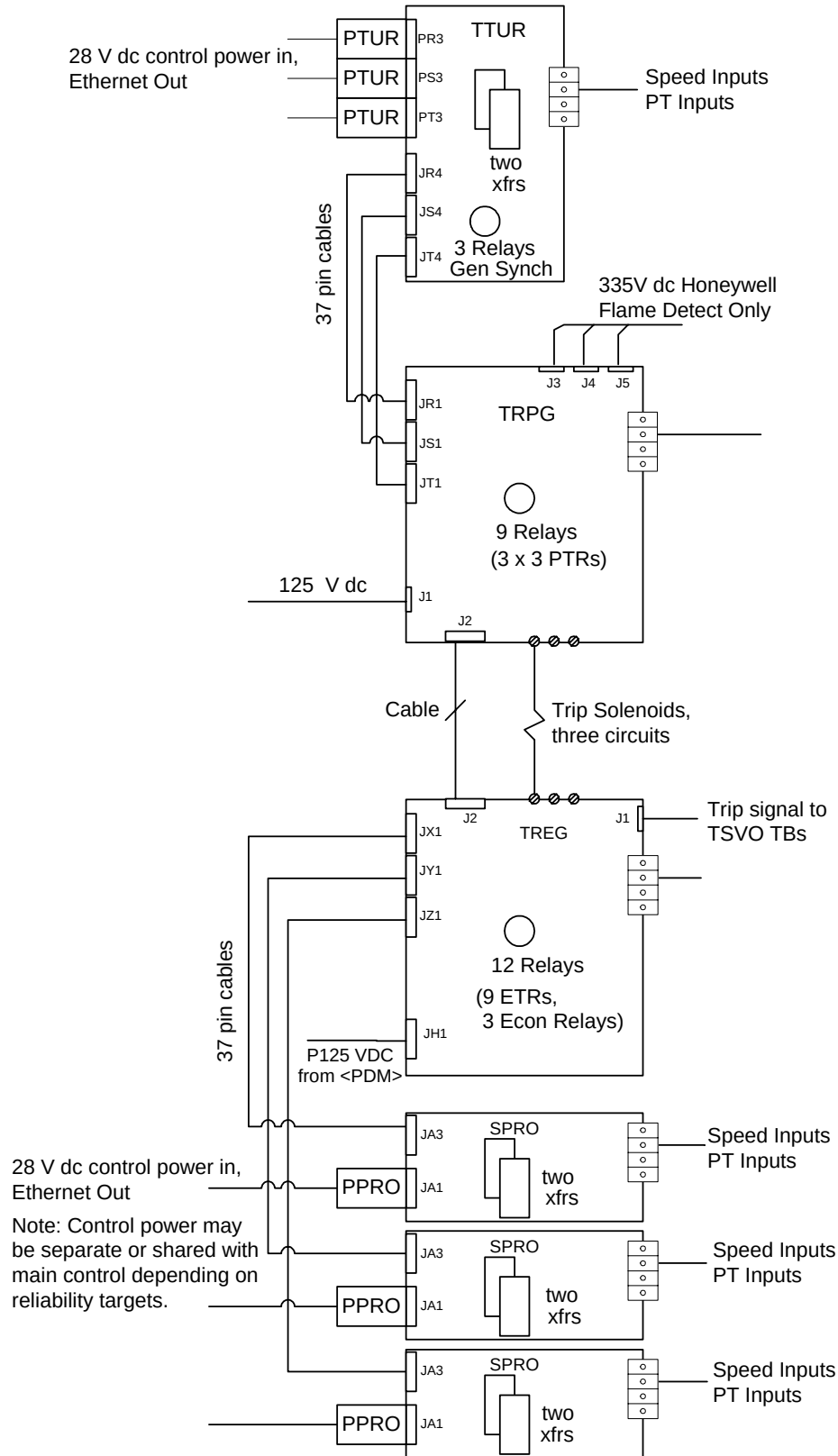
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Mark\* VIe is designed with a primary and backup trip system that interacts at the trip terminal board level. Primary protection is provided with the Turbine Primary I/O pack, PTUR, operating a primary trip board (TRPG, TRPL, TRPS, TRPA). Backup protection is provided with the PPRO I/O pack operating a backup trip board (TREG, TREL, TRES, TREA).

PPRO accepts three speed signals, including basic overspeed, acceleration, deceleration, and a hardware implemented overspeed. The pack monitors the operation of the primary control and can monitor the primary speed as a sign of normal operation. PPRO monitors the status and operation of the selected trip board through a comprehensive set of feedback signals. If a problem is detected, PPRO will trip the backup trip relays on the trip board and activate a trip on the primary control. The pack is fully independent of and unaffected by the primary control operation.

A maximum of three trip solenoids can be connected between the primary and emergency trip terminal boards. Connecting a solenoid between the boards isolates the power on both sides of the solenoid as well as visibility of solenoid voltage as a system feedback. The primary/emergency trip boards TRPG/TREG, TRPL/TREL, and TRPS/TRES are designed to operate as a pair and use cabling between the boards for system connections. TRPA and TREA are designed with no pairing required and can be used independently of each other. When TRPA and TREA are paired, they function the same as other board pairs.

The following figure shows how the TTUR and PPRO processor boards share in the turbine protection scheme. Either one can independently trip the turbine using the relays on TRPG or TREG.



PPRO Turbine Control and Protection Boards

## Compatibility

PPROH1A mounts directly on either SPRO or TREA. When mounted on SPRO, it is cable-compatible with TREG, TREL, and TRES in the following table.

*Terminal Board Compatibility*

| Board   | TMR | Simplex | Output<br>Contacts,<br>125 V dc | Output<br>Contacts,<br>24 V dc | ESTOP | Input<br>Contacts,<br>125 V dc | Input<br>Contacts,<br>24 V dc | Economy<br>Resistor |
|---------|-----|---------|---------------------------------|--------------------------------|-------|--------------------------------|-------------------------------|---------------------|
| TREGH1B | Yes | No      | Yes                             | Yes                            | Yes   | Yes                            | No                            | Yes                 |
| TREGH2B | Yes | No      | Yes                             | Yes                            | Yes   | No                             | Yes                           | Yes                 |
| TRELH1A | Yes | No      | Yes                             | Yes                            | No    | Yes                            | No                            | No                  |
| TRELH2A | Yes | No      | Yes                             | Yes                            | No    | No                             | Yes                           | No                  |
| TRESH1A | Yes | Yes     | Yes                             | Yes                            | No    | Yes                            | No                            | No                  |
| TRESH2A | Yes | Yes     | Yes                             | Yes                            | No    | No                             | Yes                           | No                  |
| TREAH1A | Yes | No      | Yes                             | No                             | Yes   | No                             | No                            | No                  |
| TREAH2A | Yes | No      | No                              | Yes                            | Yes   | No                             | No                            | No                  |

### Simplex Main Control

**Simplex backup protection** is supported by the Mark VIe trip board TRES. One PPRO network port resides on the controller IONet.

**TMR backup protection** is supported by all Mark VIe backup trip boards, TREG, TREL, TREA, and TRES. In this configuration, one port on each of three PPRO I/O packs hooks into the controller IONet.

### Dual Main Control

**Simplex backup protection** is supported by the Mark VIe trip board TRES. When used in this configuration, the first network connection is to the R controller. The second network connection is to the S controller. PPRO is then responsible for monitoring the operation of both controllers. PPRO supports two options: The pack trips if either controller malfunctions or both controllers malfunction.

**TMR backup protection** is supported by all Mark VIe backup trip boards, TREG, TREL, TREA, and TRES. This configuration uses the dual controller TMR output standard network connection. The first PPRO pack has one network port connected to the R controller network. The second pack has one network port connected to the S controller network. The third pack has one network port connected to the R controller network and one network port connected to the S controller network. The third PPRO monitors the operation of both controllers. The pack trips if either controller malfunctions or both controllers malfunction.

### Triple Main Control

**Simplex backup protection** is not supported as a simplex backup. One PPRO cannot monitor the health of all three main controls and trip on loss of a single main control. Therefore, one of the fundamental protection features cannot be met with a single pack.

**TMR Backup protection** is supported when operating with a TMR main control (two out of three running). All Mark VIe backup trip boards (TREG, TREL, TREA, and TRES) support this configuration. The normal network configuration connects the first PPRO pack to the R network, the second pack to the S network, and the third pack to the T network.

---

**Note** PPRO TMR applications do not support dual network connections for all three PPROs. In a redundant system there is no additional system reliability gained by adding network connections to the first two PPROs with dual controllers or any of the three PPROs with TMR controllers. The additional connections simply reduce mean time between failures (MTBF) without increasing mean time between forced outages (MTBFO).

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## ***Installation***

The PPRO mounts directly to a Mark VIe SPRO or TREA terminal board. When mounted on a SPRO board, cables with DC-37 pin connectors on both ends are required between the SPRO board and the selected trip terminal board. The installation steps are as follows:

### **➤ To install the PPRO pack**

- 1** Securely mount the SPRO or TREA terminal board. Mount the selected trip terminal board if SPRO is used.
- 2** Connect cable, with DC-37 pin connectors on each end, between SPRO and the selected trip terminal board if TREA is not used.
- 3** Directly plug one PPRO module into each SPRO, or three PPRO modules into TREA.
- 4** Slide the threaded posts on PPRO, located on each side of the Ethernet ports, into the slots on the terminal board mounting bracket. Adjust the bracket location so the DC-62 pin connector on PPRO and the terminal board fit together securely. Tighten the mounting bracket. The adjustment should only be required once in the life of the product. Securely tighten the nuts on the threaded posts locking PPRO in place.
- 5** Plug in one or two Ethernet cables depending on the system configuration. The PPRO module is not sensitive to Ethernet connections and selects the proper operation over either port.
- 6** Apply power to the module by plugging in the power connector on the side of the module. The I/O module has inherent soft-start capability that controls current levels upon application.
- 7** Configure the I/O module as necessary.



# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

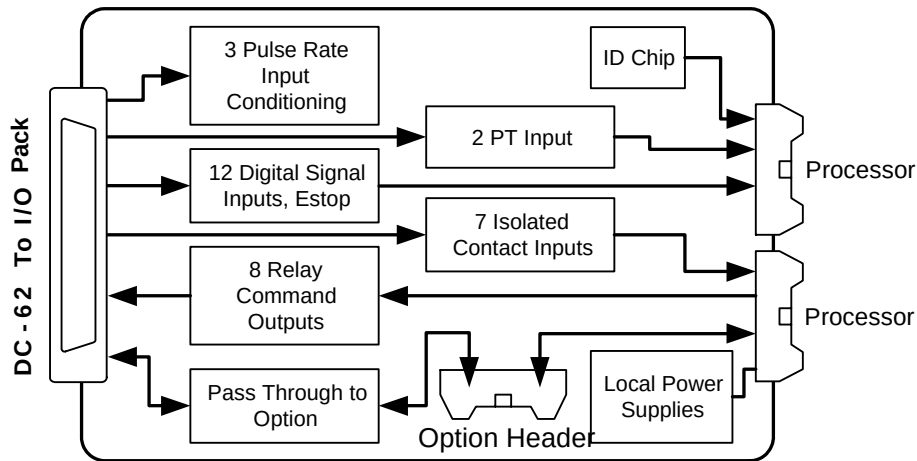
The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## Application Hardware

The PPRO I/O pack has an internal application specific circuit board that contains the hardware needed for the emergency trip function. The application board connects between the processor and either the SPRO or TREA terminal boards. The board has provisions for additional hardware expansion options. The options can be added to the I/O pack through a dedicated header. The diagram on the following page shows the functions of this board.



*PPRO Application Specific Circuit Board*

The processor and acquisition boards within the pack contain electronic ID parts that are read during power application. A similar part located with each terminal board connector allows the processor to confirm correct matching of the I/O pack to the terminal board and to report board revision status to the system level control.

The pack includes power management in the 28 V input circuit. The management function provides a soft-start feature to control current inrush during power application. After power is applied, the circuit provides a fast current limit function to prevent a pack or terminal board failure from generating back onto the 28 V power system. When power is present and working properly the green PWR LED will light. If the current limit function operates, the LED will be out until the problem is cleared.

## Status LEDs

There are six LEDs associated with the processor on the right side of the PPRO faceplate, which display the general status of the pack hardware and communications as follows:

**PWR** - A green LED is provided to show the presence of control power.

**ATTN** - A red LED is provided to show pack status. This LED indicates four different conditions as follows:

- LED out – there are no problems with the pack.
- LED solid on – a critical fault is present that prevents the pack from operating. Critical faults include detected hardware failures on the processor or acquisition boards, or the absence of loaded application code.
- LED flashing quickly (¼ second cycle) – alarm condition present. Alarm could be putting the wrong pack on the terminal board, no terminal board, or errors loading the application code.
- LED flashing at medium speed (¾ second cycle) – the pack is not online yet.
- LED flashing slowly (2 second cycle) – the pack has received a request to flash the LED to draw attention to the pack. This is used during factory test or as an aid to confirm physical location against Control System Toolbox settings.

**A green LINK LED** is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

**A yellow TxRx LED** is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

There are six additional LEDs located on the left side of the PPRO faceplate used for trip status. All six LEDs stay off until all PPRO hardware application is complete. The LEDs indicate trip status of the PPRO as follows:

**RUN** is green any time the PPRO has energized the emergency trip relays. RUN turns red any time PPRO has removed power from the emergency trip relays, voting to trip.

**ESTP** is green when the ESTOP input (if applicable) is in the run state. ESTP turns red any time ESTOP is invoked to prevent pick-up of the emergency trip relays. If the chosen trip terminal board doesn't support ESTOP then the LED defaults to green.

**OSPD** turns red any time PPRO votes to trip in response to a detected overspeed condition on any of the three speed inputs. OSPD is green when an overspeed condition is not present or latched.

**WDOG** turns red any time there is an alarm in the PPRO that has not been cleared. WDOG turns green to indicate all alarms in PPRO have been cleared.

**SYNC** is green when generator and bus voltage is synchronized and matched in amplitude. SYNC turns red when PPRO determines that AC bus and Generator bus voltage does not satisfy the synchronization requirements and synchronization has been requested by the system.

**OPT** is reserved for options that expand the capabilities of PPRO. The default display is green.

During normal PPRO operation, all six application LEDs display green. An additional feature, rotating LEDs, can be configured for the pack. Using this feature, only one LED is turned on at a time and walked up and down the six LEDs creating a Synchronized motion. The walking is regulated by the controller IONet and Synchronized across a set of three PPRO packs. This provides a quick visual indication of the system time Synchronization status.

## Connectors

A DC-62 pin connector on the underside of the PPRO pack connects directly to the terminal board. The connector contains the signals needed to sense inputs and operate a trip terminal board.

An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.

A second RJ45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.

A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

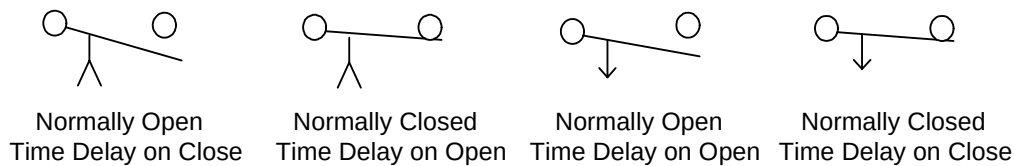
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**Note** If the trip terminal board features contact trip inputs, the power for those contacts is provided through a separate terminal board connector, not from the 28 V dc power source.

---

## Protective Functions

The PPRO performs the following protective functions in a mix of hardware, programmable logic, and firmware. In the following diagram, standard symbols for time delay contacts have been used:



In the following diagrams, a standard has been used to indicate signal origin and flow.

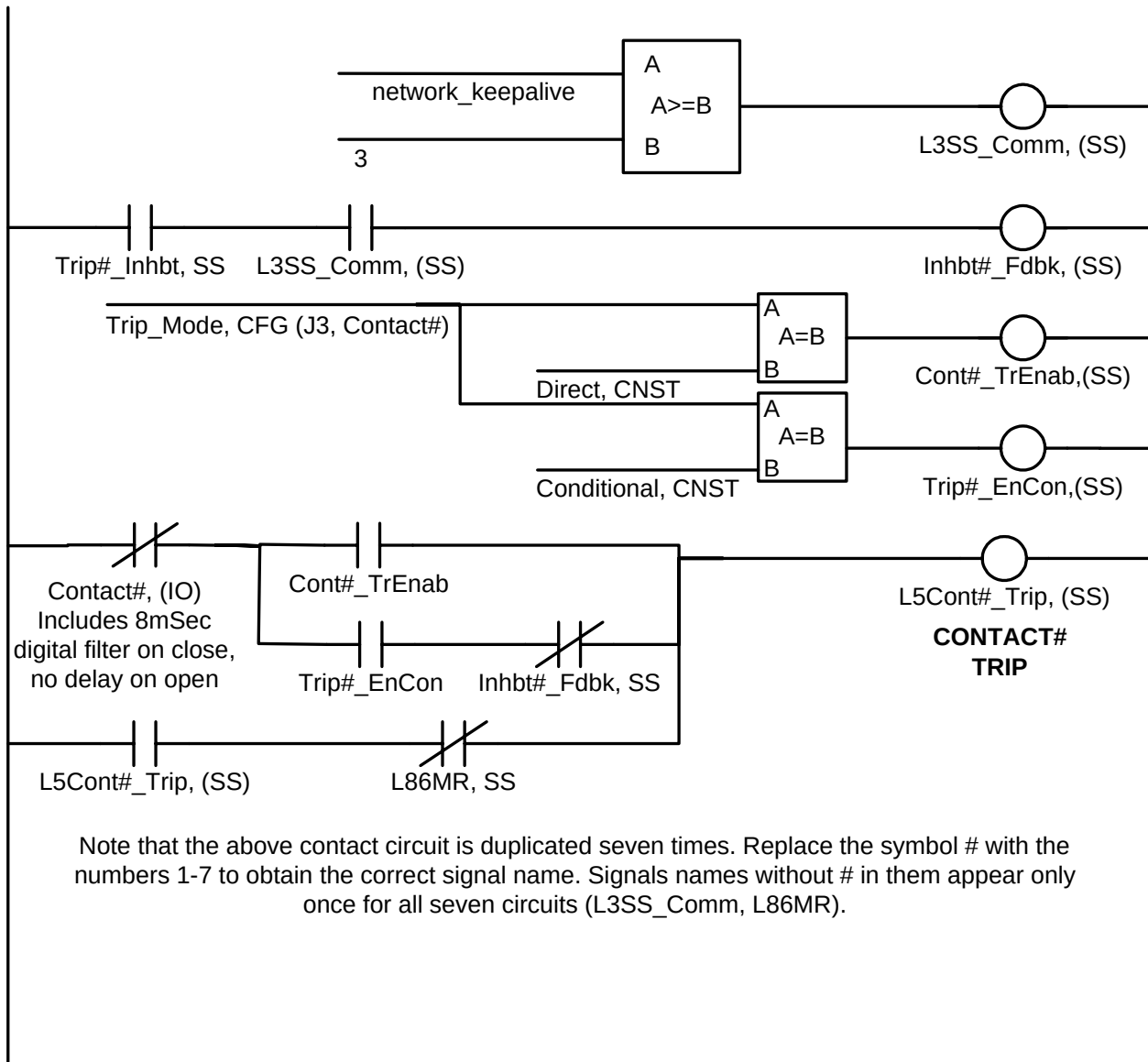
- Signal names that end with (SS) are created within PPRO and the data flow is out to the controller through signal space.
- Signal names that end with SS are created in the controller and the data flow is into PPRO through signal space.
- Signal names that end with (IO) are created within PPRO and the data flow is out to the hardware.
- Signal names that end with IO indicate the signal is a hardware input into PPRO.
- Signal names that end with anything containing CFG are part of the PPRO configuration. In this case an attempt has been made to indicate what area of the PPRO configuration contains the variable.
- When J3 is referenced in a CFG, it refers to the connection point for the trip relay board, TREA, TREG, or TREL and the corresponding configuration values.
- The combination IO (SS) indicates a signal that comes from the hardware inputs to PPRO, and is then sent out to the controller as part of signal space.

If there is no special ending on a signal name, then the signal is used internal to PPRO and is not part of the hardware or signal-space data movement. This signal is not available or visible to applications, but it is needed to adequately describe the packs operation.

## Direct/Conditional Discrete Input Trip

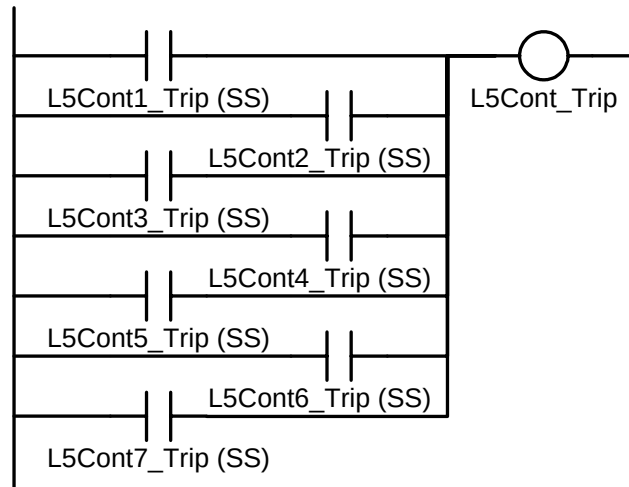
PPRO supports the seven isolated discrete contact input trip signals provided on the TREG, TREL, and TRES boards. In the following figure, the direct / conditional determination is implemented in firmware while Contact#, and L5Cont#\_Trip are in hardware logic. When configured for direct trip, the firmware is not in the trip path. When configured for conditional trip, the firmware determines the communication health (shown as network\_keepalive) and populates the programmable logic with the conditional signal from signal space. If the controller communication is lost, the default will permit any conditional trip.

**Note** The contact inputs include an 8 ms contact de-bounce filter to protect against false trips.



PPRO Contact Input Trips

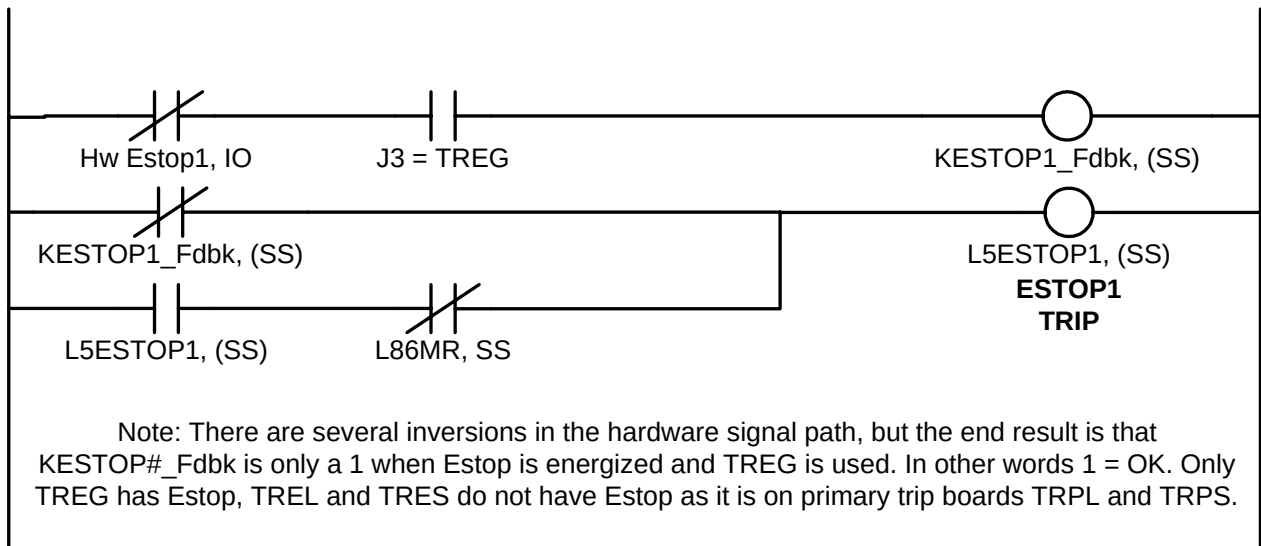
The resulting contact trip signals are combined into a single contact trip summary, L5Cont\_Trip.



*Contact Input Trip Signal Concentration*

### **Estop**

PPRO monitors the Estop trip signal that is present on the TREG board and uses it to cross trip the main control in the event Estop is invoked. It is also used within the pack logic as part of the trip relay output command. The relays are not required to close if the ESTOP signal is present. The main control counterpart is also present. If the main control votes to trip, it can also cross-trip the corresponding PPRO.

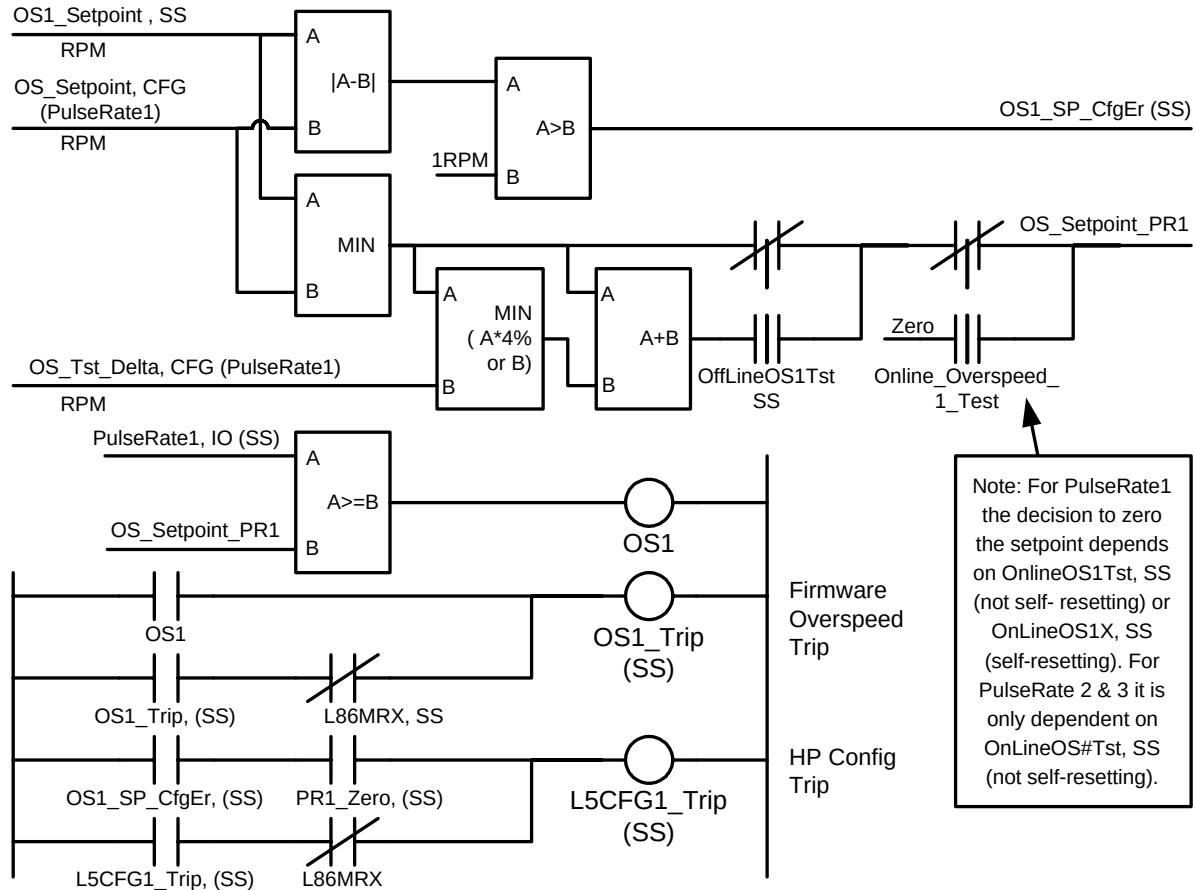


Note: There are several inversions in the hardware signal path, but the end result is that KESTOP#\_Fdbk is only a 1 when Estop is energized and TREG is used. In other words 1 = OK. Only TREG has Estop, TREL and TRES do not have Estop as it is on primary trip boards TRPL and TRPS.

*Contact Input Estop*

## Overspeed Trip

PPRO provides three speed input signals feeding firmware and hardware overspeed protection. While PPRO documentation follows the established standard of calling these three inputs HP, IP, and LP the three inputs are free to be applied as needed in a system design.



*Firmware Overspeed Trip, HP Shaft*

Firmware Overspeed Trip functions include:

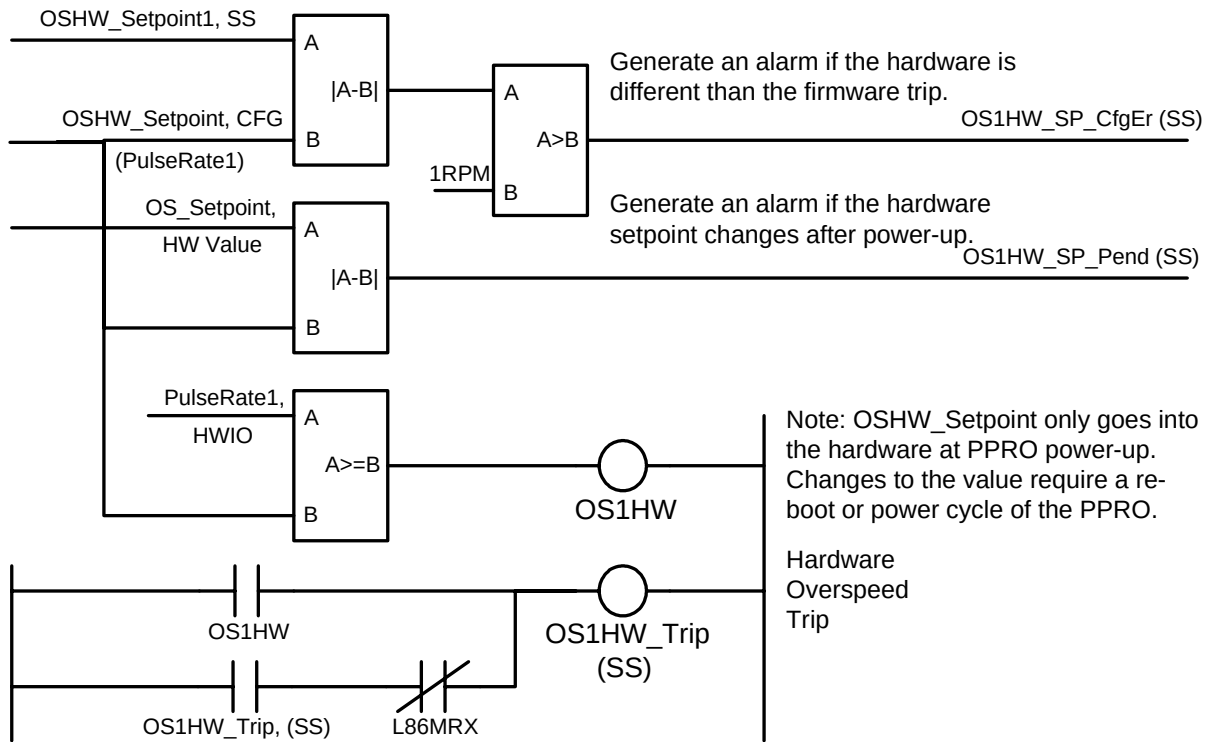
- Fault on overspeed threshold match failure between config and signal space values when speed is zero.
- Pick the lower threshold from config or signal space.
- Provide a mechanism to zero the threshold for online overspeed test.
- Provide a mechanism to modify the threshold for offline overspeed test, bounded to limit increases to the threshold to 104%.

**Note** If you want to reduce the threshold to conduct tests, a negative OS\_Tst\_Delta value is needed.



- Compare the threshold to the calculated speed and latch overspeed.

The diagram on the preceding page shows the overspeed names used for the first of three pulse rate inputs. The same figure is repeated for PulseRate2 and 3. For all variables where the number 1 appears, simply substitute a 2 or 3 for the 1 to get the signal name.



*Hardware Overspeed Trip, HP Shaft*

Hardware Overspeed Trip functions include:

- Load the independent hardware overspeed set point only when the PPRO pack re-boots or has power cycled
- Generate an alarm when the hardware config set point is >1 Hz different from the value passed through signal space from the application configuration
- Generate an alarm and signal space Boolean when the set point in config fails to match the value stored in the hardware
- Implement speed calculation and the trip logic entirely inside programmable logic
- Overspeed response time will be < 20 ms at trip speed

**Note** There is no separate enable /disable signal for this Overspeed protection. The disable signal is created by setting a high overspeed point value. The calculated speed will never reach the value needed to trigger OS1HW.

The actual hardware implementation depends on two configuration items:

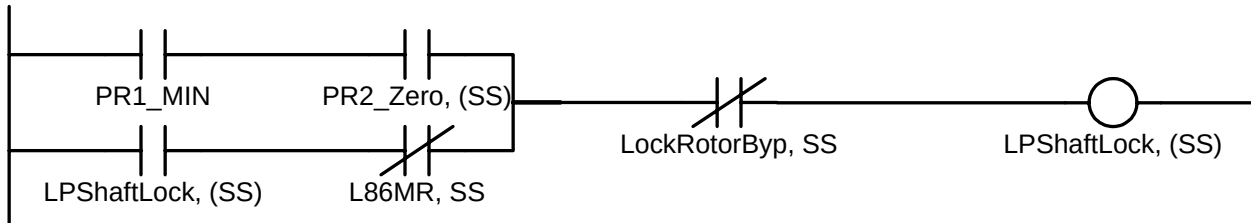
- HWOS\_Setpoint specifies the overspeed trip level in RPM.
- PRScale determines the number of speed sensor pulses per revolution used to convert pulse rate into RPM for both hardware and firmware overspeed value.

**Note** If a hardware overspeed trip occurs followed by the abrupt removal of the speed signal power, it can be necessary to cycle PPRO to reset the trip condition.

The hardware implementation requires two adjacent revolutions exceeding the HWOS\_Setpoint in order to trip the system. When a trip is present, the setting of HWOS\_Setpoint is reduced by a small amount in the hardware to provide a clean trip signal. Due to this reduction, speed must be reduced well below the overspeed threshold before a reset may take place. Because there are set limits to the time integration used in the hardware detector, the minimum RPM setting for the HWOS\_Setpoint is approximately four RPM.

### LP Shaft Locked Detection

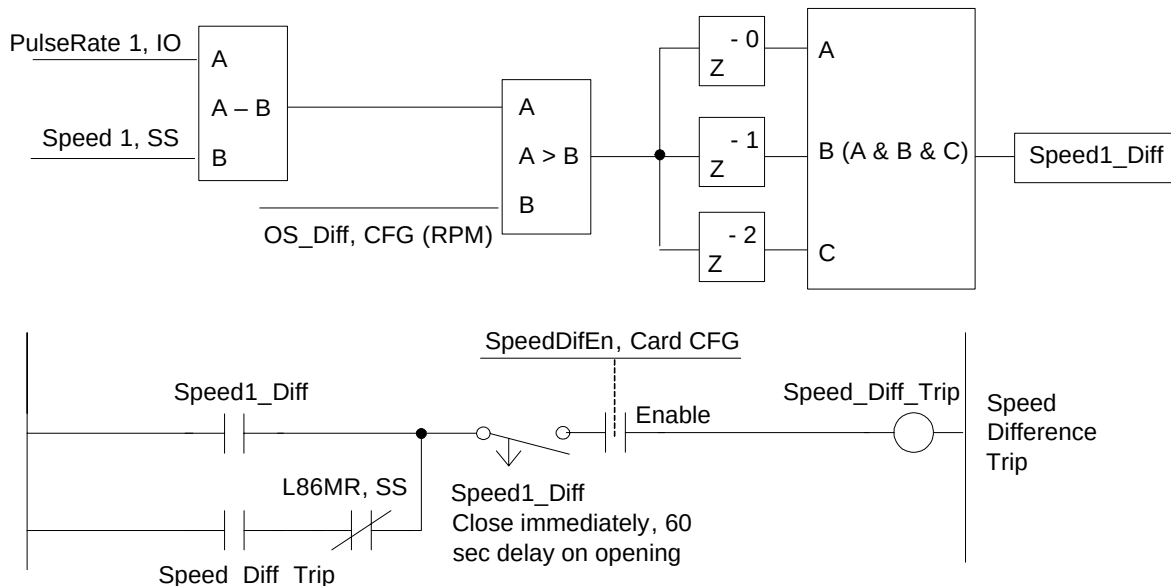
There is another protection function in addition to the overspeed protection shown on the preceding page. It generates a signal in the event the first pulse rate signal is above minimum speed, and the second pulse rate signal is still at zero.



LP Shaft Locked Detection

### Speed Difference Detection

There should never be a reason why the speed calculated by PPRO is significantly different from the speed calculated by the main control. Speed difference detection looks at the difference in magnitude between pulse rate 1 from both PPRO and the main control. If the difference is greater than the set threshold for three successive samples, a SpeedDifTrip is latched. If the main control recovers for 60 seconds, the trip is removed. This allows the main control to recover with subsequent re-arming of the backup protection.



Speed Difference Detection

Additional logic is added whenever dual control is used. When configured for dual control, there are separate speed inputs from the two controllers that come into PPRO. This trip logic will act if both controllers have a speed error, but will continue to run if one controller has a valid speed signal.

## Maximum Speed Hold

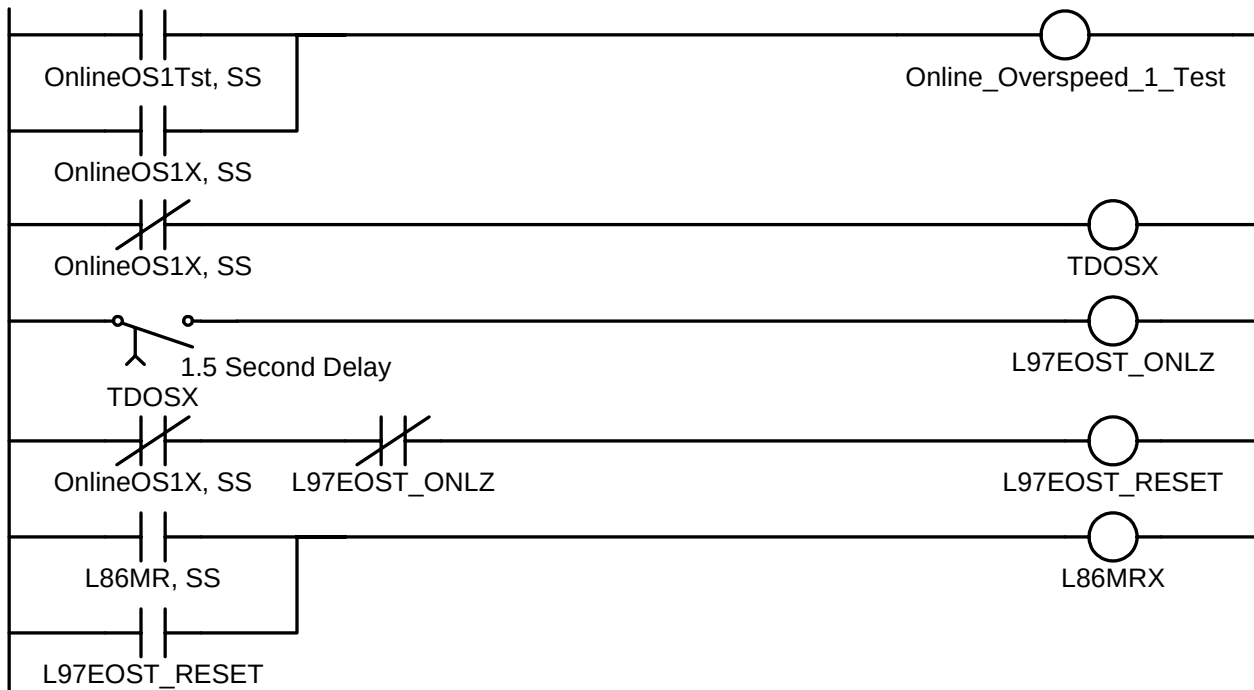
PPRO provides a maximum speed hold function that resets when:

- Using the command PR\_Max\_RST (from signal space)
- PR1\_Zero changes to false (you first start turning)

Output values are PR1\_Max, PR2\_Max, and PR3\_Max. These signals are used to determine the maximum speed obtained while running or after stopping a turbine.

## Overspeed Test Logic, Steam Turbine

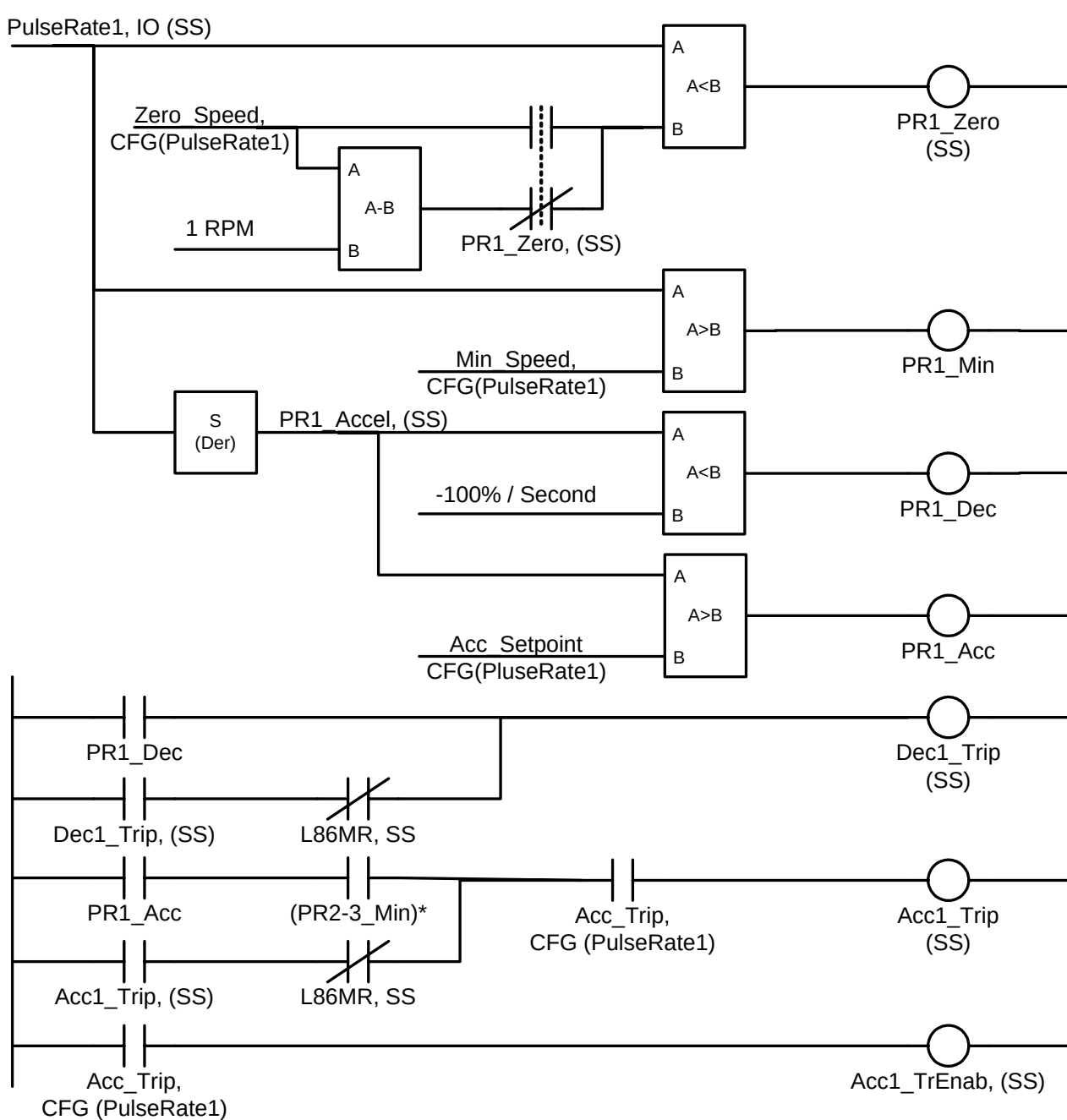
The signal OnLineOS1Tst is used for PulseRate1, OnLineOS2Tst is used for PulseRate2, and OnLineOS3Tst is used for PulseRate3. In the following figure, there is another signal, Online OS1X, which initiates an online overspeed test for PulseRate1. This signal also creates a 1.5 second reset pulse when removed.



Online Overspeed Test Logic

## Speed State Boolean Values

PPRO has detection for zero speed from a set point with 1 RPM hysteresis. The pack calculates a minimum speed signal from a set point. The rate of change of speed from a set point is calculated resulting in a selectable acceleration trip. A deceleration trip is then determined from a fixed 100% / Second rate.



### HP Shaft Accel Decel and Zero

The name of the first pulse rate input is shown in the above figure. The same figure is repeated for PulseRate2 and 3. Simply replace the 1 with a 2 or 3 to get the signal name.

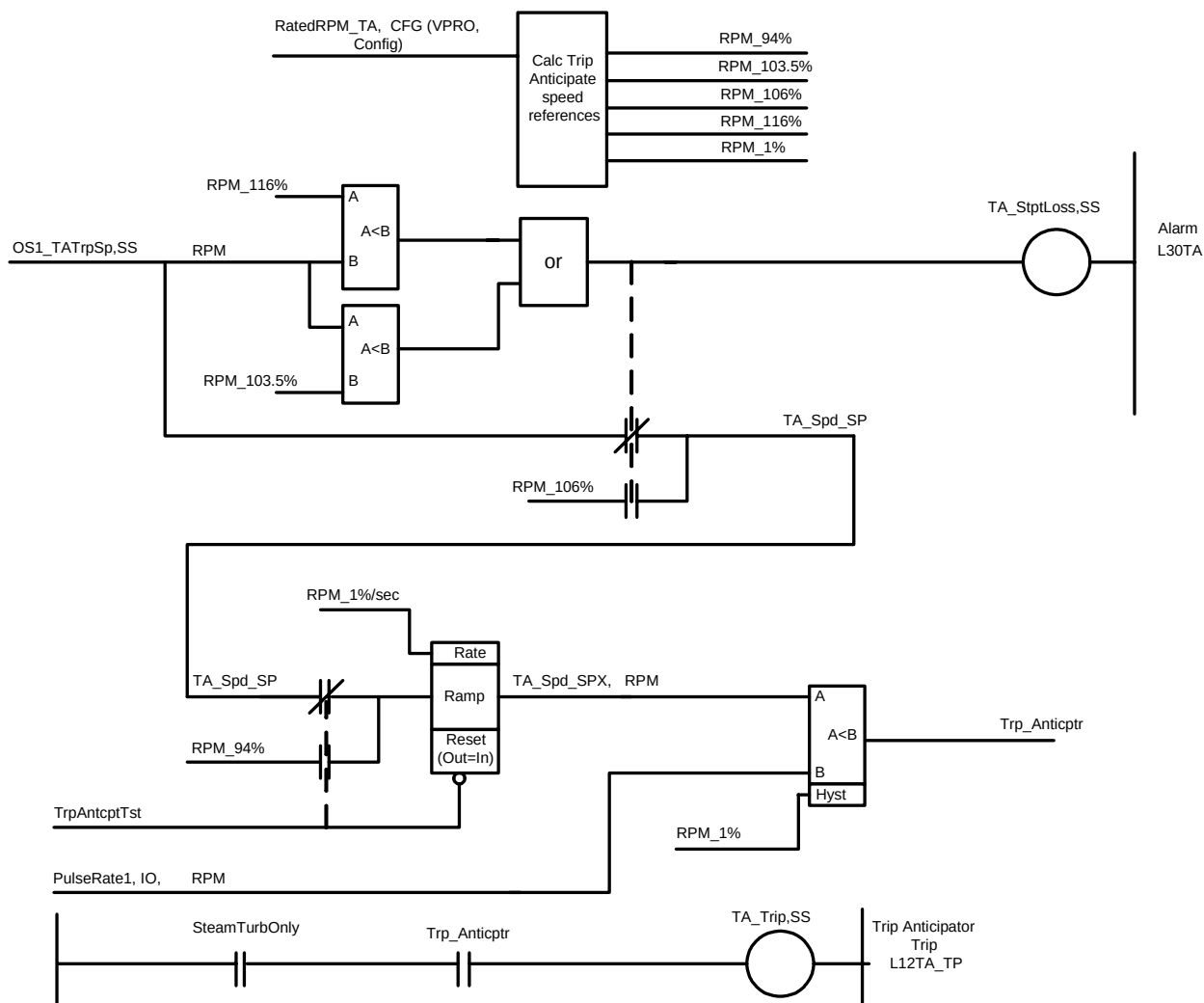
**Note** The contact, PR2-3\_Min, in the Acc1\_Trip is only present for PR2 (PR2\_Min) and PR3 (PR3\_Min). It is not used for PR1.

## Trip Anticipate Function

Steam turbine applications provide a speed trip that uses a live set point from signal space. This overspeed trip is vigorously changed as a function of turbine load. This function does the following:

- Input set point is OS1\_TATrpSp from signal space. Input rated RPM is specified by RatedRPM\_TA as part of PPRO configuration. Function test request input is TrpAntcptTst from signal space.
- If (OS1\_TATrpSP is < 103.5% OR > 116% of RatedRPM\_TA) then TA\_Spd\_Sp (the local set point value) = 106% of RatedRPM\_TA and TA\_StptLoss (Signal space) is true and alarm L30TA is declared. Otherwise, TA\_Spd\_Sp = OS1\_TATrpSP.
- If TrpAntcptTst is true, decrease the current value of TA\_Spd\_Sp by 1RPM / second. Set the minimum value of RatedRPM\_TA to 94%. If TrpAntcptTst is false, the value of TA\_Spd\_Sp from above is immediately used.
- If PulseRate1 (Speed input 1 from the pulse rate input) > TA\_Spd\_Sp the internal value Trp\_Anticptr is set properly.
- If PPRO is configured for steam turbine application (internal value SteamTurbOnly), then TA\_Trip (signal space) equals the value of Trp\_Anticptr.

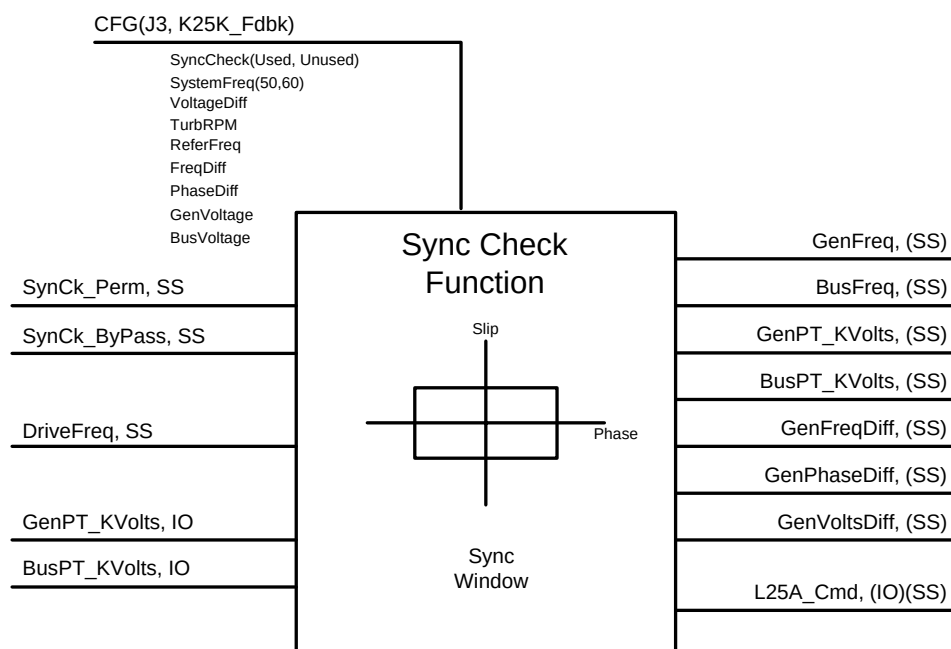
The figure on the following page illustrates the function described above.



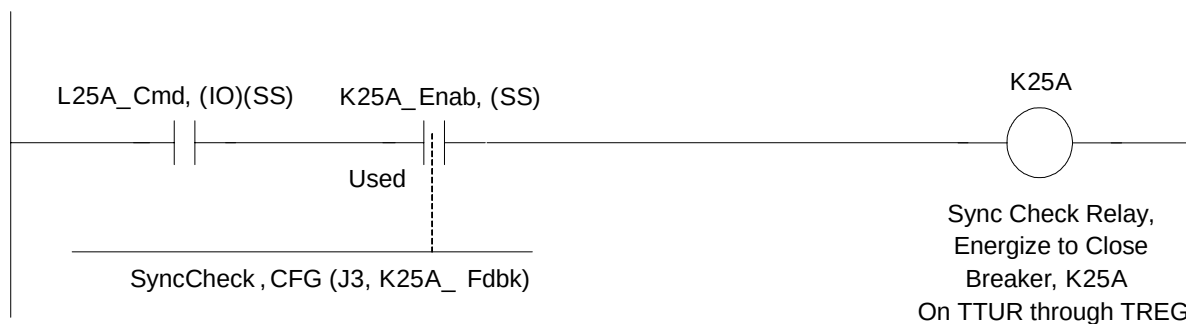
Trip Anticipation Function

## Sync Check and K25A Sync Relay Command

PPRO provides two PT inputs and performs a backup synchronizing check. SPRO does not use fanned PT inputs; there are three direct PT paths.



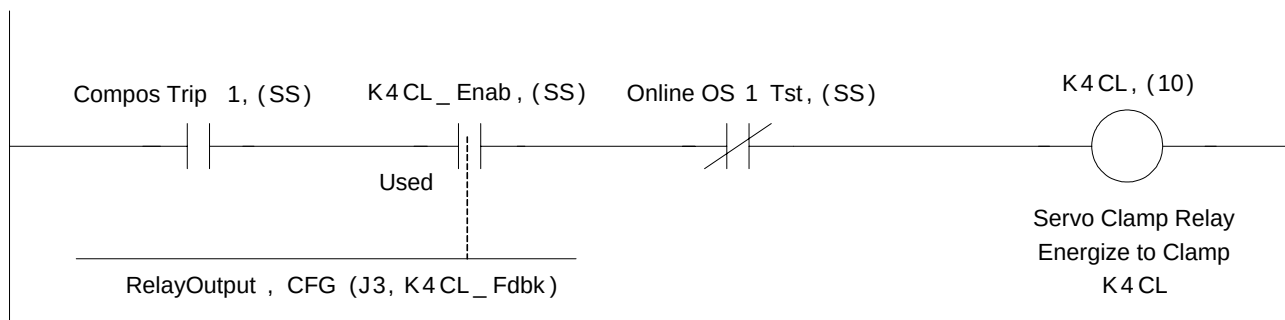
PPRO provides a command to monitor feedback for the K25A sync relay and K25A coil. The feedback is named K25A\_Fdbk, (SS).



*Sync Check and K25A Sync Relay Command*

## Servo Suicide Relay Command

PPRO provides a command to a servo suicide relay, and provides coil-monitoring feedback named K4CL\_Fdbk, (SS). This signal is typically used in a simplex control of a gas turbine system where it is highly desirable for the PPRO emergency protection to have a hardware path to close the fuel valves.

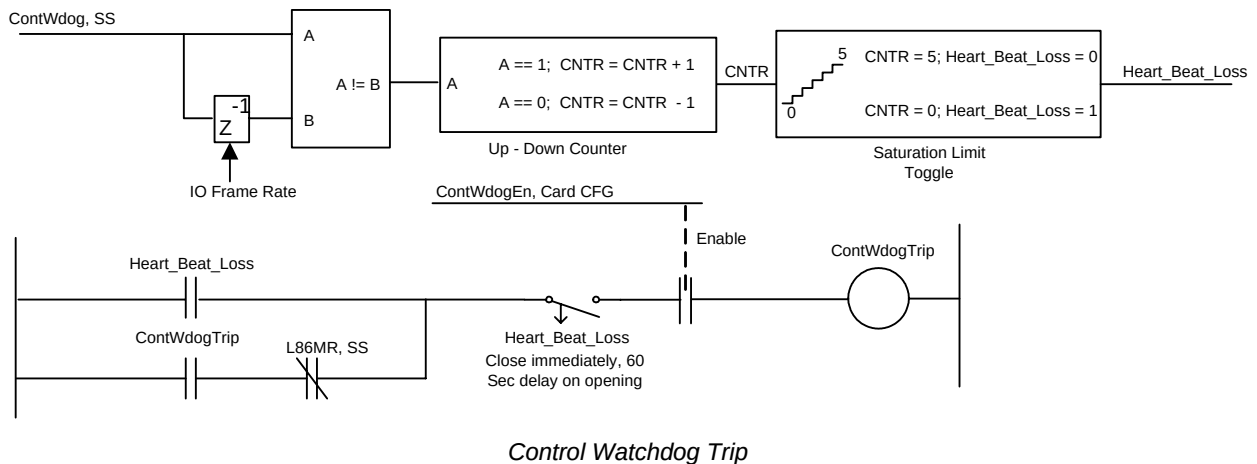


## Solenoid Voltage / Power Sense

PPRO provides three comparator voltage inputs used to monitor solenoid power or solenoid voltage depending on the trip card that is connected. SOL1\_Vfdbk (SS), SOL2\_Vfdbk (SS), and SOL3\_Vfdbk (SS) are generated from the input signals.

## Main Control Watchdog

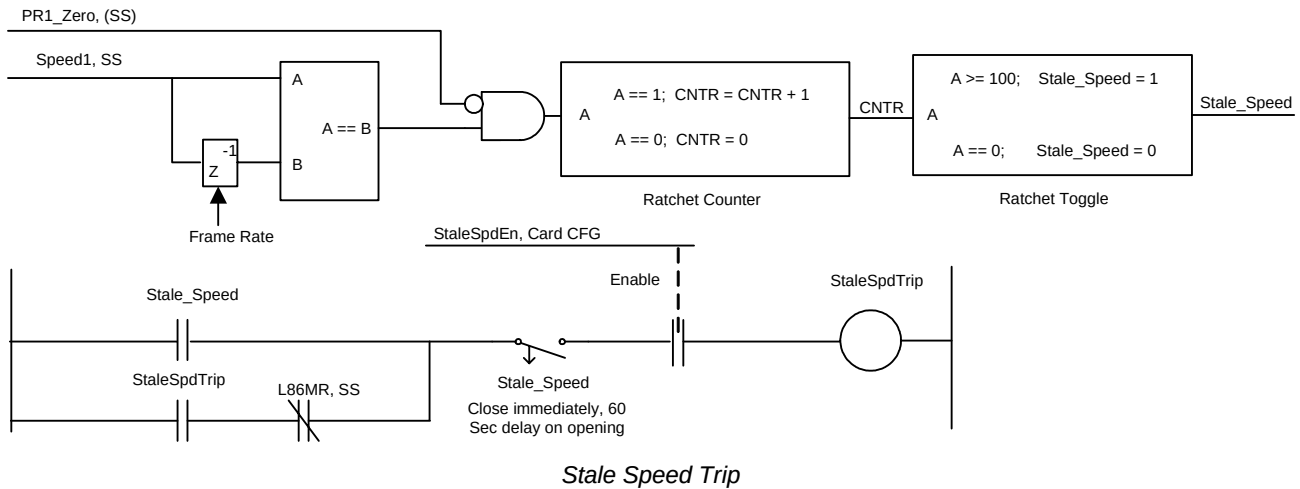
A standard control watchdog function is provided by PPRO. In this function, a value is passed from the main control to the PPRO each data frame. If the pack stops seeing the value from the main control, a counter is incremented and, after five data frames leads to a trip. If the main control recovers for 60 seconds, the trip is removed, allowing for the recovery of the main control with subsequent re-arming of the backup protection. The recovery function is provided for typical activities such as cycling power on a controller to perform maintenance. While the controller is offline, the PPRO associated with that controller will vote to trip. When the controller returns to operation, the pack will remove the vote to trip. The watchdog offers monitoring of two main controls in the event both Ethernet ports are connected. When configured for two controls, having one control active is sufficient to prevent a trip.



Control Watchdog Trip

## Stale Speed Detection

The PPRO provides an additional main control watchdog function that is based on a live speed signal. The protection works as follows: If PPRO PulseRate1 is determined to be zero speed the protection is turned off. If above zero speed, the pack looks at the value of Speed1 from the main control. If the most recent Speed1 value exactly matches the Speed1 value from the last data frame then a counter is incremented. If the counter reaches a threshold then a stale speed trip is declared and latched. If speeds are different the counter is cleared. This protection is based on the knowledge that a live speed signal always *dithers* or moves some small amount. The only way you will see consecutive signals with the same value for a period of time is if the speed calculation or worse is not functioning in the main control. If the main control recovers for 60 seconds, the trip is removed allowing for the recovery of the main control with subsequent re-arming of the backup protection. The protection offers monitoring of two main controls in the event both Ethernet ports are connected. When configured for two controls, having one control satisfy the test is sufficient to prevent a trip.

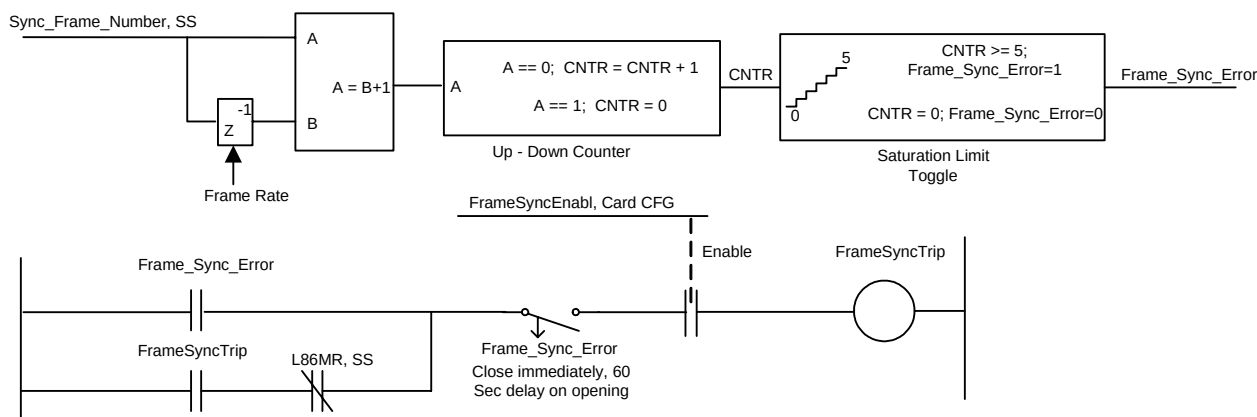




## Main Control Ethernet Monitor

The main control provides time synchronization across the distributed control elements. The time synchronization is tied tightly into the time at which traffic occurs on a given controllers IONet. The PPRO provides monitoring of this service to ensure it is working correctly. Gross errors in time synchronization are detected by PPRO through a number of different means and if problems persist the PPRO will vote to trip. Once the trip is latched, if the problem goes away for 60 seconds the trip shall be reset (this assumes the control recovers from the problem and is back on line). The monitor will offer monitoring of two main controls in the event both Ethernet ports are connected. When configured for two controls, having one control sequencing correctly is sufficient to prevent a trip.

In the following diagram, the detection has been simplified to show monitoring of an Ethernet frame number as the means for determining a problem is present.

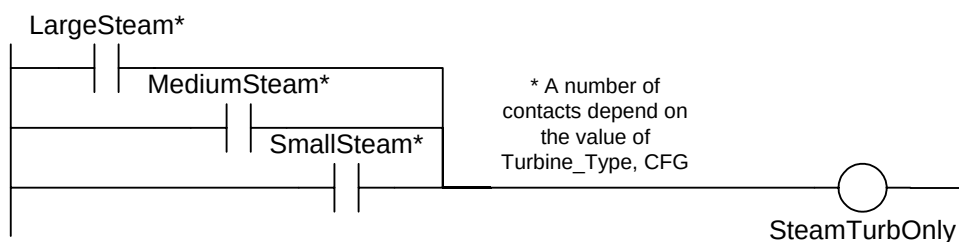


Sync Frame Count Monitor

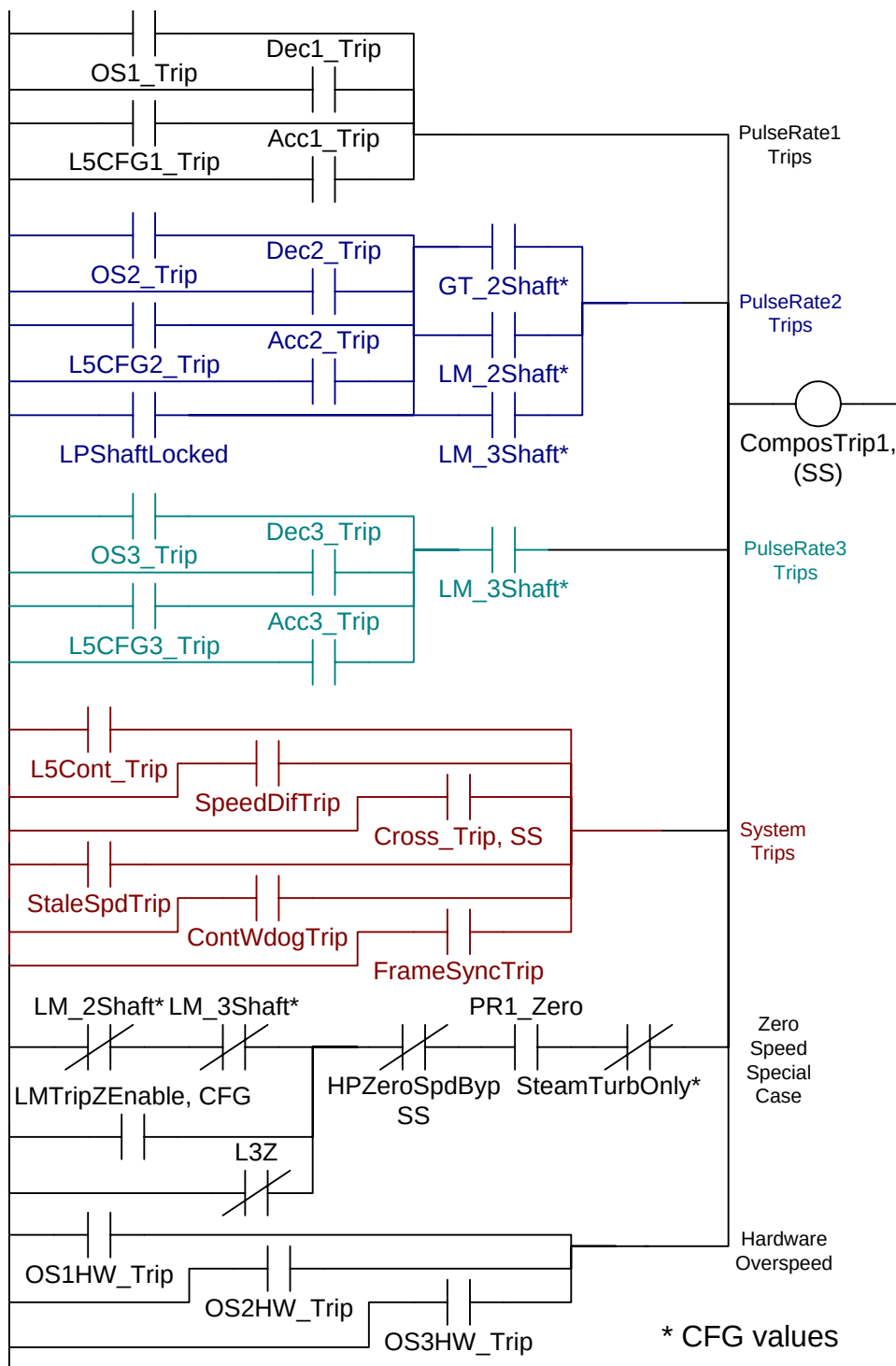
## Trip Signal Logic

The different trip signals are combined into a composite signal that is used in the relay output logic. The following figure shows how the signals are combined. This function is partitioned between firmware and programmable logic. The path to trip through hardware overspeed is done completely in hardware so that a firmware malfunction cannot defeat the protection. The same is true of the contact input trip signals when they are configured for direct trip.

There are differences between steam turbine protection and other protection. A composite signal SteamTurbOnly is created for ease of use:



Steam Turbine Trip Signals

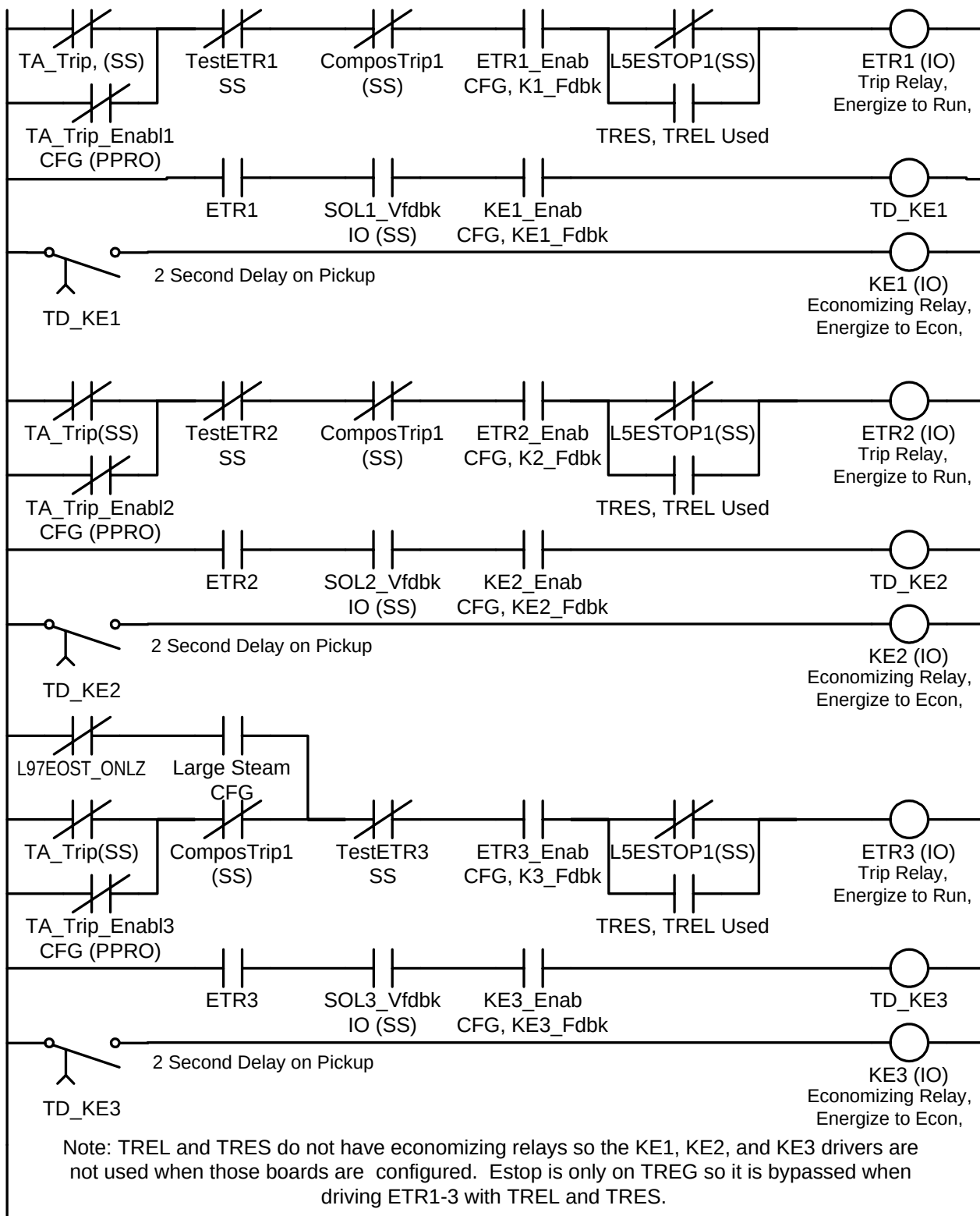


*Trip Combine (All Signals [SS] unless Marked)*

### **Trip and Economizing Relay Outputs**

PPRO provides drivers for three emergency trip relay commands, and provides monitoring for three status feedback signals. Trip is a combination of firmware trip and direct trip implemented in programmable logic. PPRO contains drivers for three economizing relay commands and monitoring for three status feedback signals. Economizing relays are used when it is desirable to introduce some series resistance in a solenoid coil path to reduce current once the solenoid is picked up. Logic for the economizing relay drivers is a time-delayed copy of the emergency trip relays as shown.

**Note** The reset signal applied to this function is not edge triggered. A continuously applied reset can result in output cycling in the presence of an intermittent trip signal. The duration of the reset should only be sufficient to allow the reset to complete and should not be maintained.



*Trip and Economizing Relay Outputs*

## PPRO Watchdog

Hardware in the PPRO monitors operation of the local firmware and provides a watchdog trip function in the event of a firmware malfunction. The operation of this watchdog does not show up in the normal sequencing figures. The I/O pack hardware is designed to be in a fail-safe or trip mode if it is not properly configured and operating. This means that with power off, while starting up, when in a hardware reset, or otherwise not online, the PPRO will vote to trip. If the PPRO watchdog acts, it will reset the hardware thereby generating a vote to trip.

It should also be noted that the processor board used inside PPRO has hardware features that allow the processor to differentiate between a reset caused by the watchdog hardware and a reset caused by cycling of power. This information is available from the PPRO after it re-starts. In the event that a PPRO votes to trip due to a reset, it is then possible to determine if a watchdog reset or a cycling of control power caused the event.

## Specifications

| Item                             | PPRO Specification                                                                                                                                                                             |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Speed Input Quantity             | Three input signals provided                                                                                                                                                                   |
| Speed input Range                | Pulse rate frequency range 2 Hz to 20 kHz                                                                                                                                                      |
| Speed Input Accuracy             | Pulse rate accuracy 0.05% of reading                                                                                                                                                           |
| Speed Input Sensitivity          | 27 mV pk (detects 2 rpm speed)                                                                                                                                                                 |
| Generator and Bus Voltage Inputs | Input voltage range 75 to 130 V rms. Loading less than 3 VA.<br>Frequency accuracy 0.05% over 45 to 66 Hz range.                                                                               |
| Frame Rate                       | 100 Hz maximum                                                                                                                                                                                 |
| <b>Physical</b>                  |                                                                                                                                                                                                |
| Size                             | 8.26 cm High x 4.19 cm Wide x 12.1 cm Deep (3.25 in. x 1.65 in. x 4.78 in.)                                                                                                                    |
| Technology                       | Surface-mount                                                                                                                                                                                  |
| <b>Environment</b>               |                                                                                                                                                                                                |
| Temperature                      | Operating: -30 to 65°C (-22 to 149 °F)                                                                                                                                                         |
| Temperature                      | Shipping & Storage: -40 to 80°C (-40 to 176 °F)                                                                                                                                                |
| Humidity                         | 5 to 95% non-condensing                                                                                                                                                                        |
| Air Quality                      | Pollution Degree 2, free convection at the module                                                                                                                                              |
| <b>Vibration</b>                 |                                                                                                                                                                                                |
| Seismic                          | Universal Building Code (UBC) – Seismic Code section 2312 Zone 4 with operation without trip                                                                                                   |
| Shipping (by road)               | Bellcore GR-63-CORE Issue 1, 1995 0.5 g, 5-100 Hz, 10 min. per octave, 1 sweep/axis x 3 axes, ~ 42 min./axis<br>3 shocks of 15 g, 2 ms impulse each repeated for all axes                      |
| Operating at site                | 1.0 g horizontal. 0.5 g vertical at 15 to 120 Hz<br>IEC 60721-3-2                                                                                                                              |
| <b>Agency Approvals</b>          |                                                                                                                                                                                                |
| Safety Standards                 | UL 508A Safety Standard Industrial Control Equipment<br>CSA 22.2 No. 14 Industrial Control Equipment<br>EN 61010-1 Safety of Electrical Equipment, Industrial Machines (Low Voltage Directive) |
| Printed Wire Board Assemblies    | UL 796 Printed Circuit Boards<br>UL recognized Board manufacturer<br>ANSI IPC guidelines<br>ANSI IPC/EIA guidelines                                                                            |

| Item                                | PPRO Specification                                    |
|-------------------------------------|-------------------------------------------------------|
| Electromagnetic Compatibility (EMC) | EN 61000-4-2 Electrostatic Discharge Susceptibility   |
|                                     | EN 6100 4-3 (ENV 50140) Radiated RF Immunity          |
|                                     | EN 61000-6-2 Generic Immunity Industrial Environment  |
|                                     | EN 61000-4-4 Electrical Fast Transient Susceptibility |
|                                     | EN 61000-4-5 Surge Immunity                           |
|                                     | EN 61000-4-6 Conducted RF Immunity                    |
|                                     | EN 55011 Radiated and Conducted RF Emissions          |
|                                     | ANSI/IEEE C37.90.1 Surge                              |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the analog feedback currents
- A comparison between the commanded state of each relay drive and the feedback from the commanded output circuit
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set

Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go health.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter    | Description                                                 | Choices                                                                                                           |
|--------------|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|
| TurbineType  | Turbine Type and Trip Solenoid Configuration                | Unused, GT_1Shaft, LM_3Shaft, MediumSteam, SmallSteam, GT_2Shaft, Stag_GT_1Sh, Stag_GT_2Sh, LargeSteam, LM_2Shaft |
| LMTripZEnabl | On LM machine, when no PR on Z,Enable a vote for Trip       | Disable, Enable                                                                                                   |
| TA_Trp_Enab1 | Steam, Enable Trip Anticipate on ETR1                       | Disable, Enable                                                                                                   |
| TA_Trp_Enab2 | Steam, Enable Trip Anticipate on ETR2                       | Disable, Enable                                                                                                   |
| TA_Trp_Enab3 | Steam, Enable Trip Anticipate on ETR3                       | Disable, Enable                                                                                                   |
| ContWdogEn   | Enable trip on loss of Control Outputs to PPRO              | Disable, Enable                                                                                                   |
| SpeedDifEn   | Enable Trip on Speed Difference between Controller and PPRO | Disable, Enable                                                                                                   |
| StaleSpdEn   | Enable Trip on Speed from Controller Freezing               | Disable, Enable                                                                                                   |
| DiagSolPwrA  | When using TREL/TRES,Sol Power,Bus A,Diagnostic Enable      | Disable, Enable                                                                                                   |
| DiagSolPwrB  | When using TREL/TRES,Sol Power,Bus B,Diagnostic Enable      | Disable, Enable                                                                                                   |

| Parameter    | Description                                                        | Choices            |
|--------------|--------------------------------------------------------------------|--------------------|
| DiagSolPwrC  | When using TREL/TRES,Sol Power,Bus C,Diagnostic Enable             | Disable, Enable    |
| FrameMonEn   | Enable trip when IO-Net frame synchronization is lost              | Disable, Enable    |
| Redundancy   | Redundancy mode of the module                                      | Simplex, DUAL, TMR |
| RotateLeds   | Rotate the Status LEDs if all status are OK                        | Disable, Enable    |
| LedDiags     | Generate diag alarm when LED status lit                            | Disable, Enable    |
| RatedRPM_TA  | Rated RPM, used for Trip Anticipater and for Speed Diff Protection |                    |
| AccelCalType | Select Acceleration Calculation Time (msec)                        |                    |
| OS_Diff      | Absolute Speed Difference in Percent For Trip Threshold            |                    |

*Terminal Board\_SPRO (MainVer\_1)*

| Variable     | Description    | Direction   | Type |
|--------------|----------------|-------------|------|
| PulseRate1   | HP speed       | AnalogInput | REAL |
| PulseRate2   | LP speed       | AnalogInput | REAL |
| PulseRate3   | IP speed       | AnalogInput | REAL |
| BusPT_KVolts | Kilo-Volts RMS | AnalogInput | REAL |
| GenPT_KVolts | Kilo-Volts RMS | AnalogInput | REAL |

*Terminal Board\_TREA (MainVer\_1)*

| Variable            | Description                                                | Direction   | Type |
|---------------------|------------------------------------------------------------|-------------|------|
| PulseRate1          | HP speed                                                   | AnalogInput | REAL |
| PulseRate2          | LP speed                                                   | AnalogInput | REAL |
| PulseRate3          | IP speed                                                   | AnalogInput | REAL |
| Fan_Spd_Fbk         | Fanned Speed Signal Feedback :- Fanned = Jumpers Closed    | Input       | BOOL |
| NotUsedA1 and A2    | Kilo-Volts RMS                                             | AnalogInput | REAL |
| KESTOP1_Fdbk        | ESTOP1,inverse sense,True = Run                            | Input       | BOOL |
| NotUsedA3 thru A9   | Contact Input 1 through 7                                  | Input       | BOOL |
| K1_Fdbk             | L4ETR1_FB, Trip Relay 1 Feedback                           | Input       | BOOL |
| K2_Fdbk             | L4ETR2_FB, Trip Relay 2 Feedback                           | Input       | BOOL |
| NotUsedA10          | L4ETR3_FB, Trip Relay 1 Feedback                           | Input       | BOOL |
| NotUsedA11 thru A13 | When TREG, Current Economizing Relay for Trip Solenoid 1-3 | Input       | BOOL |
| NotUsedA14          | Drive Control Valve Servos Closed.                         | Input       | BOOL |
| NotUsedA15          | Synch Check Relay                                          | Input       | BOOL |
| VSen1               | Voltage Sensor 1 Feedback                                  | Input       | BOOL |
| VSen2               | Voltage Sensor 2 Feedback                                  | Input       | BOOL |
| VSen3               | Voltage Sensor 3 - Power Monitor Feedback                  | Input       | BOOL |

*Terminal Board\_TREG (AuxVer\_1)*

| Variable        | Description                                   | Direction | Type |
|-----------------|-----------------------------------------------|-----------|------|
| KESTOP1_Fdbk    | ESTOP1, inverse sense,K4 relay,True = Run     | Input     | BOOL |
| Contact1 thru 7 | Contact Input 1 through 7                     | Input     | BOOL |
| K1_Fdbk         | L4ETR1_FB, Trip Relay 1 Feedback              | Input     | BOOL |
| K2_Fdbk         | L4ETR2_FB, Trip Relay 2 Feedback              | Input     | BOOL |
| K3_Fdbk         | L4ETR3_FB, Trip Relay 3 Feedback              | Input     | BOOL |
| KE1_Fdbk        | Current Economizing Relay for Trip Solenoid 1 | Input     | BOOL |
| KE2_Fdbk        | Current Economizing Relay for Trip Solenoid 2 | Input     | BOOL |
| KE3_Fdbk        | Current Economizing Relay for Trip Solenoid 3 | Input     | BOOL |
| K4CL_Fdbk       | Drive Control Valve Servos Closed.            | Input     | BOOL |
| K25A_Fdbk       | Synch Check Relay                             | Input     | BOOL |

*Terminal Board\_TREL (AuxVer\_1)*

| Variable        | Description                                              | Direction | Type |
|-----------------|----------------------------------------------------------|-----------|------|
| NotUsed1        | Placeholder for Estop, not used on TREL                  | Input     | BOOL |
| Contact1 thru 7 | Contact Input 1 through 7                                | Input     | BOOL |
| K1_Fdbk         | L4ETR1_FB, Trip Relay 1 Feedback                         | Input     | BOOL |
| K2_Fdbk         | L4ETR2_FB, Trip Relay 2 Feedback                         | Input     | BOOL |
| K3_Fdbk         | L4ETR3_FB, Trip Relay 1 Feedback                         | Input     | BOOL |
| NotUsed2        | When TREG, Current Economizing Relay for Trip Solenoid 1 | Input     | BOOL |
| NotUsed3        | When TREG, Current Economizing Relay for Trip Solenoid 2 | Input     | BOOL |
| NotUsed4        | When TREG, Current Economizing Relay for Trip Solenoid 3 | Input     | BOOL |
| K4CL_Fdbk       | Drive Control Valve Servos Closed                        | Input     | BOOL |
| K25A_Fdbk       | Synch Check Relay                                        | Input     | BOOL |

*Terminal Board\_TRES (AuxVer\_1)*

| Variable        | Description                                              | Direction | Type |
|-----------------|----------------------------------------------------------|-----------|------|
| NotUsed1        | Placeholder for Estop, not used on TREL                  | Input     | BOOL |
| Contact1 thru 7 | Contact Input 1 through 7                                | Input     | BOOL |
| K1_Fdbk         | L4ETR1_FB, Trip Relay 1 Feedback                         | Input     | BOOL |
| K2_Fdbk         | L4ETR2_FB, Trip Relay 2 Feedback                         | Input     | BOOL |
| K3_Fdbk         | L4ETR3_FB, Trip Relay 1 Feedback                         | Input     | BOOL |
| NotUsed2        | When TREG, Current Economizing Relay for Trip Solenoid 1 | Input     | BOOL |
| NotUsed3        | When TREG, Current Economizing Relay for Trip Solenoid 2 | Input     | BOOL |
| NotUsed4        | When TREG, Current Economizing Relay for Trip Solenoid 3 | Input     | BOOL |
| K4CL_Fdbk       | Drive Control Valve Servos Closed                        | Input     | BOOL |
| K25A_Fdbk       | Synch Check Relay                                        | Input     | BOOL |

*Modules\_PPPO\_Variables*

| Board Points (Signals)    | Description – Point Edit (Enter Signal Connection) | Direction   | Type |
|---------------------------|----------------------------------------------------|-------------|------|
| L3DIAG_PPPO_R,_S, and _T  | I/O Diagnostic Indication                          | Input       | BOOL |
| LINK_OK_PPPO_R,_S, and _T | I/O Link Okay Indication                           | Input       | BOOL |
| ATTN_PPPO_R,_S, and _T    | I/O Attention Indication                           | Input       | BOOL |
| PS18V_PPPO_R,_S, and _T   | I/O 18V Power Supply Indication                    | Input       | BOOL |
| PS28V_PPPO_R,_S, and _T   | I/O 28V Power Supply Indication                    | Input       | BOOL |
| IOPackTmpR,_S, and _T     | IO Pack Temperature (deg F)                        | AnalogInput | REAL |
| K1_FdbkNV_R,_S, and _T    | Non Voted L4ETR1_FB, Trip Relay 1 Feedback         | Input       | BOOL |
| K2_FdbkNV_R,_S, and _T    | Non Voted L4ETR2_FB, Trip Relay 2 Feedback         | Input       | BOOL |
| K3_FdbkNV_R,_S, and _T    | Non Voted L4ETR3_FB, Trip Relay 3 Feedback         | Input       | BOOL |
| K1FLT                     | K1 Shorted Contact Fault                           | Input       | BOOL |
| K2FLT                     | K2 Shorted Contact Fault                           | Input       | BOOL |
| PR1_Zero                  | L14HP_ZE                                           | Input       | BOOL |
| PR2_Zero                  | L14HP_ZE                                           | Input       | BOOL |
| PR3_Zero                  | L14HP_ZE                                           | Input       | BOOL |
| OS1_Trip                  | L12HP_TP                                           | Input       | BOOL |
| OS2_Trip                  | L12HP_TP                                           | Input       | BOOL |
| OS3_Trip                  | L12HP_TP                                           | Input       | BOOL |
| Dec1_Trip                 | L12HP_DEC                                          | Input       | BOOL |
| Dec2_Trip                 | L12HP_DEC                                          | Input       | BOOL |
| Dec3_Trip                 | L12HP_DEC                                          | Input       | BOOL |
| Acc1_Trip                 | L12HP_ACC                                          | Input       | BOOL |

| Board Points (Signals) | Description – Point Edit (Enter Signal Connection)    | Direction | Type |
|------------------------|-------------------------------------------------------|-----------|------|
| Acc2_Trip              | L12HP_ACC                                             | Input     | BOOL |
| Acc3_Trip              | L12HP_ACC                                             | Input     | BOOL |
| TA_Trip                | Trip Anticipate Trip,L12TA_TP                         | Input     | BOOL |
| TA_StptLoss            | L30TA                                                 | Input     | BOOL |
| OS1HW_Trip             | L12HP_TP                                              | Input     | BOOL |
| OS2HW_Trip             | L12HP_TP                                              | Input     | BOOL |
| OS3HW_Trip             | L12HP_TP                                              | Input     | BOOL |
| SOL1_Vfdbk             | When TREG,Trip Solenoid 1 Voltage                     | Input     | BOOL |
| SOL2_Vfdbk             | When TREG,Trip Solenoid 2 Voltage                     | Input     | BOOL |
| SOL3_Vfdbk             | When TREG,Trip Solenoid 3 Voltage                     | Input     | BOOL |
| L25A_Cmd               | L25A Breaker Close Pulse                              | Input     | BOOL |
| Cont1_TrEnab thru 7    | Config -- Contact 1 Trip Enabled thru 7               | Input     | BOOL |
| Acc1_TrEnab thru 3     | Config -- Accel 1 Trip Enabled thru 3                 | Input     | BOOL |
| GT_1Shaft              | Config -- Gas Turb,1 Shaft Enabled                    | Input     | BOOL |
| GT_2Shaft              | Config -- Gas Turb,2 Shaft Enabled                    | Input     | BOOL |
| LM_2Shaft              | Config -- LM Turb,2 Shaft Enabled                     | Input     | BOOL |
| LM_3Shaft              | Config -- LM Turb,3 Shaft Enabled                     | Input     | BOOL |
| LargeSteam             | Config -- Large Steam 1, Enabled                      | Input     | BOOL |
| MediumSteam            | Config -- Medium Steam Enabled                        | Input     | BOOL |
| SmallSteam             | Config -- Small Steam Enabled                         | Input     | BOOL |
| Stag_GT_1Sh            | Config -- Stag 1 Shaft, Enabled                       | Input     | BOOL |
| Stag_GT_2Sh            | Config -- Stag 2 Shaft, Enabled                       | Input     | BOOL |
| ETR1_Enab              | Config -- ETR1 Relay Enabled                          | Input     | BOOL |
| ETR2_Enab              | Config -- ETR2 Relay Enabled                          | Input     | BOOL |
| ETR3_Enab              | Config -- ETR3 Relay Enabled                          | Input     | BOOL |
| OS1HW_SP_Pend          | Hardware HP overspeed setpoint changed after power up | Input     | BOOL |
| OS2HW_SP_Pend          | Hardware LP overspeed setpoint changed after power up | Input     | BOOL |
| OS3HW_SP_Pend          | Hardware IP overspeed setpoint changed after power up | Input     | BOOL |
| KE1_Enab               | Config -- Economizing Relay 1 Enabled                 | Input     | BOOL |
| KE2_Enab               | Config -- Economizing Relay 2 Enabled                 | Input     | BOOL |
| KE3_Enab               | Config -- Economizing Relay 3 Enabled                 | Input     | BOOL |
| OS1HW_SP_CfgErr        | Hardware HP Overspd Setpoint Config Mismatch Error    | Input     | BOOL |
| OS2HW_SP_CfgErr        | Hardware LP Overspd Setpoint Config Mismatch Error    | Input     | BOOL |
| OS3HW_SP_CfgErr        | Hardware IP Overspd Setpoint Config Mismatch Error    | Input     | BOOL |
| K4CL_Enab              | Config -- Servo Clamp Relay Enabled                   | Input     | BOOL |
| K25A_Enab              | Config -- Synch Check Relay Enabled                   | Input     | BOOL |
| L5CFG1_Trip            | HP Config Trip                                        | Input     | BOOL |
| L5CFG2_Trip            | LP Config Trip                                        | Input     | BOOL |
| L5CFG3_Trip            | IP Config Trip                                        | Input     | BOOL |
| OS1_SP_CfgEr           | HP Overspd Setpoint Config Mismatch Error             | Input     | BOOL |
| OS2_SP_CfgEr           | LP Overspd Setpoint Config Mismatch Error             | Input     | BOOL |
| OS3_SP_CfgEr           | IP Overspd Setpoint Config Mismatch Error             | Input     | BOOL |



| Board Points (Signals) | Description – Point Edit (Enter Signal Connection)      | Direction    | Type |
|------------------------|---------------------------------------------------------|--------------|------|
| ComposTrip1            | Composite Trip 1                                        | Input        | BOOL |
| ComposTrip2            | Composite Trip 2                                        | Input        | BOOL |
| ComposTrip3            | Composite Trip 3                                        | Input        | BOOL |
| L5ESTOP1               | ESTOP1 Trip                                             | Input        | BOOL |
| L5Cont1_Trip thru 7    | Contact 1 Trip 7                                        | Input        | BOOL |
| LPShaftLock            | LP Shaft Locked                                         | Input        | BOOL |
| Inhbt1_Fdbk thru 7     | Trip Inhibit Signal Feedback for Contact 1 thru 7       | Input        | BOOL |
| L3SS_Comm              | Communication Fault                                     | Input        | BOOL |
| Trip1_EnCon thru 7     | Contact 1 Trip Enabled thru 7 -- Conditional            | Input        | BOOL |
| BusFreq                | SFL2 hz                                                 | AnalogInput  | REAL |
| GenFreq                | DF2 hz                                                  | AnalogInput  | REAL |
| GenVoltsDiff           | DV_ERR KiloVolts rms - Gen Low is Negative              | AnalogInput  | REAL |
| GenFreqDiff            | SFDIFF2 Slip hz - Gen Slow is Negative                  | AnalogInput  | REAL |
| GenPhaseDiff           | SSDIFF2 Phase degrees - Gen Lag is Negative             | AnalogInput  | REAL |
| PR1_Accel              | HP Accel in RPM/SEC                                     | AnalogInput  | REAL |
| PR2_Accel              | LP Accel in RPM/SEC                                     | AnalogInput  | REAL |
| PR3_Accel              | IP Accel in RPM/SEC                                     | AnalogInput  | REAL |
| PR1_Max                | HP Max Speed since last Zero Speed in RPM               | AnalogInput  | REAL |
| PR2_Max                | LP Max Speed since last Zero Speed in RPM               | AnalogInput  | REAL |
| PR3_Max                | IP Max Speed since last Zero Speed in RPM               | AnalogInput  | REAL |
| SynCk_Perm             | L25A_PERM - Sync Check Permissive                       | Output       | BOOL |
| SynCk_ByPass           | L25A_BYPASS - Sync Check ByPass                         | Output       | BOOL |
| Cross_Trip             | L4Z_XTRP - Control Cross Trip                           | Output       | BOOL |
| OnLineOS1Tst           | L97HP_TST1 - On Line HP Overspeed Test                  | Output       | BOOL |
| OnLineOS2Tst           | L97LP_TST1 - On Line LP Overspeed Test                  | Output       | BOOL |
| OnLineOS3Tst           | L97IP_TST1 - On Line IP Overspeed Test                  | Output       | BOOL |
| OffLineOS1Tst          | L97HP_TST2 - Off Line HP Overspeed Test                 | Output       | BOOL |
| OffLineOS2Tst          | L97LP_TST2 - Off Line LP Overspeed Test                 | Output       | BOOL |
| OffLineOS3Tst          | L97IP_TST2 - Off Line IP Overspeed Test                 | Output       | BOOL |
| TrpAntcptTst           | L97A_TST - Trip Anticipate Test                         | Output       | BOOL |
| LokdRotorByp           | LL97LR_BYP - Locked Rotor Bypass                        | Output       | BOOL |
| HPZeroSpdByp           | L97ZSC_BYP - HP Zero Speed Check Bypass                 | Output       | BOOL |
| PTR1                   | L20PTR1 - Primary Trip Relay CMD, for Diagnostic only   | Output       | BOOL |
| PTR2                   | L20PTR2 - Primary Trip Relay CMD, for Diagnostic only   | Output       | BOOL |
| PTR3                   | L20PTR3 - Primary Trip Relay CMD, for Diagnostic only   | Output       | BOOL |
| PR_Max_Rst             | Max Speed Reset                                         | Output       | BOOL |
| OnLineOS1X             | L43EOST_ONL - On Line HP Overspeed Test,with auto reset | Output       | BOOL |
| TestETR1               | L97ETR1 - ETR1 test, True deenergizes relay             | Output       | BOOL |
| TestETR2               | L97ETR2 - ETR2 test, True deenergizes relay             | Output       | BOOL |
| TestETR3               | L97ETR3 - ETR3 test, True deenergizes relay             | Output       | BOOL |
| Trip1_Inhbt thru 7     | Contact 1 Trip Inhibit through 7                        | Output       | BOOL |
| OS1_Setpoint           | HP Overspeed Setpoint in RPM                            | AnalogOutput | REAL |
| OS2_Setpoint           | LP Overspeed Setpoint in RPM                            | AnalogOutput | REAL |
| OS3_Setpoint           | IP Overspeed Setpoint in RPM                            | AnalogOutput | REAL |

| Board Points (Signals) | Description – Point Edit (Enter Signal Connection)        | Direction    | Type |
|------------------------|-----------------------------------------------------------|--------------|------|
| OS1_TATrpSp            | PR1 Overspeed Trip Setpoint in RPM for Trip Anticipate Fn | AnalogOutput | REAL |
| DriveFreq              | Drive (Gen) Freq (hz), used for non standard drive config | AnalogOutput | REAL |
| Speed1                 | Shaft Speed 1 in RPM                                      | AnalogOutput | REAL |
| OSHW_Setpoint1         | HP Overspeed Setpoint in RPM                              | AnalogOutput | REAL |
| OSHW_Setpoint2         | LP Overspeed Setpoint in RPM                              | AnalogOutput | REAL |
| OSHW_Setpoint3         | IP Overspeed Setpoint in RPM                              | AnalogOutput | REAL |
| ContWdog               | Controller Watchdog Counter                               | Output       | DINT |

## Alarms

### PPRO Specific Alarms

| Alarm ID | Alarm Description                                                                          | Possible Cause                                                                                                                                                                                                                                                                           | Solution                                                                                                                                                                       |
|----------|--------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17       | The wrong type of terminal board was selected in the ToolboxST* application                | Verify the connected board ID and try again                                                                                                                                                                                                                                              |                                                                                                                                                                                |
| 18       | No auxiliary IO card is attached to the JA3 connector. SPRO terminal card only.            | Verify that the auxiliary terminal board is connected and try again                                                                                                                                                                                                                      |                                                                                                                                                                                |
| 30       | The ToolboxST application configuration file is not compatible with the I/O Pack firmware. | Rebuild the Mark VIe and download both firmware and application code to the I/O Pack.                                                                                                                                                                                                    |                                                                                                                                                                                |
| 31       | The ToolboxST IO space definition is not compatible with the I/O Pack firmware.            | Rebuild the Mark VIe and download both firmware and application code to the I/O Pack.                                                                                                                                                                                                    |                                                                                                                                                                                |
| 40       | Contact Excitation Voltage Test Failure                                                    | Voltage for the contact inputs on the trip terminal board is not within published limits.                                                                                                                                                                                                | Check source of contact wetting power applied to trip terminal board.                                                                                                          |
| 69-71    | Trip Relay (ETR) Driver [ ] mismatch requested state                                       | The driver output of I/O pack for Emergency Trip Relay 1 (K1), ETR2 (K2), or ETR3 (K3) does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip terminal board. | Check I/O pack connector seating on terminal board. Check SPRO- trip card cable seating (if not TREA) and cable integrity. Replace cable, trip terminal board, SPRO, I/O pack. |
| 72-74    | Econ Relay Driver %02.0f mismatch requested state                                          | The driver output of I/O pack for Economizing Relay KE1, KE2, or KE3 does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip terminal board.                   | Check I/O pack connector seating on terminal board. Check SPRO- trip card cable seating and cable integrity. Replace cable, trip terminal board, SPRO, I/O pack.               |

| Alarm ID | Alarm Description                                              | Possible Cause                                                                                                                                                                                                                           | Solution                                                                                                                                                                                                                             |
|----------|----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 75       | Servo Clamp Relay Driver mismatch requested state              | The driver output of I/O pack for K4CL does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip terminal board. | Check I/O pack connector seating on terminal board. Check SPRO- trip card cable seating and cable integrity. Replace cable, trip terminal board, SPRO, I/O pack.                                                                     |
| 76       | K25A Relay (synch check) Driver mismatch requested state       | The driver output of I/O pack for K25A does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip terminal board. | Check I/O pack connector seating on terminal board. Check SPRO- trip card cable seating and cable integrity. Replace cable, trip terminal board, SPRO, I/O pack.                                                                     |
| 83-85    | Trip Relay (ETR) Contact [ ] mismatch requested state          | Relay feedback from Emergency Trip Relay 1 (K1), ETR2 (K2), or ETR3 (K3) does not match the commanded state. This indicates that the relay feedback from the trip terminal board does not agree with the commanded state.                | Check trip terminal board relays, cable from trip board to SPRO (if not TREA).                                                                                                                                                       |
| 86-88    | Econ Relay Contact [ ] mismatch requested state                | Relay feedback from Economizing Relay 1 (KE1), KE2, or KE3 does not match the commanded state. This indicates that the relay feedback from the trip terminal board does not agree with the commanded state.                              | Check trip terminal board relays, cable from trip board to SPRO.                                                                                                                                                                     |
| 89       | Servo Clamp Relay Contact mismatch requested state             | Relay feedback from K4CL does not match the commanded state. This indicates that the relay feedback from the trip terminal board does not agree with the commanded state.                                                                | Check I/O pack connector seating on terminal board. Check SPRO- trip card cable seating and cable integrity. Replace cable, trip terminal board, SPRO, I/O pack.                                                                     |
| 90       | K25A Relay (synch check) Coil trouble, cabling to P28V on TTUR | Relay feedback from K25A does not match the commanded state. This indicates that the relay feedback from the trip terminal board does not agree with the commanded state.                                                                | Check components of signal path- may include I/O pack, SPRO, cable, TREG, cable, TRPG, cable, TTUR, PTUR.                                                                                                                            |
| 97       | Solenoid Power Source is missing                               | Solenoid power monitoring provided by the trip terminal board indicates the absence of power.                                                                                                                                            | Check source of solenoid power. Confirm correct wiring between trip terminal boards.                                                                                                                                                 |
| 99-101   | Solenoid Voltage [ ] mismatch requested state                  | Solenoid voltage associated with K1-K3 does not match the requested state.                                                                                                                                                               | This may be due to removal of solenoid voltage through another means when I/O pack expects to see it. Review system level trip circuit wiring and confirm voltage should be present if I/O pack energizes the associated trip relay. |
| 105      | TREL/S, Solenoid Power, Bus A, Absent                          | TRES/TREL solenoid power A is absent. Solenoid power does not match solenoid state for longer than 40 milliseconds.                                                                                                                      | Check power applied to trip terminal board, field wiring, and solenoid. Replace terminal board.                                                                                                                                      |
| 106      | TREL/S, Solenoid Power, Bus B, Absent                          | TRES/TREL solenoid power B is absent. Solenoid power does not match solenoid state for longer than 40 milliseconds.                                                                                                                      | Check power applied to trip terminal board, field wiring, and solenoid. Replace terminal board.                                                                                                                                      |
| 107      | TREL/S, Solenoid Power, Bus C, Absent                          | TRES/TREL solenoid power C is absent. Solenoid power does not match solenoid state for longer than 40 milliseconds.                                                                                                                      | Check power applied to trip terminal board, field wiring, and solenoid. Replace terminal board.                                                                                                                                      |

| Alarm ID | Alarm Description                                      | Possible Cause                                                                                                                                                                                                                                                                                                                                                                       | Solution                                                                                                                                        |
|----------|--------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 108      | Control Watchdog Protection Activated                  | This alarm can only occur if Paramters -> ContWdogEn has been enabled. An alarm indicates that the signal Internal Points -> ContWdog has not changed for 5 consecutive frames. The alarm will reset itself if changes are seen for 60 seconds.                                                                                                                                      | Verify that the ContWdog is set up correctly in the toolbox and that the source of the signal is changing the value at least once a frame.      |
| 109      | Speed Difference Protection Activated                  | This alarm can only occur if Paramters -> SpeedDifEnable has been enabled. An alarm indicates that the difference between the output signal Internal Points -> Speed1 and the first I/O pack pulse rate speed is larger than the percentage Parameters -> OS_DIFF for more than 3 consecutive frames. The alarm will reset itself if the difference is within limits for 60 seconds. | Verify that the Speed1 signal is set up correctly in the ToolboxST and that the source of the signal reflects the YTUR pulse rate speed.        |
| 110      | Stale Speed Protection Activated                       | Stale speed trip protection. This alarm can only occur if Paramters -> StaleSpdEn has been enabled. An alarm indicates that the signal Internal Points -> Speed1 has not changed for 5 consecutive frames. The alarm will reset itself if the speed dithers for 60 seconds.                                                                                                          | Verify that the Speed1 signal is set up correctly in ToolboxST and that the source of the signal reflects the YTUR pulse rate speed             |
| 111      | Frame Sync Monitor Protection Activated                | This alarm can only occur if Paramters -> FrameMonEn has been enabled. An alarm indicates that the IONET synchronization was lost for at least 5 consecutive frames after the I/O pack was on line. The alarm will reset itself if the frame synch is established for at least 60 seconds.                                                                                           | Verify that the IONET is healthy. This indicates that the I/O pack is not synched with the Mark VIe start of frame signal                       |
| 112-114  | Overspeed [ ] firmware setpoint config err             | Firmware over speed limit 1 mismatch between IO signal space limit and configuration. The current configuration file downloaded from the toolbox has a different over-speed 1 limit than the IO signal OS1_Setpoint.                                                                                                                                                                 | Change the Output signal designated in InternalParameters -> OS1_Setpoint to match the configuration value under Pulse Rate -> OS_Setpoint.     |
| 115-117  | Overspeed [ ] hardware setpoint config err             | Hardware over speed limit mismatch between IO signal space limit and configuration. The current configuration file downloaded from the toolbox has a different over-speed 1 limit than the IO signal OSHW_Setpoint1.                                                                                                                                                                 | Change the Output signal designated in InternalParameters -> OSHW Setpoint [ ] to match the configuration value in Pulse Rate -> HWOS_Setpoint. |
| 118-120  | Overspeed [ ] hardware setpoint changed after power up | This alarm will always occur when Pulse Rate [ ] HWOS_Setpoint is changed and downloaded to the I/O pack after the turbine has started.                                                                                                                                                                                                                                              | Confirm that the limit change is correct. Restart the I/O pack to force the hardware overspeed to re-initialize the limit.                      |
| 121      | TREA - K1 contact string shorted                       | TREA provides voltage based detection of "stuck-on" relays in the six voting contacts used to provide K1. Zero voltage has been deteted on one or more contacts of K1 when voltage should be present.                                                                                                                                                                                | Replace TREA.                                                                                                                                   |

| Alarm ID  | Alarm Description                                            | Possible Cause                                                                                                                                                                                         | Solution                                                                             |
|-----------|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 122       | TREA - K2 contact string shorted                             | TREA provides voltage based detection of "stuck-on" relays in the six voting contacts used to provide K2. Zero voltage has been detected on one or more contacts of K2 when voltage should be present. | Replace TREA.                                                                        |
| 123       | LED - trip fault detected                                    | The TRIP LED is lit on the BPRO card because of a detected Trip condition. The LedDiag Card Parameter must be set true to get this alarm.                                                              | The condition leading to a trip condition must be cleared and a master reset issued. |
| 124       | LED - Overspeed fault detected                               | The Overspeed LED is lit on the BPRO card because of a detected Trip condition. The LedDiag Card Parameter must be set true to get this alarm.                                                         | The condition leading to a trip condition must be cleared and a master reset issued. |
| 125       | LED - Estop detected                                         | The Estop LED is lit on the BPRO card because of a detected Trip condition. The LedDiag Card Parameter must be set true to get this alarm.                                                             | The condition leading to a trip condition must be cleared and a master reset issued. |
| 126       | LED - Synch fault detected                                   | The Synch LED is lit on the BPRO card because of a detected Trip condition. The LedDiag Card Parameter must be set true to get this alarm.                                                             | The condition leading to a trip condition must be cleared and a master reset issued. |
| 224-239   | Input signal [ ] Voting Mismatch, Local={0:F3}, Voted={1:F3} | Voter disagreement between the R, S and T IO Packs                                                                                                                                                     | Adjust the TMR threshold limit or correct the cause of the difference                |
| 1128-1182 | Input signal [ ] Voting Mismatch, Local={0:F3}, Voted={1:F3} | Voter disagreement between the R, S and T IO Packs                                                                                                                                                     | Adjust the TMR threshold limit or correct the cause of the difference                |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

## ***TREA Turbine Emergency Trip***

### ***Functional Description***

The Aeroderivative Turbine Emergency Trip (TREA1A) terminal board works with PPRO turbine I/O packs as part of the Mark\* VIe system. The inputs and outputs are as follows:

- Customer input terminals provided through two 24-point pluggable barrier terminal blocks (H1A, H2A) or 48 pluggable Euro-style box terminals (H3A, H4A).
- Nine passive pulse rate devices (three per X/Y/Z section) sensing a toothed wheel to measure the turbine speed.
- Jumper blocks that enable fanning of one set of three speed inputs to all three PPRO I/O packs.
- Two 24 V dc (H1A, H3A) or 125 V dc (H2A, H4A) TMR voted output contacts to trip the system.
- Four 24-125 V dc voltage detection circuits for monitoring trip string.
- Daughterboards connectors for optional feature expansion.

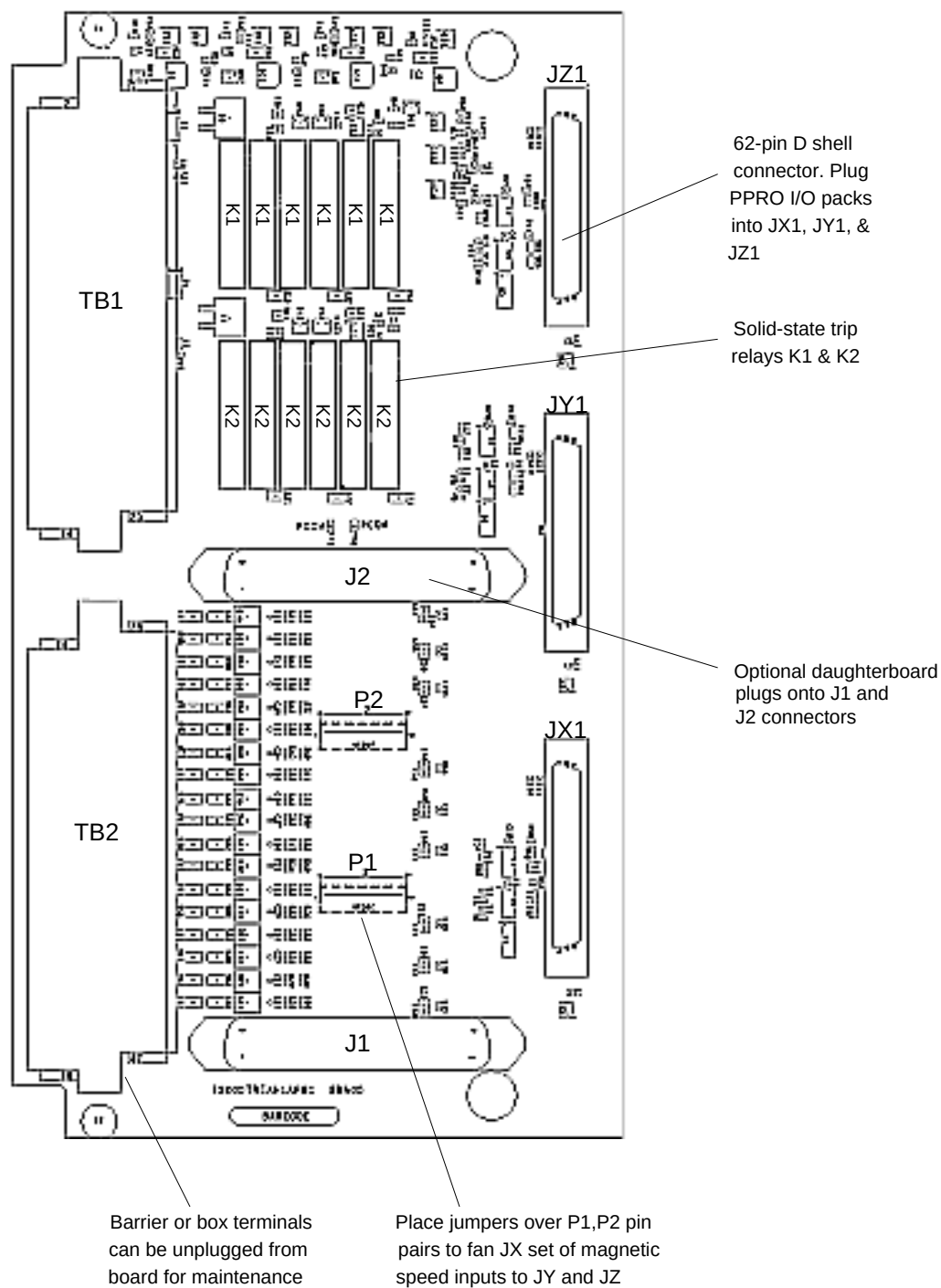
For TMR systems, signals fan out to the JX1, JY1, and JZ1 DC-62 PPRO connectors.

### ***Mark VI Systems***

TREA#A cannot be used with the Mark VI system.

## Mark VIe Systems

TREAH#A supports the Mark VIe system and accommodates PPRO I/O packs.



*TREAH1A Turbine Terminal Board*



## Installation

For H1 and H2 board variants, voltage detection and the breaker relay are wired to the I/O terminal blocks TB1. Passive pulse rate pick-ups are wired to TB2. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left of each terminal block.

For H3 and H4 board variants, voltage detection and the breaker relay are wired to the I/O box terminals at the top of the board. Passive pulse rate pick-ups are wired to the lower terminals. All terminals plug into a header on the TREA board and accept up to a single #12 AWG wire.



**The TREA must be configured for the desired speed input connections using the following table. Jumpers P1 and P2 select fanning of the X section pulse rate pickups to the Y and Z PPROs.**

### Caution

| Speed Input Connections                              | Function                                                                | Jumper                                         |
|------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------|
| Wire to all 9 pulse inputs:<br>PR1_X – PR3_Z         | Each set of three pulse inputs goes to its own dedicated PPRO I/O pack. | Cannot use jumper:<br>Place in STORE position. |
| Wire to bottom 3 pulse inputs only:<br>PR1_X – PR3_X | The same set of signals are fanned to all the PPRO I/O packs.           | Use jumper:<br>Place over pin pairs.           |
| NO wiring to PR1_Y-PR3_Z                             |                                                                         |                                                |

Screw terminal connections are listed in the following table. Terminal names starting with DBRD are reserved for the addition of an optional daughterboard.

*TREA Terminal Board Wiring*

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 1   | K1_PDC      | 2   | K1_NDC      |
| 3   | K2_PDC      | 4   | K2_NDC      |
| 5   | SOL1_A      | 6   | SOL1_B      |
| 7   | SOL2_A      | 8   | SOL2_B      |
| 9   | PWR_A       | 10  | PWR_B       |
| 11  | TRP_A       | 12  | TRP_B       |
| 13  | K4_PDC      | 14  | K4_NDC      |
| 15  | K5_PDC      | 16  | K5_NDC      |
| 17  | K6_PDC      | 18  | K6_NDC      |
| 19  | DBRD1_A     | 20  | DBRD1_B     |
| 21  | DBRD2_A     | 22  | DBRD2_B     |
| 23  | DBRD3_A     | 24  | DBRD3_B     |
| 25  | DBRD4_A     | 26  | DBRD4_B     |
| 27  | DBRD5_A     | 28  | DBRD5_B     |
| 29  | DBRD6_A     | 30  | DBRD6_B     |
| 31  | PR1H_Z      | 32  | PR1L_Z      |

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 33  | PR2H_Z      | 34  | PR2L_Z      |
| 35  | PR3H_Z      | 36  | PR3L_Z      |
| 37  | PR1H_Y      | 38  | PR1L_Y      |
| 39  | PR2H_Y      | 40  | PR2L_Y      |
| 41  | PR3H_Y      | 42  | PR3L_Y      |
| 43  | PR1H_X      | 44  | PR1L_X      |
| 45  | PR2H_X      | 46  | PR2L_X      |
| 47  | PR3H_X      | 48  | PR3L_X      |

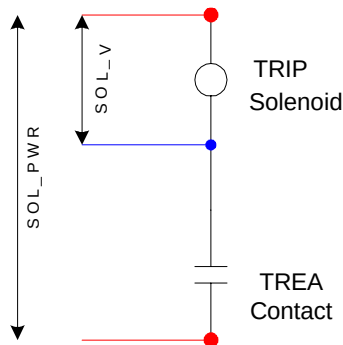
### Contact outputs



The contact outputs are polarity sensitive. Wire the circuit carefully to avoid damaging the relays. There is no contact or solenoid suppression, user must add external solenoid suppression to avoid damaging the relays and their contacts.

### Caution

A voltage detection circuit is included on TREA that is able to detect a shorted relay when voltage is present across the open contact set.



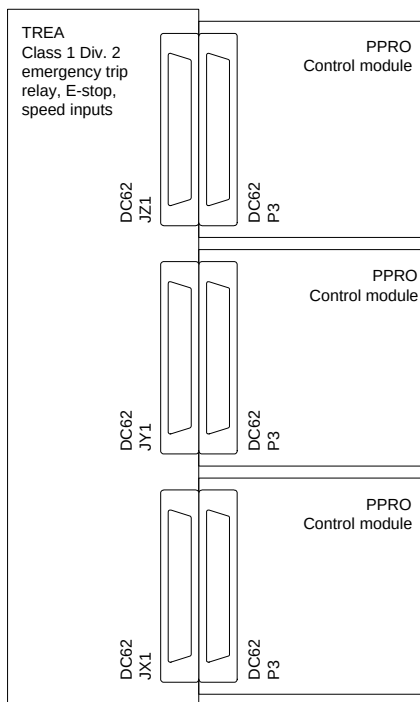
Connection to TREA contact output

### E-STOP/TRP Input

- The TRP input is configurable in PPRO to either be required or bypass the signal. When enabled the TRP input works through a hardware path on PPRO and does not act through PPRO firmware. When enabled TRP must be powered for the trip relays to close.
- The ESTOP must be connected to a CLEAN dc source battery or filtered (< 5% ripple) rectified ac.
- There must be a minimum of 18 V dc at the TRP inputs for proper operation. The current required was kept low to minimize drop on long cable runs.
- As the TRP is very fast < 5 ms and the output relay contacts are also fast (< 15 ms), best wiring practices should be utilized to avoid disoperation. Use twisted-pair cable when possible and avoid running with ac wiring.

## Operation

**System Design:** The TREA board is designed using three PPRO I/O packs mounted directly on it. The TREA / PPRO assembly then forms a self-contained emergency trip function.



TREAH1A, H2A, H3A, and H4A will only function correctly with three PPRO I/O packs. Simplex operation is not possible.

**Speed Inputs:** When used with PPRO I/O packs mounted directly on the TREA, the speed inputs provide two options. Each PPRO I/O pack may receive a dedicated set of three speed inputs from their respective TREA terminal points as is done on SPRO. As an option, jumpers P1 and P2 may be placed on the TREA to take the first three speed inputs (those for the X pack) and fan them to the Y and Z packs. When this is selected, the terminal board points for Y and Z. Speed inputs become no-connects and should not be used. As a check, the PPRO is configured for fanned or direct speed input and a feedback signal provided by TREA. If there is a mismatch between the jumper position and PPRO configuration, an alarm will be generated.

**EStop:** The TREA includes an EStop function. This consists of an optically isolated input circuit designed for a dc input in the range of 24 V to 125 V nominal. When energized, the circuit enables coil drive power in the X, Y, and Z relay circuits through independent hardware paths. The response time of this circuit of less than five milliseconds plus the response time of the trip relays of less than one millisecond yields very fast EStop response. EStop is monitored by PPRO firmware, but the action to remove trip relay coil power is a hardware path in PPRO. It is possible to configure PPRO to turn off the Estop function.

**Voltage Monitors:** The trip relays on TREA may be freely located anywhere in a trip string. Because the trip string circuit is not fixed, there are three general-purpose isolated voltage sensor inputs on TREA. These may be used to monitor any points in the trip system and drive the voltage status into the system controller where action may be taken. Typical use of these inputs may be to sense the power supply voltage for the two trip strings (PWR) and to sense the solenoid voltage of the device being driven by the relays (SOL1, SOL2). This set of applications is used in the wording of the board symbol, but the sensors may be freely applied to best serve the application.

**Trip Relays:** The trip relays are made using sets of six individual form devices arranged in a voting pattern. Any two controllers that vote to close will establish a conduction path through the set. Because detection of a shorted relay is important to preserve tripping reliability, there is a sensing circuit applied to each of the sets of relays. When the relays are commanded to open, and voltage is present across the relays, the circuit will detect if one or more relays are shorted. This signal goes to the PPRO I/O pack to create an alarm. The TREA sensing circuit uses the relay commands from all three packs to avoid a false indication, in the event that one PPRO I/O pack votes to close the relay while the other two PTUR I/O packs vote to open. The voting arrangement is shown in the following TREA symbol.

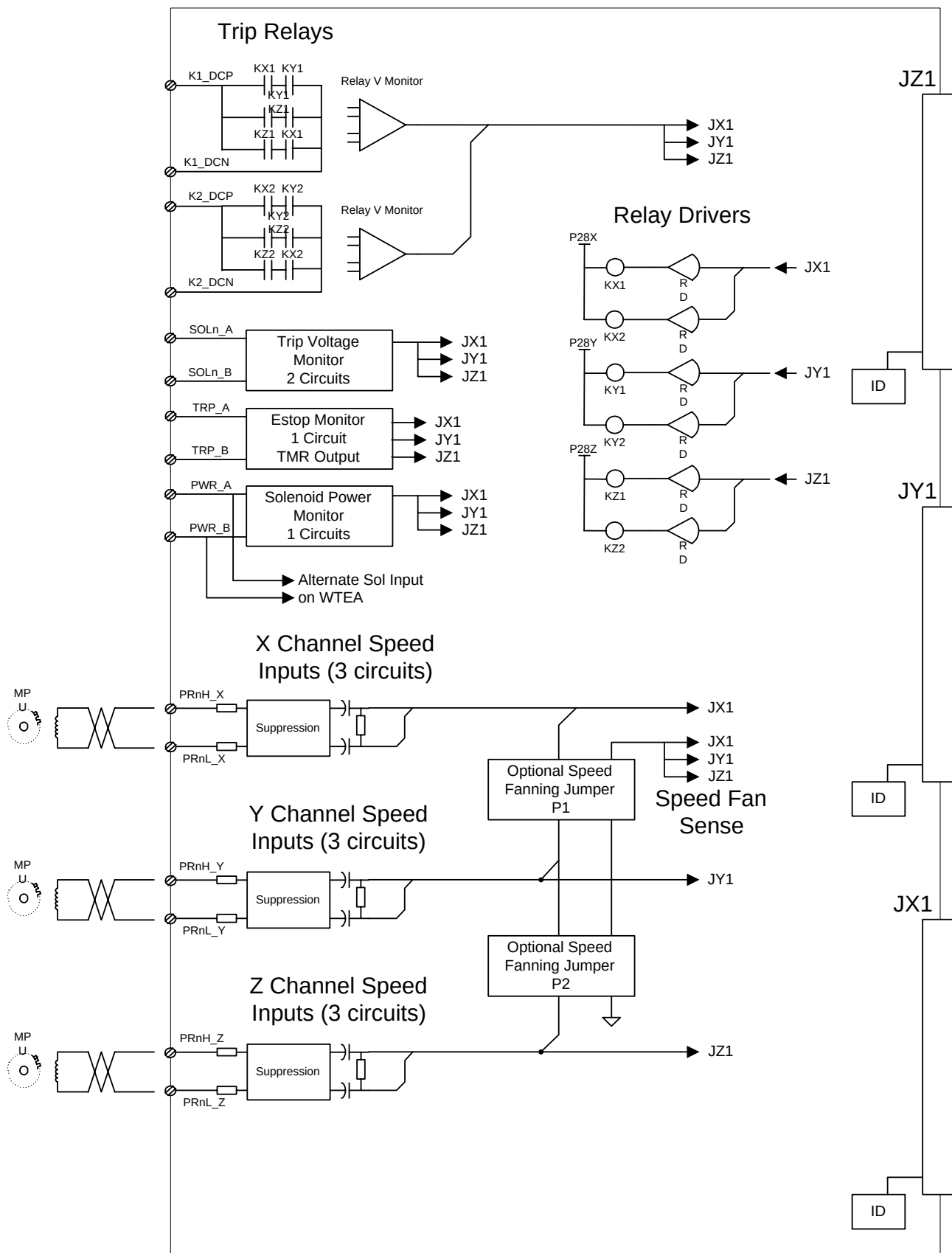
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**Contacts are polarity-sensitive, external voltage suppression MUST be used.**

***Caution***

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TREA1A Trip Board

**Note** The above drawing is simplified with many circuit paths omitted for clarity.

## ***Specifications***

| <b>Item</b>                   | <b>Specification</b>                                                                                                                                                                                                                             |
|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs              | 3 x 3 passive (magnetic) speed pickups<br>3 voltage detection circuits<br>1 ESTOP/TRP input                                                                                                                                                      |
| Number of outputs             | 2 trip contacts                                                                                                                                                                                                                                  |
| Contact ratings               | NEMA class F. Minimum operations: 100,000.                                                                                                                                                                                                       |
| IS200TREA1A, H3A              | Voltage: 28 V dc max<br>Max. Current 10 A dc @ 40°C (104 °F) maximum<br>de-rate current linearly to 7 A dc @ 65°C (149 °F) maximum.<br>Leakage: 2.21 mA max                                                                                      |
| IS200TREA2A, H4A              | Voltage: 145 V dc max<br>Max. Current 3 A dc @ 40°C (104 °F) maximum<br>de-rate current linearly to 2 A dc @ 65°C (149 °F) maximum<br>Leakage: 3.31 mA max                                                                                       |
| Voltage detection inputs      | Min/max input voltage rating: 16/150 V dc max pk<br>Current Loading (Max leakage): 3 mA<br>Detection delay (max): 60 ms<br>Voltage isolation: Optically isolated: 2500 V rms isolation, for one min.<br>Surge/Spike rating: 1000 V pk for 8.3 ms |
| ESTOP/TRP detection           | Input Voltage: 24-125 V dc $\pm 10\%$ (18/150 V pk Min/Max)<br>Loading (max): 12 mA (5 typical)<br>Delay (max): 5 ms (<1 typical)                                                                                                                |
| MPU pulse rate range          | 2 Hz to 20 kHz                                                                                                                                                                                                                                   |
| MPU pulse rate accuracy       | 0.05% of reading                                                                                                                                                                                                                                 |
| MPU input circuit sensitivity | 27 mV pk (detects 2 rpm speed)                                                                                                                                                                                                                   |
| <b>Physical</b>               |                                                                                                                                                                                                                                                  |
| Size                          | 33.0 cm high x 17.8 cm, wide (13 in. x 7 in.)                                                                                                                                                                                                    |
| Technology                    | Surface mount                                                                                                                                                                                                                                    |
| Temperature                   | -30 to 65°C (-22 to +149 °F)                                                                                                                                                                                                                     |

## ***Diagnostics***

Diagnostic tests are made on the terminal board:

- Feedback from the shorted contact detector is checked, if a shorted relay is detected an alarm will be created.
- Feedback from speed pickup fanning jumpers is checked; if there is a mismatch between intention and actual position, an alarm is created.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm xxDIAG\_PPPO occurs. The diagnostic signals can be individually latched and then reset with the RESET\_DIA signal if they go healthy.
- Terminal board connectors have their own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by PPPO and a mismatch is encountered, a hardware incompatibility fault is created.

## **Configuration**

Jumpers JP1 and JP2 select the fanning of the 3 X section passive speed pickups to the S and T section PPROs. Place the jumper over the pin pairs if you want to fan the 3 R speed input to the other two TMR sections.

---

# **TREG Turbine Emergency Trip**

## **Functional Description**

The Gas Turbine Emergency Trip (TREG) terminal board provides power to three emergency trip solenoids and is controlled by the I/O controller. Up to three trip solenoids can be connected between the TREG and TRPG terminal boards. TREG provides the positive side of the dc power to the solenoids and TRPG provides the negative side. The I/O controller provides emergency overspeed protection, emergency stop functions, and controls the 12 relays on TREG, nine of which form three groups of three to vote inputs controlling the three trip solenoids.

There are a number of board types as follows:

- The H1A version is not used for new production and is replaced by H1B.
- H1B is the primary version for 125 V dc applications. Control power from the JX1, JY1, and JZ1 connectors are diode combined to create redundant power on the board for status feedback circuits and powering the economizing relays. Power separation is maintained for the trip relay circuits.
- H2B is used for 24 V dc applications. All other features are the same as H1B.
- H3B is a special version of H1B for use in systems with redundant TREG boards. Feedback circuit and economizing relay power is provided only by the JX1 connector.
- H4B is a special version of H1B for use in systems with redundant TREG boards. Feedback circuit and economizing relay power is provided only by the JY1 connector.
- H5B is a special version of H1B for use in systems with redundant TREG boards. Feedback circuit and economizing relay power is provided only by the JZ1 connector.

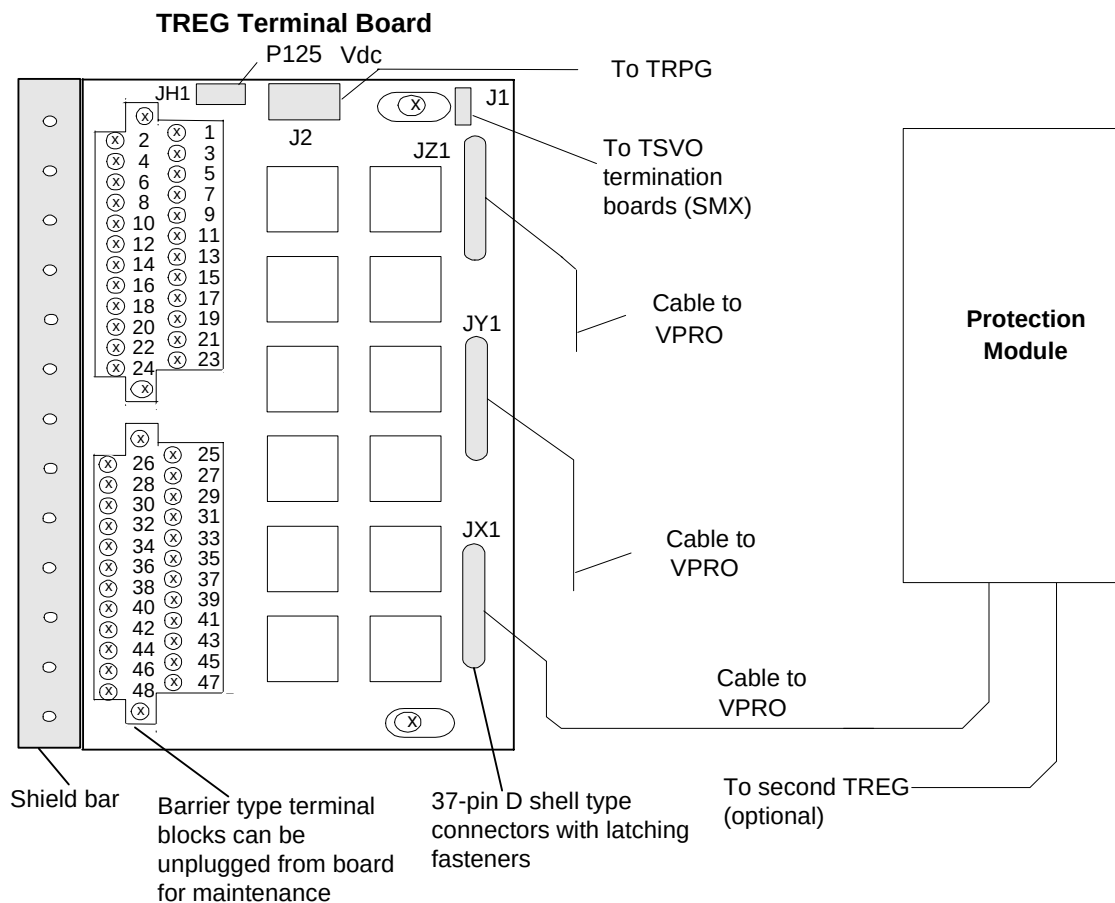
In redundant TREG applications, it is typical to find one H3B and one H4B board used together. It is important that system repairs be done with the correct board type to maintain the control power separation designed into these systems.

## **Mark VI Systems**

In Mark\* VI systems, the VPRO works with the TREG terminal board. Cables with molded plugs connect TREG to the VPRO module.

## **Mark VIe Systems**

In Mark VIe systems, TREG is controlled by the PPRO pack on SPRO. The PPRO I/O packs plug into the D-type connectors on SPRO. Cables with molded plugs connect TREG to the SPRO board.



*TREG Turbine Emergency Trip Terminal Board, and Protection Module I/O Controller*



The three trip solenoids, economizing resistors, and the emergency stop are wired directly to the first I/O terminal block. Up to seven trip interlocks can be wired to the second terminal block. The wiring connections are shown in the following figure.

**Turbine Emergency Trip Terminal Board TREG**

Power 125V dc

To TRPG, 12 wires

To TSVO boards on SMX systems

JH1

J2

J1

JZ1

JY1

JX1

VPRO

VPRO

VPRO

1 SOL 1 or 4  
2 RES 1A  
3 SOL 2 or 5  
4 RES 2A  
5 SOL 3 or 6  
6 RES 3A  
7 E-TRP (H)  
8 E-TRP (L)  
9 JUMPER  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24

25  
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35  
36  
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41  
42  
43  
44  
45  
46  
47  
48

PWR\_N1  
RES 1B  
PWR\_N2  
RES 2B  
PWR\_N3  
RES 3B  
E-TRP (H)  
E-TRP (L)

PWR\_P2 (for probe)

PWR\_P1 (for probe)

Contact TRP1 (L)  
Contact TRP2 (L)  
Contact TRP3 (L)  
Contact TRP4 (L)  
Contact TRP5 (L)  
Contact TRP6 (L)  
Contact TRP7 (L)

Contact TRP1 (H)  
Contact TRP2 (H)  
Contact TRP3 (H)  
Contact TRP4 (H)  
Contact TRP5 (H)  
Contact TRP6 (H)  
Contact TRP7 (H)

Up to two #12 AWG wires per point with 300 volt insulation

Terminal blocks can be unplugged from terminal board for maintenance

GEH-6721G Mark VIe Control System Guide Volume II

## Operation

TREG is entirely controlled by the VPRO protection module, and the only connections to the control modules are the J2 power cable and through the trip solenoids. In simplex systems a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

### Control of Trip Solenoids

Both TRPG and TREG control the trip solenoids so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. The nine trip relay coils on TREG are supplied with 28 V dc from the I/O controller. The trip solenoids are supplied with 125 V dc through plug J2, and draw up to 1 A with a 0.1 second L/R time constant.

---

**Note** The solenoid circuit has a metal oxide varistor (MOV) for current suppression and a 10  $\Omega$ , 70 W economizing resistor.

---

A separately fused 125 V dc feeder is provided from the turbine control for the solenoids, which energize in the run mode and de-energize in the trip mode. Diagnostics monitor each 125 V dc feeder from the power distribution module at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

Two series contacts from each emergency trip relay (ETR1, 2, 3) are connected to the positive 125 V dc feeder for each solenoid, and two series contacts from each primary trip relay (PTR1,2,3 in TRPG) are connected to the negative 125 V dc feeder for each solenoid. An economizing relay (KE1, 2, 3) is supplied for each solenoid with a normally closed contact in parallel with the current limiting resistor. These relays are used to reduce the current load after the solenoids are energized. The ETR and KE relay coils are powered from a 28 V dc source from the I/O controller. Each I/O controller in each of the R8, S8, and T8 sections supplies an independent 28 V dc source.

The 28 V dc bus is current limited and used for power to an external manual emergency trip contact, shown as E-STOP. Three master trip relays (K4X, K4Y, K4Z) disconnect the 28 V dc bus from the ETR, and KE relay coils if a manual emergency trip occurs. Any trip that originates in either the protection module (such as EOS) or the TREG (such as a manual trip) will cause each of the three protection module sections to transmit a trip command over the IONet to the control module, and may be used to identify the source of the trip.

In addition, the K4CL servo clamp relay will energize and send a contact feedback directly from the TREG terminal board to the TSVO servo terminal board. TSVO disconnects the servo current source from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high.

---

**Note** The primary and emergency overspeed systems will trip the hydraulic trip solenoids independent of this circuit.

---



## ***Solenoid Trip Tests***

Application software in the controller is used to initiate tests of the trip solenoids. Online tests allow each of the trip solenoids to be manually tripped one at a time, either through the PTR relays from the controller, or through the ETR relays from the protection module. A contact from each solenoid circuit is wired back as a contact input to give a positive indication that the solenoid has tripped. Primary and emergency offline overspeed tests are provided too for verification of actual trips due to software simulated trip overspeed conditions.

## ***Specifications***

| <b>Item</b>                         | <b>Specification</b>                                                                                                                        |
|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Number of trip solenoids            | Three solenoids per TREG (total of six per I/O controller)                                                                                  |
| Trip solenoid rating                | H1 - 125 V dc standard with 1 A draw<br>H2 - 24 V dc is alternate with 1 A draw                                                             |
| Trip solenoid circuits              | Circuits rated for NEMA class E creepage and clearance<br>Circuits can clear a 15 A fuse with all circuits fully loaded                     |
| Solenoid inductance                 | Solenoid maximum L/R time constant is 0.1 second                                                                                            |
| Suppression                         | MOV across the solenoid                                                                                                                     |
| Relay outputs                       | Three economizer relay outputs, two second delay to energize<br>Driver to breaker relay K25A on TTUR<br>Servo clamp relay on TSVO           |
| Solenoid control relay contacts     | Contacts are rated to interrupt inductive solenoid loads at 125 V dc, 1 A<br>Bus voltage can vary from 70 to 145 V dc                       |
| Trip inputs                         | Seven trip interlocks to the I/O controller protection module, 125/24 V dc<br>One emergency stop hard wired trip interlock, 24 V dc         |
| Trip interlock excitation           | H1 - Nominal 125 V dc, floating, ranging from 100 to 145 V dc<br>H2 - Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc               |
| Trip interlock current              | H1 for 125 V dc applications:<br>Circuits draw 2.5 mA (50 $\Omega$ )<br>H2 for 24 V dc applications:<br>Circuits draw 2.5 mA (10 $\Omega$ ) |
| Trip interlock isolation            | Optical isolation to 1500 V on all inputs                                                                                                   |
| Trip interlock filter               | Hardware filter, 4 ms                                                                                                                       |
| Trip interlock ac voltage rejection | 60 V rms @ 50/60 Hz at 125 V dc excitation                                                                                                  |
| Size                                | 17.8 cm wide x 33.02 cm, high (7.0 in x 13.0 in)                                                                                            |

## ***Diagnostics***

The I/O controller runs diagnostics on the TREG board and connected devices. The diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, economizer relay driver and contact feedbacks, K25A relay driver and coil, servo clamp relay driver and contact feedback, and the solenoid voltage source. If any of these do not agree with the desired value then a fault is created.

TREG connectors JX1, JY1, and JZ1 have their own ID device that is interrogated by I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location. When the chip is read by the I/O board and a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no switches on the terminal board.

---

**Note** A jumper must be placed across terminals 15 and 17 if the second emergency stop input is not required.

---

---

# ***TREL Turbine Emergency Trip***

## ***Functional Description***

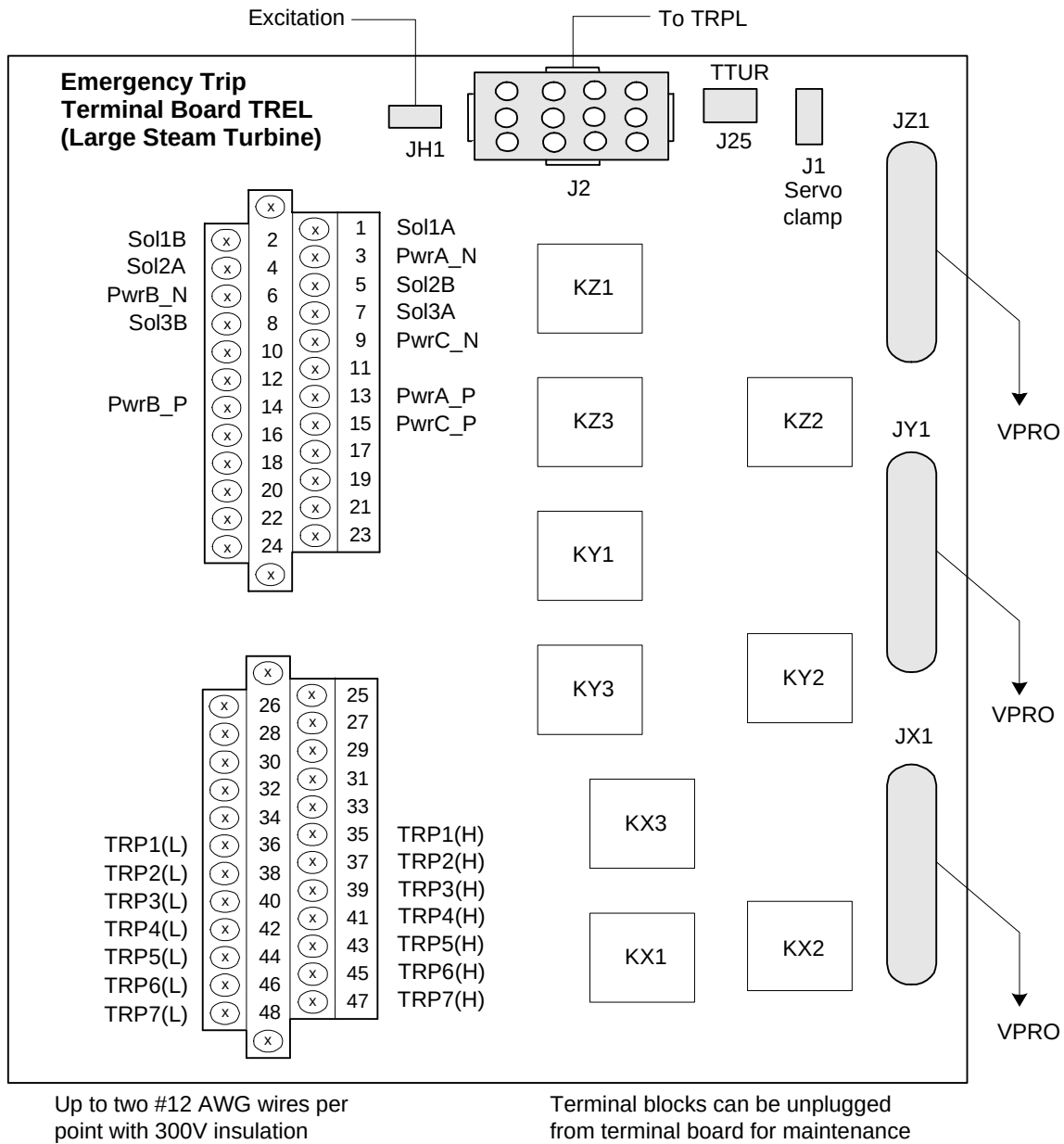
The Large Steam Turbine Emergency Trip (TREL) terminal board is used for the emergency overspeed protection for large steam turbines. TREL is controlled by the VPRO in the protection module, and provides power to three emergency trip solenoids, which can be connected between the TREL and TRPL terminal boards. TREL provides the positive side of the 125 V dc to the solenoids and TRPL provides the negative side. I/O controller provides emergency overspeed protection, emergency stop functions, and controls the nine relays on TREL, which form three groups of three to vote inputs controlling the three trip solenoids. The three groups are called ETR (emergency trip) 1, 2, and 3.

- TREL is only available in TMR form.
- TREL has no economizing relay as with TREG.
- TREL has no E-STOP function as with TREG.

A second TREL board may be driven from the protection module.

## Installation

The three trip solenoids are wired to the first I/O terminal block. Up to seven trip interlocks are wired to the second terminal block. The wiring connections are shown in the following figure. Connector J2 carries three power buses from TRPL, and JH1 carries the excitation voltage for the seven trip interlocks.



*TREL Terminal Board Wiring*

## Operation

TREL is entirely controlled by the VPRO protection module, and the only connections to the turbine control are the J2 power cable and the trip solenoids. In simplex systems, a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

### Control of Trip Solenoids

Both TRPL and TREL control the trip solenoids 1 and 2 so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. ETR3 is set up to supply power to trip solenoid #3. The nine trip relay coils on TREL are supplied with 28 V dc from I/O controller. The trip solenoids are supplied with 125 V dc (or 24 V dc) through plug J2, and draw up to 1 A with a 0.1 second L/R time constant.

---

**Note** The solenoid circuit has an MOV for current suppression on TRPL.

---

A separately fused 125 V dc feeder is provided from the PDM to the solenoids. Diagnostics monitor each 125 V dc feeder from the PDM at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

---

**Note** A normally closed contact from each relay is used to sense the relay status for diagnostics.

---

Two series contacts from each of the emergency trip relays (ETR1, 2, 3) are connected to the positive 125 V dc feeder for each solenoid, and two series contacts from each of the primary trip relays are connected to the negative 125 V dc feeder for each solenoid. The ETR relay coils are powered from a 28 V dc source from the I/O controller. Each I/O controller in each of the R8, S8, and T8 sections supplies an independent 28 V dc source.

The K4CL servo clamp relay will energize and send a contact feedback directly from the TREL terminal board to the TSVO servo terminal board. TSVO disconnects the servo current source from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high.

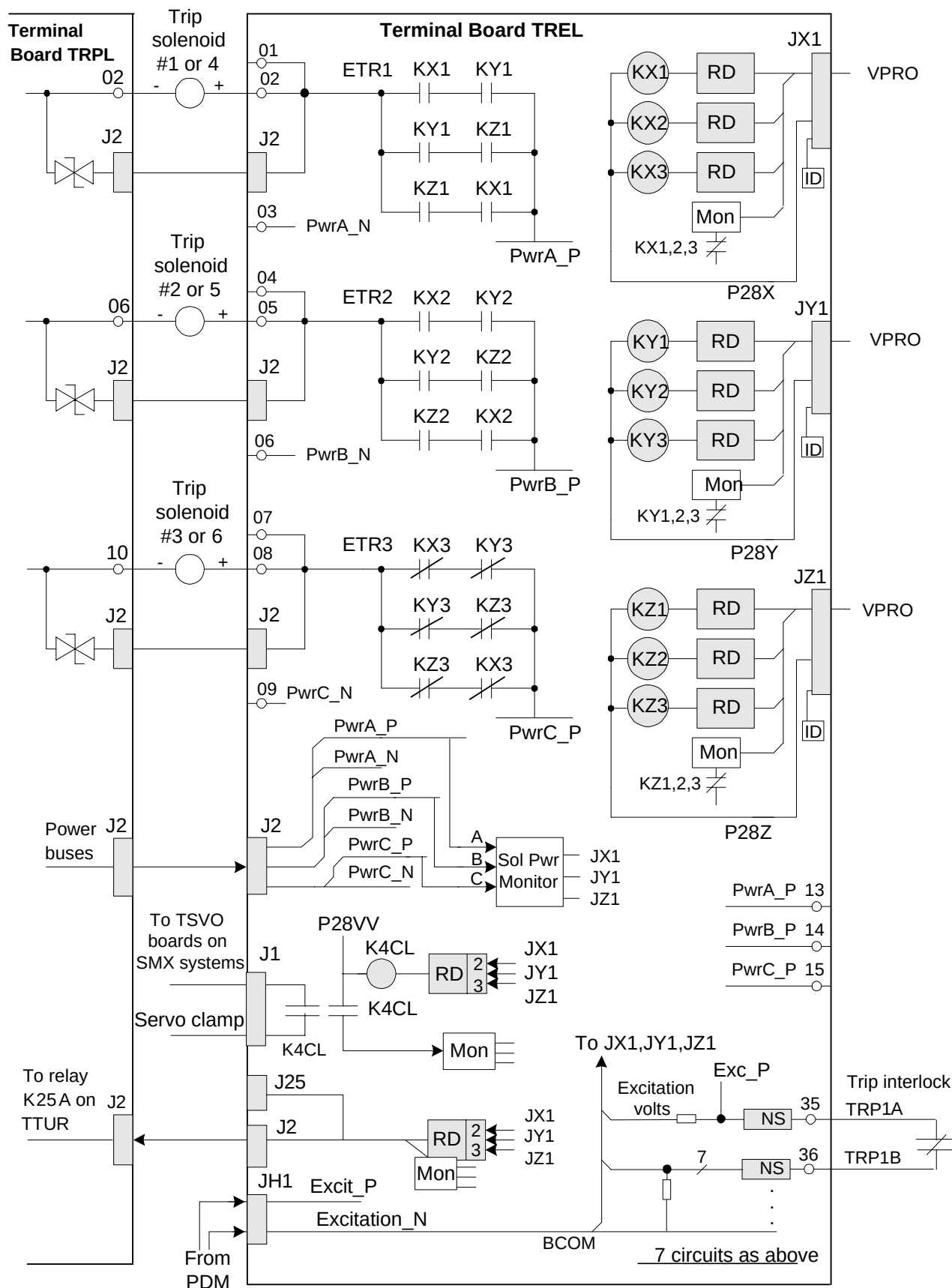
---

**Note** The primary and emergency overspeed systems will trip the hydraulic trip solenoids independent of this circuit.

---

### Solenoid Trip Tests

Application software in the controller is used to initiate tests of the trip solenoids. Online tests allow each of the trip solenoids to be manually tripped one at a time, either through the PTR relays from the controller, or through the ETR relays from the protection module. A contact from each solenoid circuit is wired back as a contact input to give a positive indication that the solenoid has tripped. Primary and emergency offline overspeed tests are provided too for verification of actual trips due to software simulated trip overspeed conditions.



TREL Terminal Board, Trip Interlocks, and Trip Solenoids

## Specifications



| Item                                | Specification                                                                                                                               |
|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Number of trip solenoids            | Three solenoids per TREL (total of six per I/O controller)                                                                                  |
| Trip solenoid rating                | H1 - 125 V dc standard with 1 A draw<br>H2 - 24 V dc is alternate with 3 A draw                                                             |
| Trip solenoid circuits              | Circuits rated for NEMA class E creepage and clearance<br>Circuits can clear a 15 A fuse with all circuits fully loaded                     |
| Solenoid inductance                 | Solenoid maximum L/R time constant is 0.1 sec                                                                                               |
| Suppression                         | MOV on TRPL across the solenoid                                                                                                             |
| Relay Outputs                       | Driver to breaker relay K25A on TTUR.<br>Servo clamp relay on TSVO                                                                          |
| Solenoid control relay contacts     | Contacts are rated to interrupt inductive solenoid loads at 125 V dc, 1 A.<br>Bus voltage can vary from 70 to 145 V dc                      |
| Trip inputs                         | Seven trip interlocks to the I/O controller protection module, 125/24 V dc                                                                  |
| Trip interlock excitation           | H1 - Nominal 125 V dc, floating, ranging from 100 to 145 V dc<br>H2 - Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc               |
| Trip interlock current              | H1 for 125 V dc applications:<br>Circuits draw 2.5 mA (50 $\Omega$ )<br>H2 for 24 V dc applications:<br>Circuits draw 2.5 mA (10 $\Omega$ ) |
| Trip interlock isolation            | Optical isolation to 1500 V on all inputs                                                                                                   |
| Trip interlock filter               | Hardware filter, 4 ms                                                                                                                       |
| Trip interlock ac voltage rejection | 60 V rms @ 50/60 Hz at 125 V dc excitation                                                                                                  |
| Size                                | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                             |

## ***Diagnostics***

The protection module runs diagnostics on the TREL board and connected devices. The diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, K25A relay driver and coil, servo clamp relay driver and contact feedback, and the solenoid voltage source. If any of these do not agree with the desired value, a fault is created.

TREL connectors JX1, JY1, and JZ1 have their own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location. When the chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no jumpers or hardware settings on the board.

---

# **TRES Turbine Emergency Trip**

## ***Functional Description***

The Small Steam Turbine Emergency Trip (TRES) terminal board is used for the emergency overspeed protection for small/medium size steam turbines. TRES is controlled by the VPRO protection module, and provides power to three emergency trip solenoids, which can be connected between the TRES and TRPS terminal boards. TRES provides the positive side of the 125 V dc to the solenoids and TRPS provides the negative side. The VPRO provides emergency overspeed protection, emergency stop functions, and controls the three relays on TRES, which control the three trip solenoids.

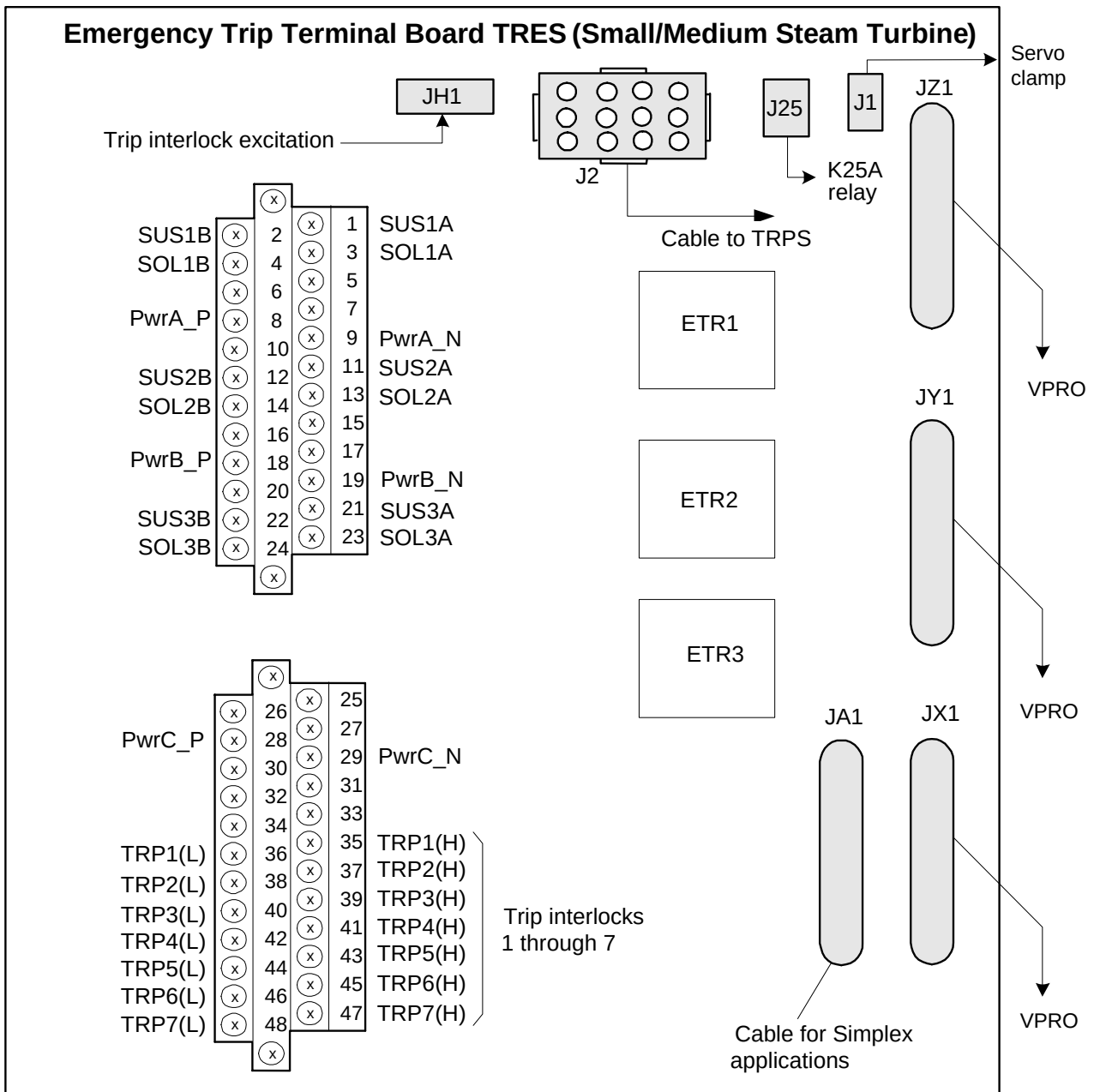
- TRES has both simplex and TMR form.
- There are seven dry contact inputs for trip interlocks.
- TRES has no economizing relays.
- There are no emergency stop inputs.

In the TRES, the seven dry contact inputs excitation and signal are monitored and fanned to the protection module. The board includes the synch check relay driver, K25A, and associated monitoring, the same as on TREG, and the servo clamp relay driver, K4CL, and its associated monitoring. A second TRES board cannot be driven from the protection module.

## ***Installation***

The three trip solenoids are wired to the first I/O terminal block. Up to seven trip interlocks are wired to the second terminal block. The wiring connections are shown in the following figure.

Connector J2 carries three power buses from TRPS, and JH1 carries the excitation voltage for the seven trip interlocks.



Up to two #12 AWG wires per point with 300V insulation

Terminal blocks can be unplugged from terminal board for maintenance

*TRES Terminal Board Wiring*

## Operation

The VSVO protection module controls TRES. In simplex systems, a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

### Control of Trip Solenoids

Both TREL and TRES control the trip solenoids 1 and 2 so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. ETR3 is set up to supply power to trip solenoid #3. The nine trip relay coils on TRES are supplied with 28 V dc from the I/O controller. The trip solenoids are supplied with 125 V dc (or 24 V dc) through plug J2, and draw up to 1 A with a 0.1 second L/R time constant.

---

**Note** The solenoid circuit has an MOV for current suppression on TREL.

---

A separately fused 125 V dc feeder is provided from the PDM for the solenoids. Diagnostics monitor each 125 V dc feeder from the PDM at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

---

**Note** A normally closed contact from each relay is used to sense the relay status for diagnostics

---

Two series contacts from each of the emergency trip relays (ETR1, 2, 3) are connected to the positive 125 V dc feeder for each solenoid, and two series contacts from each of the primary trip relays are connected to the negative 125 V dc feeder for each solenoid. The ETR relay coils are powered from a 28 V dc source from the I/O controller. Each I/O controller in each of the R8, S8, and T8 sections supplies an independent 28 V dc source.

The K4CL servo clamp relay will energize and send a contact feedback directly from the TRES terminal board to the TSVO servo terminal board. TSVO disconnects the servo current source from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high.

---

**Note** The primary and emergency overspeed systems will trip the hydraulic trip solenoids independent of this circuit.

---

### Solenoid Trip Tests

Application software in the controller is used to initiate tests of the trip solenoids. Online tests allow each of the trip solenoids to be manually tripped one at a time, either through the PTR relays from the controller, or through the ETR relays from the protection module. A contact from each solenoid circuit is wired back as a contact input to give a positive indication that the solenoid has tripped. Primary and emergency offline overspeed tests are provided too for verification of actual trips due to software simulated trip overspeed conditions.



## Specifications

| Item                                | Specification                                                                                                                               |
|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Number of trip solenoids            | Three solenoids per TRES                                                                                                                    |
| Trip solenoid rating                | 125 V dc standard with 1 A draw<br>24 V dc is alternate with 3 A draw                                                                       |
| Trip solenoid circuits              | Circuits rated for NEMA class E creepage and clearance<br>Circuits can clear a 15 A fuse with all circuits fully loaded                     |
| Solenoid inductance                 | Solenoid maximum L/R time constant is 0.1 sec                                                                                               |
| Suppression                         | MOV on TRPS across the solenoid                                                                                                             |
| Relay Outputs                       | Driver to breaker relay K25A on TTUR<br>Servo clamp relay on TSVO                                                                           |
| Solenoid control relay contacts     | Contacts are rated to interrupt inductive solenoid loads at 125 V dc, 1 A.<br>Bus voltage can vary from 70 to 145 V dc.                     |
| Trip inputs                         | Seven trip interlocks to VPRO protection module                                                                                             |
| Trip interlock excitation           | H1 - Nominal 125 V dc, floating, ranging from 100 to 145 V dc<br>H2 - Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc               |
| Trip interlock current              | H1 for 125 V dc applications:<br>Circuits draw 2.5 mA (50 $\Omega$ )<br>H2 for 24 V dc applications:<br>Circuits draw 2.5 mA (10 $\Omega$ ) |
| Trip interlock isolation            | Optical isolation to 1500 V on all inputs                                                                                                   |
| Trip interlock filter               | Hardware filter, 4 ms                                                                                                                       |
| Trip interlock ac voltage rejection | 60 V rms @ 50/60 Hz at 125 V dc excitation                                                                                                  |
| Size                                | 17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)                                                                                             |

## Diagnostics

The I/O controller runs diagnostics on the TRES board and connected devices. The diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, K25A relay driver and coil, servo clamp relay driver and contact feedback, and the solenoid voltage source. If any of these do not agree with the desired value, a fault is created.

TRES connectors JA1, JX1, JY1, and JZ1 have their own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location. When the chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

There are no jumpers or hardware settings on the board.

---

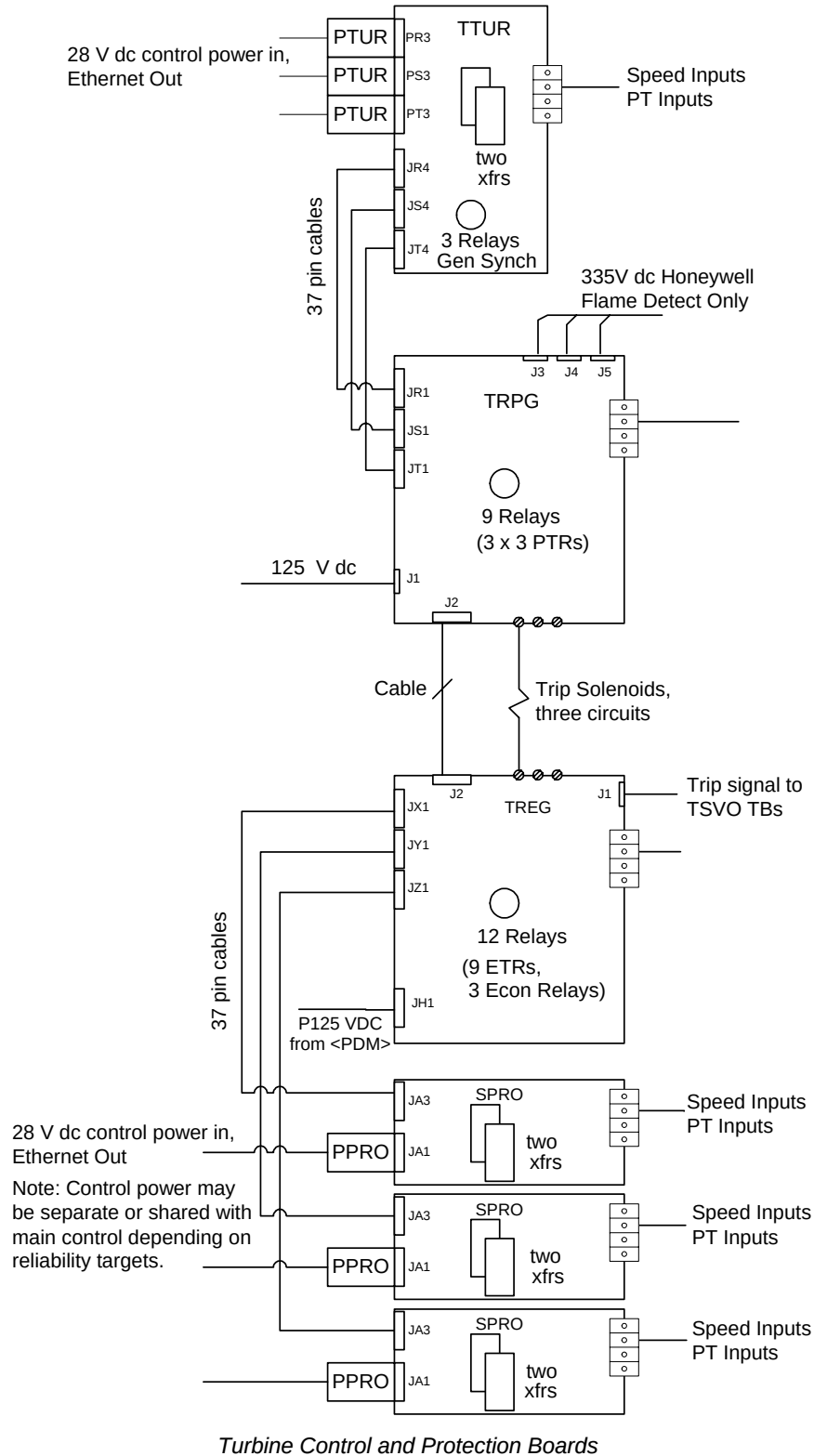
# ***SPRO Emergency Protection***

## ***Functional Description***

The Emergency Protection (SPRO) terminal board hosts a PPRO I/O pack. It conditions speed signal inputs for the PPRO and contains a pair of potential transformers (PTs) for bus and generator voltage input. It has a DC-37 pin connector adjacent to the PPRO pack connector that accepts a cable leading to a Mark\* VIe backup trip relay terminal board.

- SPROH1A features 24 barrier terminals in a pluggable block.
- SPROH2A features 24 pluggable Euro-style box terminals.

The following figure shows how the SPRO and PPRO with cabling into a trip relay board form the backup protection in a Mark VIe system. Primary protection is provided by PTUR, TTUR, and a primary trip relay terminal board.





## ***I/O pack and Terminal Board Compatibility***

SPRO accepts direct mounting of one PPROH1A and provides DC-37 connector for a cable to the selected backup trip relay terminal board. SPRO is cable-compatible with the trip boards listed in the following table.

| Board   | TMR | Simplex | Output Contacts<br>125 V dc | Output<br>Contacts<br>24 V dc | ESTOP | Input<br>Contacts<br>125 V dc | Input<br>Contacts<br>24 V dc | Economy<br>Resistor |
|---------|-----|---------|-----------------------------|-------------------------------|-------|-------------------------------|------------------------------|---------------------|
| TREGH1B | Yes | No      | Yes                         | Yes                           | Yes   | Yes                           | No                           | Yes                 |
| TREGH2B | Yes | No      | Yes                         | Yes                           | Yes   | No                            | Yes                          | Yes                 |
| TRELH1A | Yes | No      | Yes                         | Yes                           | No    | Yes                           | No                           | No                  |
| TRELH2A | Yes | No      | Yes                         | Yes                           | No    | No                            | Yes                          | No                  |
| TRESH1A | Yes | Yes     | Yes                         | Yes                           | No    | Yes                           | No                           | No                  |
| TRESH2A | Yes | Yes     | Yes                         | Yes                           | No    | No                            | Yes                          | No                  |
| TREAH1A | Yes | No      | Yes                         | No                            | No    | Yes                           | No                           | No                  |
| TREAH2A | Yes | No      | No                          | Yes                           | No    | No                            | Yes                          | No                  |

## ***Main Control Compatibility***

Please refer to *GEI-100596 PPRO Turbine Protection* documentation for a description of the different backup protection arrangements available for simplex, dual, and TMR controls.

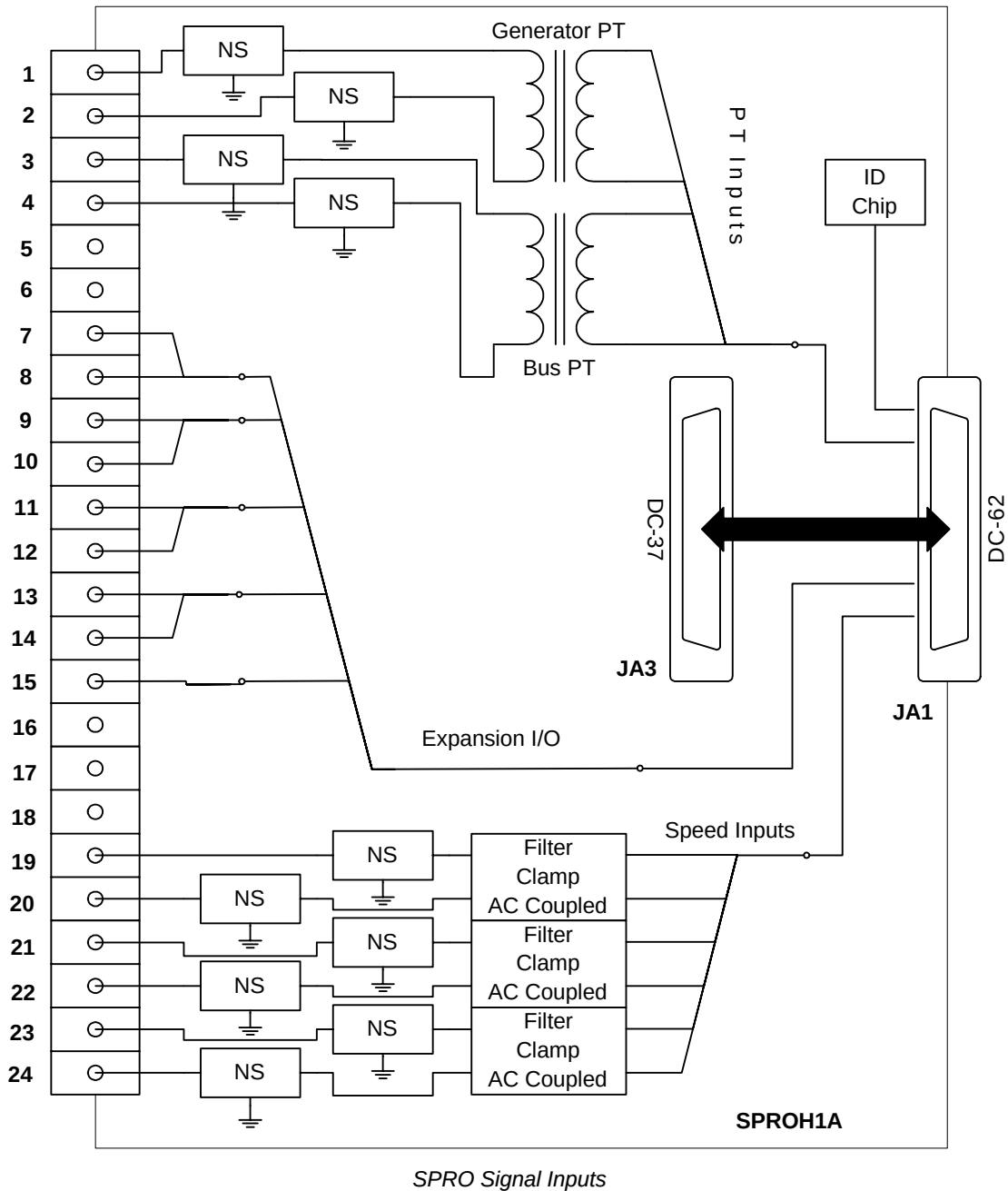
## ***Installation***

The SPRO and a plastic insulator mount on a sheet metal carrier, which mounts on a DIN-rail. Optionally, the SPRO and insulator mount on a sheet metal assembly, which bolts directly in a panel. Speed signals and PT inputs are wired directly to the terminal block using typical #18 AWG wires. The SPROH1A barrier terminal block is removable for board replacement. The SPROH2A Euro-Block type terminal block has terminals that can be removed for board replacement.

The PPRO I/O pack mounts directly on connector JA1 of the SPRO. A DC-37 pin conductor cable plugs into connector JA3 of SPRO with the other end attached to the selected backup trip terminal board.

## Operation

In the following drawing, the PT inputs to SPRO are shown on terminals 1-4. Three speed inputs are shown on terminals 19-24. Terminals 7-15 are reserved for future control feature expansion and are routed to the JA1 PPRO connector. Terminals 5-6 and 16-18 have no board connection. The JA1 and JA3 connectors provide locations for PPRO and the trip terminal board cable.



## ***Specification***

| <b>Item</b>                               | <b>Specification</b>                                                                                                                                                                                                                                                                                                             |
|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Generator and bus voltage sensors         | Two single-phase potential transformers, with secondary output supplying a nominal 115 V rms<br>Each input has less than 3 VA of loading.<br>Allowable voltage range for synch is 75 to 130 V rms<br>Each PT input is magnetically isolated with a 1,500 V rms barrier.<br>Cable length can be up to 1,000 ft. of 18 AWG wiring. |
| Magnetic speed pickup pulse rate range    | 2 Hz to 20,000 Hz                                                                                                                                                                                                                                                                                                                |
| Magnetic speed pickup pulse rate accuracy | 0.05% of reading                                                                                                                                                                                                                                                                                                                 |
| Magnetic speed pickup sensitivity         | 27 mV pk (detects 2 rpm speed)                                                                                                                                                                                                                                                                                                   |
| Size                                      | 15.9 cm high x 17.8 cm wide (6.25 in. x 7.0 in.)                                                                                                                                                                                                                                                                                 |
| Technology                                | Surface-mount                                                                                                                                                                                                                                                                                                                    |
| Temperature                               | Operating: -30 to 65°C (-22 to +149 °F)                                                                                                                                                                                                                                                                                          |

## ***Diagnostics***

The SPRO board and backup trip relay terminal board contain electronic ID parts that are read during power initialization. This information is used by PPRO to confirm a valid hardware arrangement prior to starting normal operation.

## ***Configuration***

There are no jumpers or hardware settings on the board.

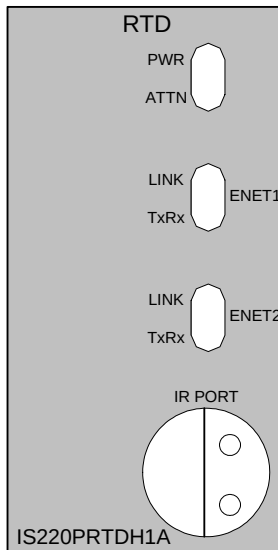
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## ***Notes***

# PRTD RTD Input

## PRTD RTD Input

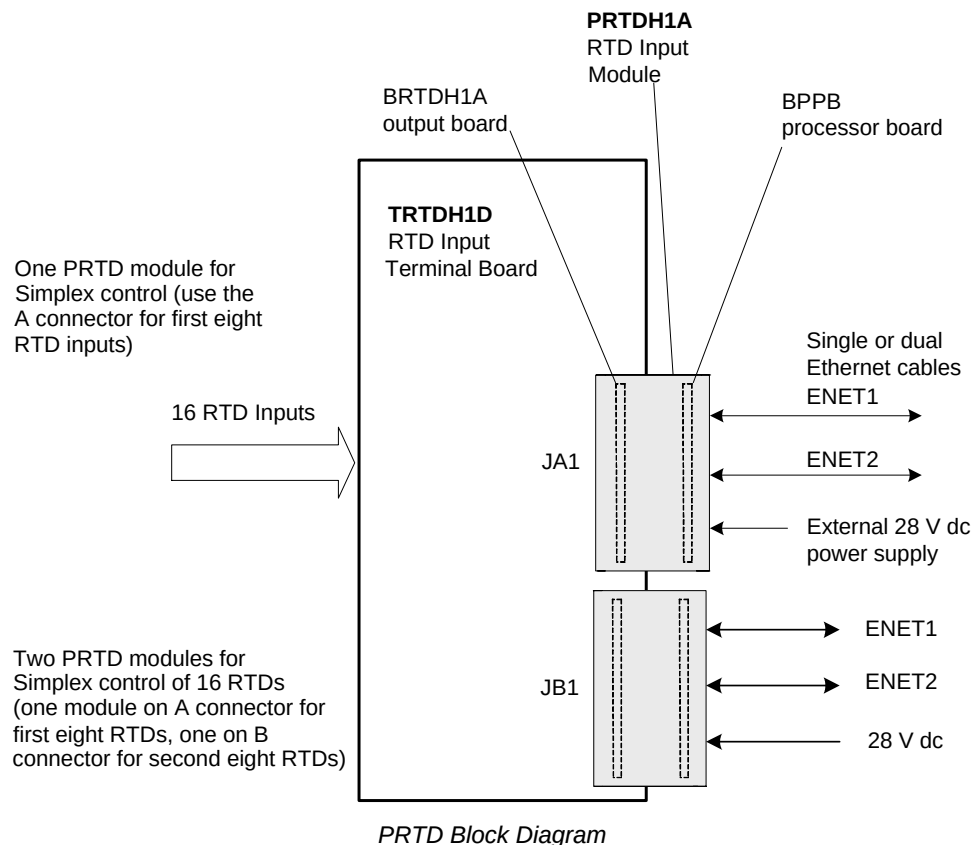
### Functional Description



The Resistance Temperature Device (RTD) Input (PRTD) pack provides the electrical interface between one or two I/O Ethernet networks and a RTD input terminal board. The pack contains a processor board common to all Mark\* VIE distributed I/O packs and an acquisition board specific to the thermocouple input function. The I/O pack is capable of handling up to eight RTD inputs and can handle 16 RTD inputs on the TRTD terminal boards.

**Note** The PRTD pack supports only simplex operation.

Input to the pack is through a DC-37 pin connector that connects directly with the associated terminal board connector, and a three-pin power input. Output is through dual RJ45 Ethernet connectors. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PRTDH1A is compatible with the RTD input terminal boards TRTDH1D, H2D, and the SRTD board, but not the DIN-rail mounted DRTD board. The following table gives details of the compatibility.

| Terminal Board     | TRTD                                   | SRTD          |
|--------------------|----------------------------------------|---------------|
| Version and Inputs | TRTDH1D, H2D                           | 8 RTD         |
| Control mode       | Simplex - Yes    Dual - No    TMR - No | Simplex - Yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

The PRTD provides galvanic isolation of the TRD input circuit. This requires changes in the terminal board transient protection, provided on the TRTDH1D and TRTDH2D boards. The H1D version of the board provides filtering compatible with the standard scan rate of PRTD. The H2D version of the terminal board provides less filtering to allow proper performance when the fast scan rate of PRTD is selected. If PRTD is mounted on an earlier revision of the TRTD board, an incompatibility will be reported, although no physical damage will occur.

## Installation

### ➤ To install the PRTD pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one or two PRTD (for simplex control of eight or 16 RTDs) into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded inserts adjacent to the Ethernet ports. The inserts connect with a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-37 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two cables (depending on system configuration) to negotiate proper operation over either port. If dual connections are used the standard practice is to hook ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

---

**Note** The PRTD mounts directly to a Mark VIe terminal board. Simplex terminal boards (TRTDH1C) have two DC-37 pin connectors that receive the PRTDs, one for each set of 8 RTD inputs. TMR capable terminal boards (TRTDH1B) have six DC-37 pin connectors, but supports only simplex control with one or two packs.

---

# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## ***Analog Input Hardware***

The PRTD input board accepts eight three-wire RTD inputs from the RTD terminal board.

The pack supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The eight RTDs can be located up to 300 meters (984 feet) from the turbine I/O cabinet with a maximum two-way cable resistance of 15  $\Omega$ .

The A/D converter in the pack samples each signal and the excitation current four times per second for normal mode scanning, and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Linearization for the selection of RTD types is performed in software by the processor. RTD open and short circuits are detected by out of range values. An RTD, which is determined to be out of hardware limits, is removed from the scanned inputs in order to prevent adverse affects on other input channels. Repaired channels are reinstated automatically in 20 seconds, or can be manually reinstated.

## ***Calibration***

RTD inputs are automatically calibrated using the filtered calibration source and null voltages.

## ***ID Line***

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## ***Power Management***

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.



## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Connectors

The pack contains the following connectors:

- A DC-37 pin connector on the underside of the I/O pack connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the side of the pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

## Specifications

The following table provides information specific to the PRTD pack.

| Item                     | PRTD Specification                                   |             |                    |
|--------------------------|------------------------------------------------------|-------------|--------------------|
| Number of channels       | 8 channels per pack (16 channels per terminal board) |             |                    |
| RTD types                | 10, 100, and 200 $\Omega$ platinum                   |             |                    |
|                          | 10 $\Omega$ copper                                   |             |                    |
|                          | 120 $\Omega$ nickel                                  |             |                    |
| Span                     | 0.3532 to 4.054 V                                    |             |                    |
| A/D converter resolution | 14-bit resolution                                    |             |                    |
| Scan time                | Normal scan 250 ms (4 Hz)                            |             |                    |
|                          | Fast scan 40 ms (25 Hz)                              |             |                    |
| Measurement accuracy     | RTD Type                                             | Group Gain  | Accuracy at 400 °F |
|                          | 120 $\Omega$ Nickel                                  | Normal_ 1.0 | 2 °F               |

| Item                      | PRTD Specification                                                                 |                   |       |
|---------------------------|------------------------------------------------------------------------------------|-------------------|-------|
|                           | 200 $\Omega$ Platinum                                                              | Normal_1.0        | 2 °F  |
|                           | 100 $\Omega$ Platinum                                                              | Normal_1.0        | 4 °F  |
|                           | 100 $\Omega$ Platinum -51 to +204°C<br>(-60 °F to 400 °F)                          | Gain_2.0          | 2 °F  |
|                           | 10 $\Omega$ Copper                                                                 | 10 $\Omega$ Cu_10 | 10 °F |
| Common mode rejection     | Ac common mode rejection 60 dB @ 50/60 Hz,<br>Dc common mode rejection 80 dB       |                   |       |
| Common mode voltage range | $\pm 5$ Volts                                                                      |                   |       |
| Normal mode rejection     | Rejection of up to 250 mV Rms is 60 dB @ 50/60 Hz system frequency for normal scan |                   |       |
| Maximum lead resistance   | 15 $\Omega$ maximum two-way cable resistance                                       |                   |       |

### ***RTD Types and Ranges***

RTD inputs are supported over a full-scale input range of 0.3532 to 4.054 V. The following table shows the types of RTD used and the temperature ranges.

| RTD Type              | Name/Standard                  | Range °C    | Range °F     |
|-----------------------|--------------------------------|-------------|--------------|
| 10 $\Omega$ copper    | MINCO_CA GE 10 $\Omega$ Copper | -51 to +260 | -60 to +500  |
| 100 $\Omega$ platinum | SAMA 100                       | -51 to +593 | -60 to +1100 |
| 100 $\Omega$ platinum | DIN 43760                      | -51 to +700 | -60 to +1292 |
|                       | IEC-751                        |             |              |
|                       | MINCO_PD                       |             |              |
|                       | MINCO_PE                       |             |              |
|                       | PT100_DIN                      |             |              |
| 100 $\Omega$ platinum | MINCO_PA                       | -51 to +700 | -60 to +1292 |
|                       | IPTS-68                        |             |              |
|                       | PT100_PURE                     |             |              |
| 100 $\Omega$ platinum | MINCO_PB                       | -51 to +700 | -60 to +1292 |
|                       | Rosemount 104                  |             |              |
|                       | PT100_USIND                    |             |              |
| 120 $\Omega$ nickel   | MINCO_NA                       | -51 to +249 | -60 to +480  |
|                       | N 120                          |             |              |
| 200 $\Omega$ platinum | PT 200                         | -51 to +204 | -60 to +400  |

## ***Diagnostics***

The pack performs the following self-diagnostic tests

- A power-up self-test that includes checks of RAM, Flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each RTD type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set, and the input is no longer scanned. If any one of the 8 input's hardware limits is set it creates a composite diagnostic alarm, L3DIAG\_PRTD, referring to the entire board. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal
- Each RTD input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limit signals
- Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter              | Description                                                                                                                                          | Choices                                                                                                                                                      |
|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>PRTD_Mod_Config</b> |                                                                                                                                                      |                                                                                                                                                              |
| System Limits          | Enable or disable all system limit checking                                                                                                          | Enable, disable                                                                                                                                              |
| Auto Reset             | Automatic restoring of RTDs removed from scan                                                                                                        | Enable, disable                                                                                                                                              |
| GroupRate              | Group A => RTD's 1-8 sample rate and n+ system frequency filter if 0 Hz sampling                                                                     | 4 Hz, 50 Hz filter<br>4 Hz, 60 Hz filter<br>25 Hz                                                                                                            |
| <b>PRTD_Pnt_Cfg</b>    |                                                                                                                                                      |                                                                                                                                                              |
| Group B Rate           | Sampling rate and system frequency filter for second group of eight inputs                                                                           | 4 Hz, 50 Hz filter<br>4 Hz, 60 Hz filter<br>25 Hz                                                                                                            |
| Group B Gain           | Gain 2.0 is for higher accuracy if ohms<190, second group of eight inputs                                                                            | Normal_1.0<br>Gain_2.0<br>10 $\Omega$ Cu_10.0                                                                                                                |
|                        | First of 16 RTDs - card point signal                                                                                                                 | Point Edit (Input FLOAT)                                                                                                                                     |
| <b>SwConfigDefs</b>    |                                                                                                                                                      |                                                                                                                                                              |
| RTD Type               | Select RTD type or ohms input<br>RTDs linearizations supported by RTD, (unused inputs are removed from scanning)                                     | Unused<br>CU10 MINCO_CA<br>PT100_DIN MINCO_PD<br>PT100_PURE MINCO_PA<br>PT100_USIND MINCO_PB<br>N120 MINCO_NA<br>MINCO_PIA PT100_SAMA<br>PT200 MINCO_PK Ohms |
| SysLim1 Enabl          | Enable system limit 1 fault check<br>Enables or disables a temperature limit for each RTD, can be used to create an alarm                            | Enable, disable                                                                                                                                              |
| SysLim1 Latch          | Latch system limit 1 fault<br>Determines whether the limit condition will latch or unlatch for each RTD; reset used to unlatch.                      | Latch, unlatch                                                                                                                                               |
| SysLim1 Type           | System limit 1 check type ( >= or <= )<br>Limit occurs when the temperature is greater than or equal (>=), or less than or equal to a preset value.  | Greater than or equal,<br>Less than or equal                                                                                                                 |
| System Limit 1         | System limit 1 - Deg F or ohms.<br>Enter the desired value of the limit temperature                                                                  | -60 to 1,300                                                                                                                                                 |
| SysLim2 Enabled        | Enable system limit 2 fault check<br>Enables or disables a temperature limit used to create an alarm                                                 | Enable, disable                                                                                                                                              |
| SysLim2 Latch          | Latch system limit 2 fault<br>Determines whether the limit condition will latch or unlatch; reset used to unlatch.                                   | Latch, unlatch                                                                                                                                               |
| SysLim2 Type           | System limit 2 check type ( >= or <= ).<br>Limit occurs when the temperature is greater than or equal (>=), or less than or equal to a preset value. | Greater than or equal,<br>Less than or equal                                                                                                                 |

| Parameter      | Description                                                                                                                                                                             | Choices                                       |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|
| System Limit 2 | System limit 2 - Deg F or ohms.<br>Enter the desired value of the limit temperature, Deg F or ohms                                                                                      | -60 to 1,300                                  |
| RTDGain        | Select RTD sensor gain.<br>Gain 2.0 is for higher accuracy if ohms<190.                                                                                                                 | Normal_1.0<br>Gain_2.0<br>10 $\Omega$ Cu_10.0 |
| TMR_DiffLimt   | Diag limit, TMR input vote difference, in eng units<br>Limit condition occurs if three temperatures in R,S,T differ by more than a preset value; this creates a voting alarm condition. | -60 to 1,300                                  |

| Point Signal | Description-Point Edit (Enter Signal Connection) | Direction | Type  |
|--------------|--------------------------------------------------|-----------|-------|
| L3DIAG_PRTD  | I/O diagnostic indication                        | Input     | BIT   |
| LINK_OK_PRTD | I/O link okay indication                         | Input     | BIT   |
| ATTN_PRTD    | I/O attention indication                         | Input     | BIT   |
| IOPackTmp    | I/O pack temperature                             | Input     | FLOAT |
| SysLim1RTD1  | System limit 1                                   | Input     | BIT   |
| :            | :                                                | Input     | BIT   |
| SysLim1RTD8  | System limit 1                                   | Input     | BIT   |
| SysLim2RTD1  | System limit 2                                   | Input     | BIT   |
| :            | :                                                | Input     | BIT   |
| SysLim2RTD8  | System limit 2                                   | Input     | BIT   |

## Alarms

### PRTD Specific Alarms

| Alarm ID | Alarm Description                            | Possible Cause                                                                                                                                   | Solution                                                                                             |
|----------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| 32-39    | RTD [ ] High Voltage Rdg, Counts are [ ]     | An RTD wiring/cabling open, or an open on the PRTD board, or a PRTD hardware problem (such as multiplexer), or the RTD device has failed.        | Check the field wiring and verify connections.<br>Check RTD for proper operation.<br>Replace IOPack. |
| 48-55    | RTD [ ] Low Voltage Rdg, Counts are [ ]      | An RTD wiring/cabling short, or a short on the PRTD board, or a PRTD hardware problem (such as multiplexer), or the RTD device has failed.       | Check the field wiring and verify connections.<br>Check RTD for proper operation.<br>Replace IOPack. |
| 64-71    | RTD [ ] High Current Rdg, Counts are [ ]     | The current source on the PRTD is bad, or the measurement device has failed.                                                                     | Replace IOPack.                                                                                      |
| 80-87    | RTD [ ] Low Current Rdg, Counts are [ ]      | An RTD wiring/cabling open, or an open on the PRTD board, or a PRTD hardware problem (such as multiplexer), or the RTD device has failed.        | Check the field wiring and verify connections.<br>Check RTD for proper operation.<br>Replace IOPack. |
| 96-103   | RTD [ ] Resistance Calc High, it is [ ] Ohms | The wrong type of RTD has been configured or selected by default, or there are high resistance values created by high voltage and/or low current | Verify that RTD type configuration matches the attached device type.                                 |
| 112-119  | RTD [ ] Resistance Calc Low, it is [ ] Ohms  | The wrong type of RTD has been configured or selected by default, or there are low resistance values created by low voltage and/or high current. | Verify that RTD type configuration matches the attached device type.                                 |

| Alarm ID | Alarm Description                                  | Possible Cause                                                                                                                                             | Solution        |
|----------|----------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| 128      | Voltage Ckt for RTD's 1-4 Has Ref Raw Counts High  | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 129      | Volatge Ckt for RTD's 1-4 Has Ref Raw Counts Low   | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 130      | Voltage Ckt for RTD's 5-8 Has Ref Raw Counts High  | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 131      | Voltage Ckt for RTD's 5-8 Has Ref Raw Counts Low   | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 136      | Voltage Ckt for RTD's 1-4 Has Null Raw Counts High | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 137      | Voltage Ckt for RTD's 1-4 Has Null Raw Counts Low  | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 138      | Voltage Ckt for RTD's 5-8 Has Null Raw Counts High | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 139      | Voltage Ckt for RTD's 5-8 Has Null Raw Counts Low  | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 144      | Current Ckt for RTD's 1-8 Has Ref Raw Counts High  | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 145      | Current Ckt for RTD's 1-8 Has Ref Raw Counts Low   | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 146      | Current Ckt for RTD's 1-8 Has Null Raw Counts High | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |
| 147      | Current Ckt for RTD's 1-8 Has Null Raw Counts Low  | Internal PRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged. | Replace IOPack. |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

## **TRTD RTD Input**

### **Functional Description**

The RTD Input (TRTD) terminal board accepts 16, three-wire RTD inputs. These inputs are wired to two barrier type terminal blocks. The inputs have noise suppression circuitry to protect against surge and high frequency noise. TRTD communicates with one or more I/O processors, which convert the inputs to digital temperature values and transfer them to the controller.

There are four versions of TRTD as follows:

- TRTDH1B is a TMR version that fans out the signals to three VRTD boards using six DC-type connectors.
- TRTDH1C is a simplex board with two DC-type connectors for VRTD.
- TRTDH1D is a simplex board with two DC-type connectors for PRTD, normal scan.
- TRTDH2D is a simplex board with two DC-type connectors for PRTD, fast scan.

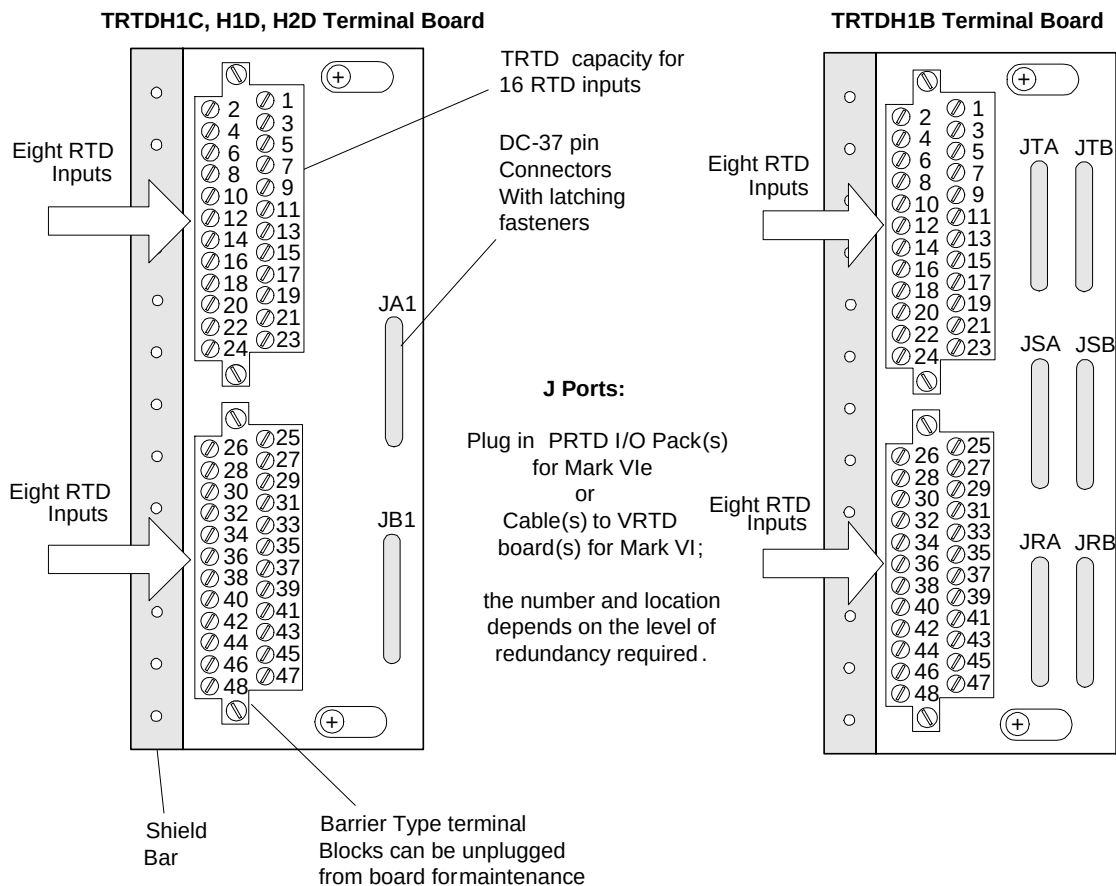
### **Mark VI Systems**

In the Mark\* VI system, TRTDH1B and TRTDH1C works with the VRTD processor and supports simplex and TMR applications. One TRTDH1C connects to the VRTD with two cables. In TMR systems, TRTDH1B connects to three VRTD processors with six cables.

### **Mark VIe Systems**

In the Mark VIe system, TRTDH1D and TRTDH2D works with the PRTD I/O pack and support simplex applications only. Two PRTD packs plug into the TRTD for a total of 16 inputs.





*RTD Input Terminal Boards*

## Installation

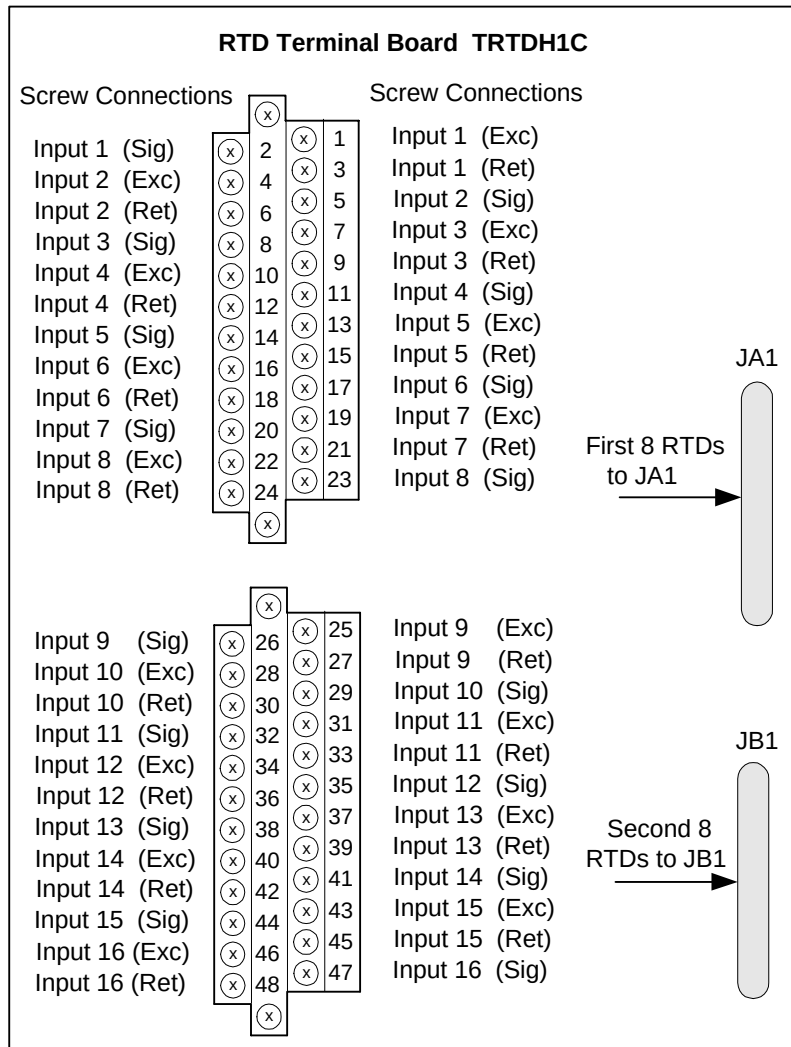
Connect the wires for the 16 RTDs directly to the two terminal blocks on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.



### Caution

**For CE mark applications, double-shielded wire must be used. All shields must be terminated at the shield terminal strip. Do not terminate shields located at the end device.**

In a TMR Mark VI system, TRTDH1B provides redundant RTD inputs by fanning the inputs to three VRTD boards in the R, S, and T racks. The inputs meet the same environmental, resolution, suppression, and function requirements and codes as the TRTDH1C terminal board; however, the fast scan is not available.



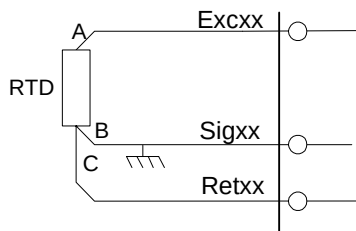
#### J-Port Connections

Plug in PRTD I/O Pack(s) for Mark VIe

or

Cable to VRTD I/O board(s) for Mark VI;

The number and location depends on the number of inputs required.



#### Application Note:

- Optional Ground: connect the B wire to ground;
- RTD Group wiring, that is sharing the B wire; tie the B wires together at the RTDs, tie the Sigxx signals together at the TRTD terminal board, and interconnect with one wire.

TRTDH1C RTD Terminal Board Wiring

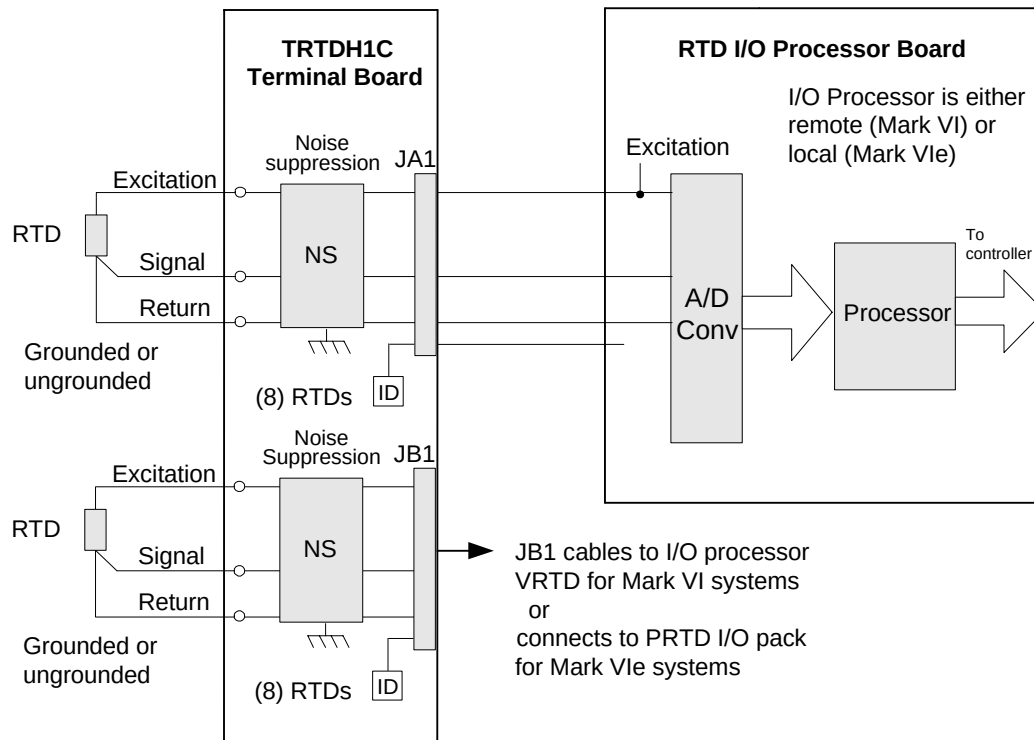
## Operation

TRTD supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The 16 RTDs can be located up to 300 m (984 ft) from the turbine control cabinet with a maximum two-way cable resistance of 15  $\Omega$ .

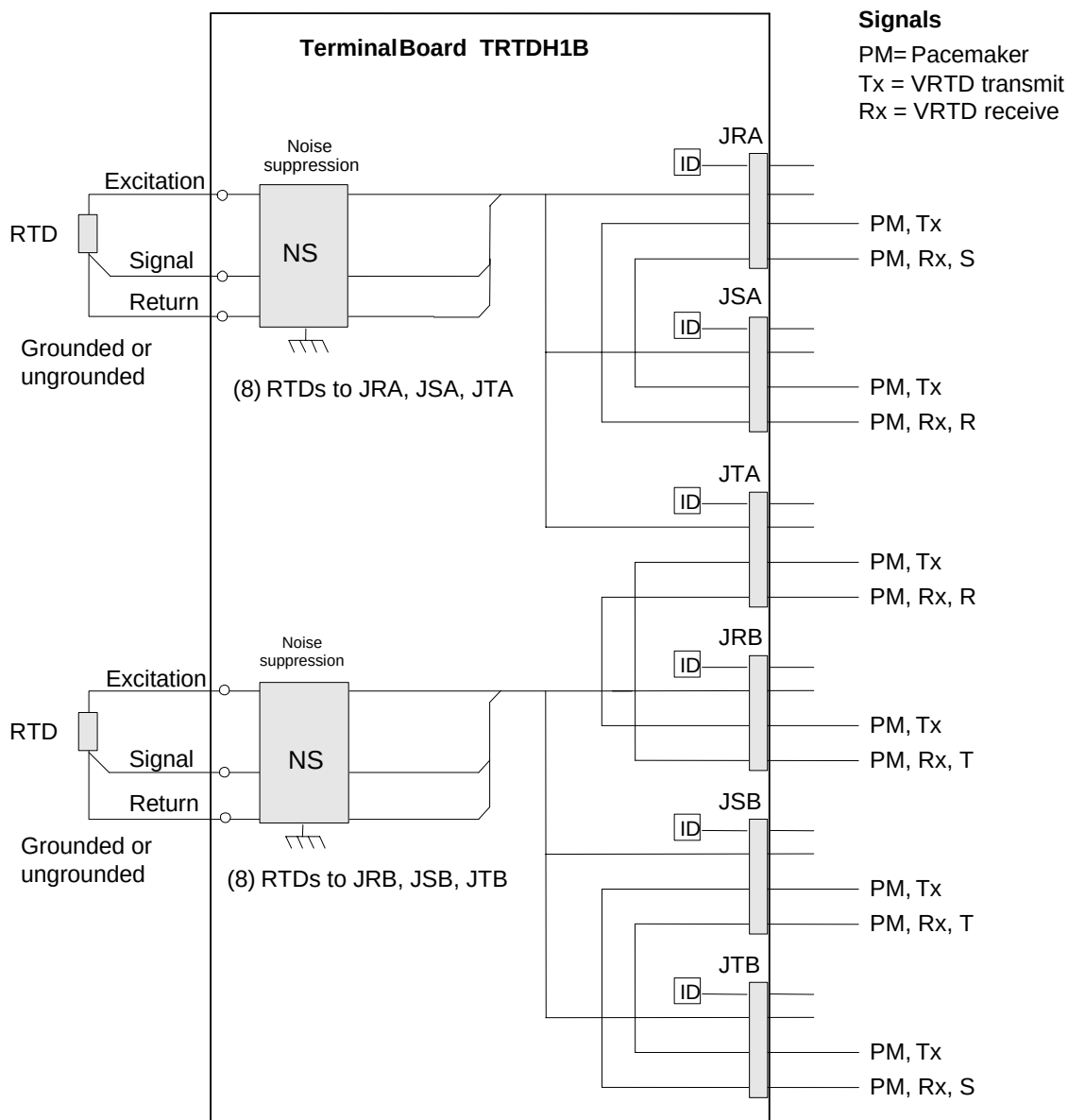
The A/D converter in the I/O processor samples each signal and the excitation current four times per second for normal mode scanning and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Software performs the linearization for the selection of 15 RTD types.

RTD open and short circuits are detected by out-of-range values. An RTD that is determined to be outside the hardware limits is removed from the scanned inputs to prevent adverse effects on other input channels. Repaired channels are reinstated automatically in 20 seconds or can be manually reinstated.

All RTD signals have high-frequency decoupling to ground at signal entry. RTD multiplexing in the I/O processor is coordinated by redundant pacemakers so that the loss of a single cable or I/O processor does not cause the loss of any RTD signals in the control database.



*TRTD (Simplex) Inputs and Signal Processing*



TRTDH1 TMR-Capable RTD Terminal Board

### Calibration

RTD inputs are automatically calibrated using the filtered calibration source and null voltages.

## **Specifications**

| <b>Item</b>             | <b>Specification</b>                                                                        |
|-------------------------|---------------------------------------------------------------------------------------------|
| Number of channels      | Eight channels per terminal board                                                           |
| RTD types               | 10, 100, and 200 $\Omega$ platinum<br>10 $\Omega$ copper<br>120 $\Omega$ nickel             |
| Span                    | 0.3532 to 4.054 V                                                                           |
| Maximum lead resistance | 15 $\Omega$ maximum two-way cable resistance                                                |
| Fault detection         | High/low (hardware) limit check<br>High/low (software) system limit check<br>Failed ID chip |

### **RTD Accuracy**

| <b>RTD Type</b>                                        | <b>Group Gain</b>   | <b>Accuracy at 400 °F</b> |
|--------------------------------------------------------|---------------------|---------------------------|
| 120 $\Omega$ nickel                                    | 120 $\Omega$ nickel | 2 °F                      |
| 200 $\Omega$ platinum                                  | Normal_ 1.0         | 2 °F                      |
| 100 $\Omega$ platinum                                  | Normal_ 1.0         | 4 °F                      |
| 100 $\Omega$ platinum -51 to 240°C (- 60 °F to 400 °F) | Gain_ 2.0           | 2 °F                      |
| 10 $\Omega$ copper                                     | 10 $\Omega$ Cu_10   | 10 °F                     |

### **RTD Types and Ranges**

RTD inputs are supported over a full-scale input range of 0.3532 to 4.054 V. The following table shows the types of RTD used and the temperature ranges.

| <b>RTD Type</b>       | <b>Name/Standard</b>           | <b>Range °C</b> | <b>Range °F</b> |
|-----------------------|--------------------------------|-----------------|-----------------|
| 10 $\Omega$ copper    | MINCO_CA GE 10 $\Omega$ Copper | -51 to +260     | -60 to +500     |
| 100 $\Omega$ platinum | SAMA 100                       | -51 to +593     | -60 to +1100    |
| 100 $\Omega$ platinum | DIN 43760                      | -51 to +700     | -60 to +1292    |
|                       | IEC-751                        |                 |                 |
|                       | MINCO_PD                       |                 |                 |
|                       | MINCO_PE                       |                 |                 |
|                       | PT100_DIN                      |                 |                 |
| 100 $\Omega$ platinum | MINCO_PA                       | -51 to +700     | -60 to +1292    |
|                       | IPTS-68                        |                 |                 |
|                       | PT100_PURE                     |                 |                 |
| 100 $\Omega$ platinum | MINCO_PB                       | -51 to +700     | -60 to +1292    |
|                       | Rosemount 104                  |                 |                 |
|                       | PT100_USIND                    |                 |                 |
| 120 $\Omega$ nickel   | MINCO_NA                       | -51 to +249     | -60 to +480     |
|                       | N 120                          |                 |                 |
| 200 $\Omega$ platinum | PT 200                         | -51 to +204     | -60 to +400     |

## ***Diagnostics***

Diagnostic checks include the following:

- Each RTD type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the input's hardware limits is set, it creates a composite diagnostic alarm, L3DIAG\_XXXX, referring to the entire board. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal.
- Each RTD input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limit signals. In TMR systems, limit logic signals are voted and the resulting composite diagnostic is present in each controller.
- The resistance of each RTD is checked and compared with the correct value, and if high or low, a fault is created.
- Each connector has its own ID device, which is interrogated by the I/O processor board. The terminal board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the connector location. If a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no jumpers or hardware settings on the board.

---

# ***SRTD Simplex RTD Input***

## ***Functional Description***

The Simplex Resistance Temperature Device (RTD) Input (SRTD) terminal board is a compact RTD terminal board, designed for DIN-rail or flat mounting. The board has eight RTD inputs and connects to the PRTD I/O processor. High-density Euro-block type terminal blocks are mounted to the board. An on-board ID chip identifies the board to the I/O processor for system diagnostic purposes.

## ***Mark VIe Systems***

In the Mark\* VIe systems, the PRTD I/O pack works with the SRTD. The I/O pack plugs into the DC-37 pin connector and communicates with the controller over Ethernet. Only simplex systems are supported.

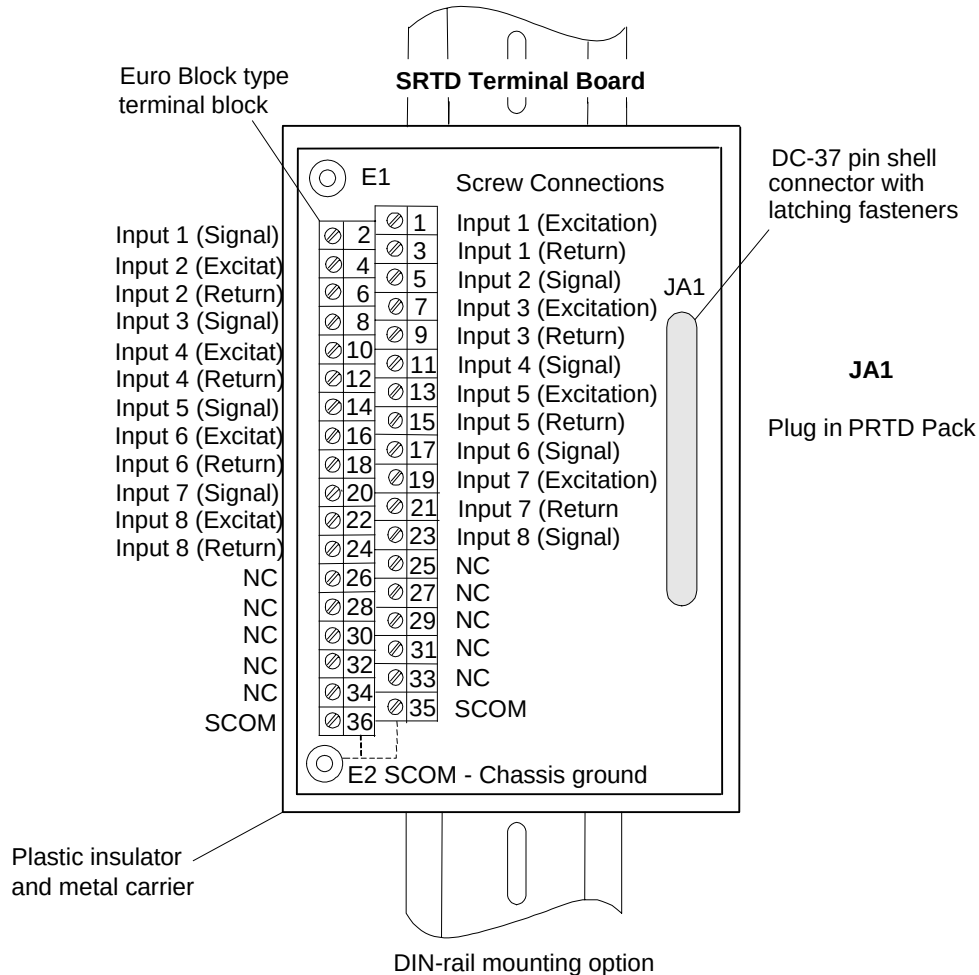
## ***Installation***

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**Note** There is no shield terminal strip with this design.

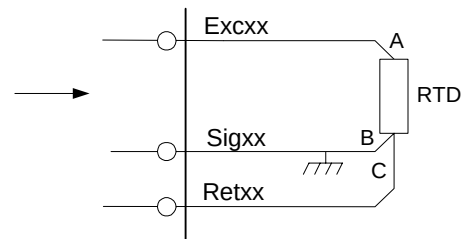
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The SRTD and a plastic insulator mount on a sheet metal carrier which, mounts on a DIN rail. Optionally the SRTD and insulator mount on a sheet metal assembly bolts directly in a cabinet. The eight RTDs are wired directly to the Euro-style box type terminal block, which has 36 terminals and is available in two types. Typically #18 AWG wires (shielded twisted triplet) are used. I/O cable shield terminal uses an external mounting bracket supplied by GE or the customer. Terminals 25 through 34 are not connected. E1 and E2 are mounting holes for the chassis ground screw connection (SCOM).



#### Application Notes:

- Optional Ground: connect the B wire to ground;
- RTD Group wiring, that is sharing the B wire; tie the B wires together at the RTDs, tie the Sigxx signals together at the RTD terminal board, and interconnect with one wire.



#### SRTD Terminal Board Wiring and Cabling

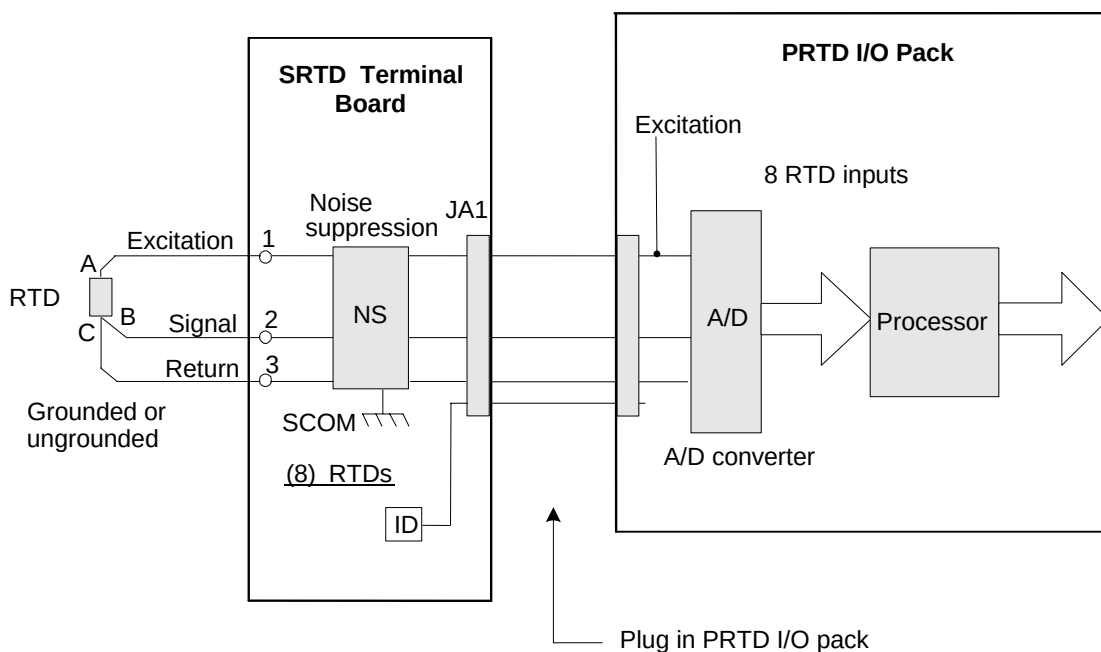
Two types of Euro-style box type terminal blocks are available:

- Terminal board SRTDH1 has a permanently mounted terminal block with 36 terminals.
- Terminal board SRTDH2 has a right-angle header accepting a range of commercially available pluggable terminal blocks, with a total of 36 terminals.

## Operation

The terminal board supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The eight RTDs can be located up to 300 m (984 ft) from the turbine control cabinet with a maximum two-way cable resistance of 15  $\Omega$ . The on-board noise suppression is similar to that on the TRTD. The RTD inputs and signal processing are illustrated in the figure.

The A/D converter in the PRTD pack samples each signal and the excitation current four times per second for normal mode scanning, and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Linearization for the selection of 15 RTD types is performed by the processor.



*SRTD Board and Input Processor Board*

RTD open and short circuits are detected by out-of-range values. An RTD that is determined to be out of hardware limits is removed from the scanned inputs to prevent adverse affects on other input channels. Repaired channels are reinstated automatically in 20 seconds, or can be manually reinstated.

## Calibration

RTD inputs are automatically calibrated using the filtered calibration source and null voltages.



## **Specifications**

| <b>Item</b>             | <b>Specification</b>                                                                           |
|-------------------------|------------------------------------------------------------------------------------------------|
| Number of channels      | Eight channels per terminal board                                                              |
| RTD types               | 10, 100, and 200 $\Omega$ platinum<br>10 $\Omega$ copper<br>120 $\Omega$ nickel                |
| Span                    | 0.3532 to 4.054 V                                                                              |
| Maximum lead resistance | 15 $\Omega$ maximum two-way cable resistance                                                   |
| Fault detection         | High/low (hardware) limit check<br>High/low (software) system limit check<br>Incorrect ID chip |

### **RTD Accuracy**

| <b>RTD Type</b>                                        | <b>Group Gain</b>   | <b>Accuracy at 400 °F</b> |
|--------------------------------------------------------|---------------------|---------------------------|
| 120 $\Omega$ nickel                                    | 120 $\Omega$ nickel | 2 °F                      |
| 200 $\Omega$ platinum                                  | Normal_ 1.0         | 2 °F                      |
| 100 $\Omega$ platinum                                  | Normal_ 1.0         | 4 °F                      |
| 100 $\Omega$ platinum -51 to 240°C (- 60 °F to 400 °F) | Gain_ 2.0           | 2 °F                      |
| 10 $\Omega$ copper                                     | 10 $\Omega$ Cu_10   | 10 °F                     |

### **RTD Types and Ranges**

RTD inputs are supported over a full-scale input range of 0.3532 to 4.054 V. The following table shows the types of RTD used and the temperature ranges.

| <b>RTD Type</b>       | <b>Name/Standard</b>           | <b>Range °C</b> | <b>Range °F</b> |
|-----------------------|--------------------------------|-----------------|-----------------|
| 10 $\Omega$ copper    | MINCO_CA GE 10 $\Omega$ Copper | -51 to +260     | -60 to +500     |
| 100 $\Omega$ platinum | SAMA 100                       | -51 to +593     | -60 to +1100    |
| 100 $\Omega$ platinum | DIN 43760                      | -51 to +700     | -60 to +1292    |
|                       | IEC-751                        |                 |                 |
|                       | MINCO_PD                       |                 |                 |
|                       | MINCO_PE                       |                 |                 |
|                       | PT100_DIN                      |                 |                 |
| 100 $\Omega$ platinum | MINCO_PA                       | -51 to +700     | -60 to +1292    |
|                       | IPTS-68                        |                 |                 |
|                       | PT100_PURE                     |                 |                 |
| 100 $\Omega$ platinum | MINCO_PB                       | -51 to +700     | -60 to +1292    |
|                       | Rosemount 104                  |                 |                 |
|                       | PT100_USIND                    |                 |                 |
| 120 $\Omega$ nickel   | MINCO_NA                       | -51 to +249     | -60 to +480     |
|                       | N 120                          |                 |                 |
| 200 $\Omega$ platinum | PT 200                         | -51 to +204     | -60 to +400     |

## ***Diagnostics***

Diagnostic checks include the following:

- Each RTD type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the input's hardware limits is set, it creates a composite diagnostic alarm, L3DIAG\_xxxx, referring to the entire board. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal.
- Each RTD input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limit signals. In TMR systems, limit logic signals are voted and the resulting composite diagnostic is present in each controller.
- The resistance of each RTD is checked and compared with the correct value, and if high or low, a fault is created.
- Each connector has its own ID device, which is interrogated by the I/O processor board. The terminal board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the connector location. If a mismatch is encountered, a hardware incompatibility fault is created.

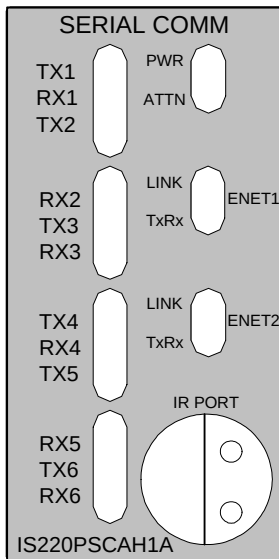
## ***Configuration***

There are no jumpers or hardware settings on the board.

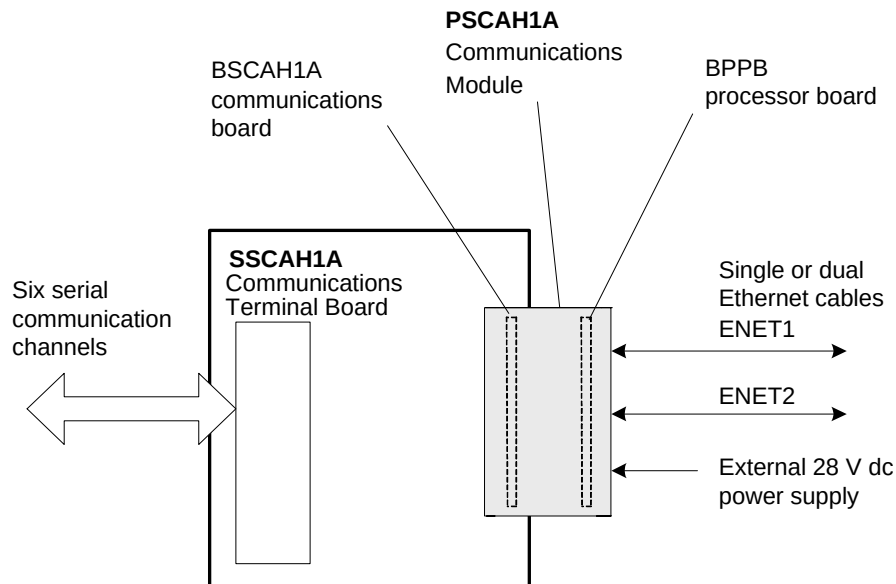
# PSCA Serial Communication Input/Output

## PSCA Serial Communication Input/Output

### Functional Description



The Serial Communication Input/Output (PSCA) pack provides the electrical interface between one or two I/O Ethernet networks and a serial communications terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs and a serial communications board. The communications board contains six serial transceiver channels, each of which can be individually configured to comply with RS-232, RS-422, or RS-485 half duplex standards. Input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. One of the Ethernet ports can be used to support Ethernet Modbus communication on Simplex Networks. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PSCAH1A is compatible with the SSCAH1A terminal board, but not the DIN-rail mounted DSCB board. The following table gives details of the compatibility:

| Terminal Board | DSCB | SSCAH1A     |
|----------------|------|-------------|
| Control mode   | No   | Simplex=yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

## Installation

### ➤ To install the PSCA pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PSCA pack into the terminal board connector.
- 3 Mechanically secure the packs using the threaded inserts adjacent to the Ethernet ports. The inserts connect with a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack operates over either port. If dual connections are used, standard practice is to hook ENET1 to the network associated with the R controller, however, the PSCA is not sensitive to Ethernet connections and will negotiate proper operation over either port.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

---

**Note** The PSCA mounts directly to a Mark VIe SSCA terminal board. The simplex terminal board has a single DC-62 pin connector that receives the PSCA.

---

# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## Serial Channels

The BSCA board in the pack contains six independently configurable serial channels. The processor board configures the channels with one of three mode inputs as follows:

| Mode | Transceiver                     |
|------|---------------------------------|
| 0    | RS-232                          |
| 1    | RS-422                          |
| 2    | RS-485 half duplex only         |
| 3    | Default/reset state (fail safe) |

Jumpers on the SSCA terminal board are used to set up the terminal scheme for the selected communication mode.

### Data Flow from PSCA to Controller

Data flow from PSCA to the Mark VIe controller is of two types, fixed I/O and Modbus I/O. Fixed I/O is associated with the smart pressure transducers and the Kollmorgen<sup>®</sup> electric drive data. This data is completely processed every frame, the same as conventional I/O. The required frame rate is 100 Hz. These signals are mapped into signal space, using the .tre file, and have individual health bits, use system limit checking, and have offset/gain scaling.

Modbus I/O is the I/O associated with the Modbus ports. Because of the quantity of these signals, they are not completely processed every frame; instead they are packaged and transferred to the Mark VIe Controller, over the IONet through a special service. This can accommodate up to 2400 bytes, at 4 Hz, or 9600 bytes at 1 Hz, or combinations thereof. This I/O is known as second class I/O, where coherency is at the signal level only, not at the device or board level. Health bits are assigned at the device level, the Mark VIe Controller expands (fully populate) for all signals, and system limit checking is not performed. Two consecutive time outs are required before a signal is declared unhealthy. Diagnostic messages are used to annunciate all communication problems.

**Honeywell<sup>®</sup> Pressure Transducers:** Serial ports 1 and 2 support the Honeywell pressure configuration. It reads inputs from the Honeywell Smart Pressure Transducers, type LG-1237. As an option (pressure transducers or Modbus) this service is available only on ports 1 and 2. The pressure transducer protocol utilizes interface board DS200XDSAG#AC, and RS-422. Each port can service up to six transducers. The service is 375 kbaud, asynchronous, nine data bits, (11 bits including start and stop). It includes communication miss counters, one per device, and associated diagnostics as failsafe features.

After four consecutive misses, it forces the input pressure to 1.0 psi, and posts a diagnostic. After four consecutive hits (good values) it removes the forcing and the diagnostic.

**Kollmorgen Electric Drive:** Three ports (any three, but no more than three) support the Kollmorgen electric drive. It communicates with a Kollmorgen Electric Fast Drive FD170/8R2-004 at a 19200 baud rate, point-to-point, using RS-422.

**Serial Modbus Master Service:** The current Modbus design supports the Master mode on all six serial ports, however the design does not preclude the future enhancement of Modbus slave mode of operation. It is configurable at the port level as follows:

- Physical connection: RS-232, RS-422, RS-485
- Baud Rate. 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115000
- Parity: none, odd, even
- Data Bits: seven, eight
- Stop Bits: one, two
- Station addresses
- Multidrop, up to eight devices per port; maximum of 18 devices per board
- RTU
- Time-out (seconds) per device
- 32-bit data format, i.e. byte format
- Device response delay time

The Modbus service is configurable at the signal level as follows:

- Signal type
- Register number
- Read/write
- Transfer rate, 0.5, 1, 2, or 4 Hz
- Scaling, offset, and gain

The service supports function codes 1-7, 15, and 16; it also supports double 16-bit registers for floating point numbers and 32-bit counters. It periodically (20s) attempts to reestablish communications with a dead station.

Type casting and scaling of all I/O signals to/from engineering units are supported on the PSCA and the toolbox, for both fixed I/O and Modbus I/O.

**Ethernet Modbus Master Service:** The PSCA can use one of its two Ethernet ports to support the Ethernet Modbus Master Protocol. This configuration can only be used with a simplex network. The Ethernet IP address for Modbus can not be included in the range of the IONET submask range. All Ethernet Modbus stations are configured on Port 7 through the ToolboxST\* application. The Ethernet Modbus implementation follows the Open Modbus/TCP Specification for a Class 1 device.

The ToolboxST application will allow up to 18 Ethernet Modbus stations to be attached to the PSCA. The CPU loading for each station varies depending on the number of Modbus registers being requested and the update rate. Also, the field device connect and data response rate may vary. Data throughput should be validated in system test when multiple stations and/or large amounts of data are being transferred

The following parameters are defined for all stations on the PSCA Ethernet port,

- TCP/IP Address for the PSCA Ethernet port
- TCP/IP Subnet mask
- TCP/IP Gateway IP address of intermediate router. (optional)

The next set of parameters are defined for each field device station

- Field Device TCP/IP address
- Field Device TCP/IP port (Modbus default is 502)
- Modbus Station Address (optional)
- TCP/IP connection timeout (TCP/IP default is 75 seconds)
- TCP/IP read/write timeout
- 32-bit data format i.e. byte order
- Open Modbus/TCP IP protocol

The Modbus service is configurable at the signal level as follows:

- Signal type
- Register number
- Read/write
- Transfer rate, 0.5, 1, 2, or 4 Hz
- Scaling, offset, and gain

The service supports function codes 1-7, 15, and 16. It also supports double 16-bit registers for floating point numbers and 32-bit counters. It periodically (20s) attempts to re-establish communications with a dead station.

Type casting and scaling of all I/O signals to/from engineering units are supported on the PSCA and the ToolboxST application, for both fixed I/O and Modbus I/O.

### ***ID Line***

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-62 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

### ***Power Management***

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.



## Status LEDs

Each serial channel has two indicator LEDs. The TX LED flashes when PEFV transmits from a port.

The RX LED flashes when a port is receiving data.

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly (¼ cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed (¾ cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Connectors

- A DC-62 pin connector on the underside of the I/O pack connects directly to a discrete output terminal board.
- An RJ45 Ethernet connector named ENET1 on the pack side is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the pack side is the redundant or secondary system interface.

---

**Note** The terminal board provides fused power output from a power source that is applied directly to the terminal board, not through this pack connector.

---

## Specifications

The following table provides information specific to the PSCA pack.

| Item                  | PSCA Specification                                                                              |
|-----------------------|-------------------------------------------------------------------------------------------------|
| Channels              | Six independently configurable serial channels<br>One Ethernet Modbus Channel (simplex network) |
| Communication choices | RS-232 Mode<br>RS-422 Mode<br>RS-485 Mode half duplex only<br>Ethernet Modbus Mode              |
| RS-232 Mode           | Cable distance: 50 ft<br>Communication Rate: 19,200 baud maximum                                |

| Item            | PSCA Specification                                                                     |
|-----------------|----------------------------------------------------------------------------------------|
| RS-422 Mode     | Cable distance: 1000 ft<br>Communication Rate: 375 Kbps maximum<br>Number of Drops: 8  |
| RS-485 Mode     | Cable distance: 1,000 ft<br>Communication Rate: 375 Kbps maximum<br>Number of drops: 8 |
| <b>Physical</b> |                                                                                        |
| Size            | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in. x 1.65 in. x 4.78 in.)            |
| Technology      | Surface-mount                                                                          |
| Temperature     | Operating: -30 to 65°C (-22 to +149 °F)                                                |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Analog inputs such as pressure and position have system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET\_SYS reset the out of limits

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Alarms

### PSCA Specific Alarms

| Alarm ID | Alarm Description                                                       | Possible Cause                                                          | Solution                                                                                                                                                                                                                              |
|----------|-------------------------------------------------------------------------|-------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32-67    | Port # {0:F0}<br>Device/Station # {1:F0}<br>No Response                 | A command was sent to a field device and no response was received       | Verify that the Serial or Ethernet cable is connected to the field device and that the device is power up and configured for the correct station ID. Make sure that the baud rate and parity are set correctly for serial connections |
| 72-107   | Port # {0:F0}<br>Device/Station # {1:F0}<br>Bad Data                    | The field device could not provide data for 1 or more registers         | Verify that the Modbus register definitions on the field device include the registers being request by the PSCA. Also verify that float values request all 32 bits of the value.                                                      |
| 108-113  | Configure Problem,<br>Port # {0:F0},<br>Communications<br>Nonfunctional | The configuration file downloaded from Toolbox ST contained an error.   | Verify that the IO and Configuration compatibility codes agree between the ToolboxST and the PSCA. Download Firmware and application code to the PSCA                                                                                 |
| 114-119  | Electric Drive, Port # {0:F0}, Save Command Nonfunctional               | The last parameter set saved to the Kollmorgen drive was not successful | The verify step failed after attempting to save parameters to the drive. Retry the save request.                                                                                                                                      |

| Alarm ID | Alarm Description                                                                               | Possible Cause                                                                                                                                                    | Solution                                                                                                                                              |
|----------|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 120-143  | Ethernet Configure Problem, Stn # {0:F0}, Communications Nonfunctional                          | The configuration file downloaded from Toolbox ST contained an error.                                                                                             | Verify that the IO and Configuration compatibility codes agree between the ToolboxST and the PSCA. Download Firmware and application code to the PSCA |
| 151-168  | The Ethernet Modbus field device could not provide data for 1 or more registers.                | Verify the Modbus register definitions on the field device include the registers being requested by the PSCA and float values request all 32 bits. (18 stations). |                                                                                                                                                       |
| 170-175  | The configuration file downloaded from ToolboxST application contained an error                 | Verify that the I/O and configuration compatibility codes agree between the ToolboxST application and the PSCA. (6 ports).                                        |                                                                                                                                                       |
| 176-193  | The Ethernet Modbus configuration file downloaded from ToolboxST application contained an error | Verify that the I/O and configuration compatibility codes agree between the ToolboxST application and the PSCA. (18 stations).                                    |                                                                                                                                                       |

### ***I/O Pack Alarms***

| Fault | Fault Description                                         | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                  | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                            | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                              | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                               | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                         | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state     | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                         | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                  | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                      | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                      | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash              | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                           | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code    | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch      | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                             | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]         | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                  | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                       | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]           | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]           | Not receiving EGD information from Controller                                                                                                              |

| <b>Fault</b> | <b>Fault Description</b>                                                    | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 273          | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                            |
| 274          | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                    |
| 275          | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                            |
| 276          | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                |
| 277          | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                |
| 278          | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                           |
| 293          | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                             |
| 301          | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                |
| 314          | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                           |
| 315          | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                             |
| 316          | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected         |
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ]             | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                                   | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated                           | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                             | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch                          | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                             | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                                    | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                                  | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                             | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                               | Config Shmem CRC changed                                                                |

## ***SSCA Simplex Serial Communication Input/Output***

### ***Functional Description***

The Simplex Serial Communication Input/Output (SSCA) terminal board is a compact serial communication terminal board that provides up to six communication channels. Each channel may be configured for RS-232C, RS-485, or RS-422 signaling. Only a simplex version of the board is available.

High-density Euro-style box type terminal blocks are used. An on-board ID chip identifies the board to the PSCA I/O pack for system diagnostic purposes.

### **Mark VIe Systems**

In the Mark\* VIe systems, the PSCA I/O pack works with the SSCA. The I/O pack plugs into the DC-37 pin connector and communicates with the controller over Ethernet. Only simplex systems are supported.

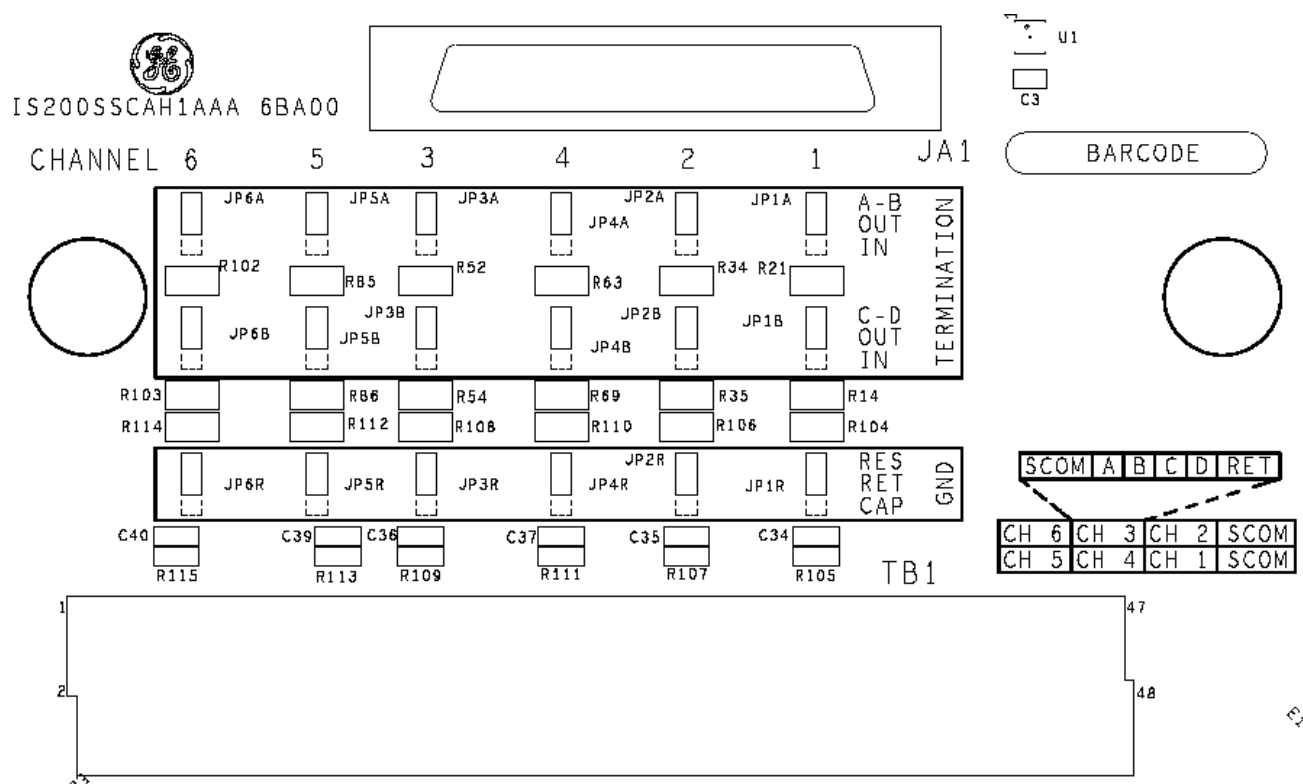
## Installation

The SSCA board is mounted on a DIN-rail using a sheet metal carrier and plastic insulator mount. This assembly will also bolt directly into a cabinet. There are two types of Euro-Block terminal blocks available:

- SSCAH1 has a permanently mounted terminal block with 48 terminals.
- SSCAH2 has a right-angle header accepting a range of commercially available pluggable terminal blocks, with 48 terminals.

**Note** There is no shield termination strip with this design.

Typically, SSCA uses #18 AWG (shielded twisted pair) wiring. The I/O cable shield termination is on an external mounting bracket supplied by the customer or by GE. The chassis ground connection uses E1 and E2 as mounting holes. One of the SCOM terminals (37-48) must be connected to a suitable shield ground.



SSCA Jumper Positions

## Operation

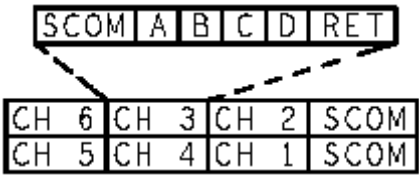
The SSCA terminal board includes six connection points for each of the six serial communication channels. The points include four signal lines A-D, a signal return, and a shield common (SCOM). The signal assignments are shown in the following table.

| Protocol | A       | B      | C             | D             | Notes                               |
|----------|---------|--------|---------------|---------------|-------------------------------------|
| RS-422   | TX+     | TX-    | RX+           | RX-           | Cable length up to 1000 ft.         |
| RS-485   | TX/RX+  | TX/RX- | Jumper from A | Jumper from B | Cable length up to 1000ft           |
| RS-232   | DTR/RTS | TX     | CTS           | RX            | Cable length up to 50 ft or 2500 pF |

Return for RS-232C is through the terminal called RET.

The signals for all six serial communication channels are arranged in the same order. Viewing into the box terminals, the signal order is SCOM, A, B, C, D, Ret viewed left to right.

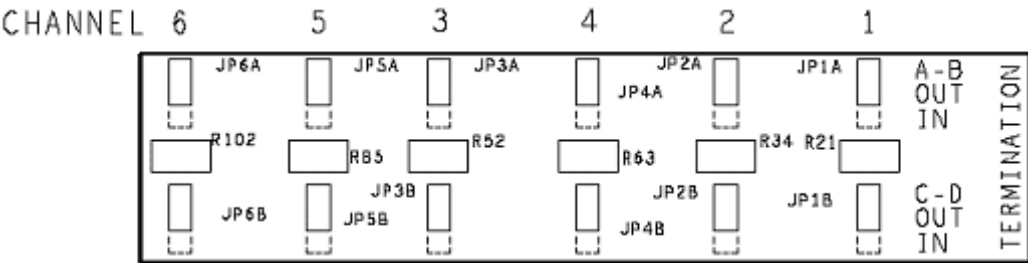
The groups of six signals for a serial channel are assigned to terminals adjacent to each other. Viewing the bottom set of terminals the channels are five, four, and one viewed left to right. The top set of terminals contain channels six, three, and two viewed left to right. The board SCOM connections are grouped on the right side of the terminals. A simple diagram is included on SSCA to aid in identifying signal locations.



The explicit terminal board screw connections are:

|           | SCOM | A  | B  | C  | D  | RET |
|-----------|------|----|----|----|----|-----|
| Channel 1 | 26   | 28 | 30 | 32 | 34 | 36  |
| Channel 2 | 25   | 27 | 29 | 31 | 33 | 35  |
| Channel 3 | 13   | 15 | 17 | 19 | 21 | 23  |
| Channel 4 | 14   | 16 | 18 | 20 | 22 | 24  |
| Channel 5 | 02   | 04 | 06 | 08 | 10 | 12  |
| Channel 6 | 01   | 03 | 05 | 07 | 09 | 11  |

When using RS-422 or RS-485, there is the need to provide a termination resistor at either end of a transmission line. SSCA provides selectable termination resistors for each pair of signal lines. Jumpers JP1A and JP1B apply or remove the termination resistors between signals A-B and C-D. The same function is repeated for each serial communication channel. The default jumper position is to disconnect the termination resistor. The SSCA is clearly marked to show the relationship of the termination jumpers and the serial communication channel signals.



In RS-232C systems, it is often not desirable to have a hard ground of the RET signal path on both ends of a cable. SSCA includes jumper selectable grounding options for each of the six RET lines. The line may be grounded through a 100 Ω resistor or through a 0.01 uF capacitor / 1M Ω resistor parallel combination. If the device attached to SSCA features a hard ground of the RET line then the capacitive ground should be selected on SSCA. If there is not a hard ground on the connected equipment then the resistive ground (default position) should be selected on SSCA.

RET ground jumpers are identified on SSCA as JP1R through JP6R. Positions are shown as RES and CAP for resistive and capacitive return connection. The jumpers are clearly labeled on the SSCA.



### Specifications

| Item                                      | Specification                                                                                                          |
|-------------------------------------------|------------------------------------------------------------------------------------------------------------------------|
| Number of channels                        | Six channels                                                                                                           |
| Termination resistors                     | Jumper selectable between open and resistor of 121 Ω, ½ W, 1%.                                                         |
| RS-232C return path ground                | Selectable between resistive ground of 100 Ω, ½ W, 1% or 1M Ω, ½ W, 1% in parallel with 0.01 uF, 500 V, 10% capacitor. |
| Maximum drops in RS-422 or RS-485 systems | Eight drops maximum                                                                                                    |
| Size                                      | 15.9 cm high x 10.2 cm wide (6.25 in. x 4.0 in.)                                                                       |
| Technology                                | Surface-mount                                                                                                          |
| Temperature                               | Operating: -30 to 65°C (-22 °F TO 149 °F)                                                                              |

### Diagnostics

Diagnostic tests are made on the terminal board components as follows:

The JA connector on the terminal board has its own ID device that is interrogated by the PSCA I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the J connector location. When this chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

### Configuration

Configuration of the terminal board is by means of jumpers. For location of these jumpers refer to the operation section. The jumper choices are as follows:

- Jumpers JP1A through JP6A apply or remove termination resistors between signal lines A and B for the six serial communication channels.
- Jumpers JP1B through JP6B apply or remove termination resistors between signal lines C and D for the six serial communication channels.
- Jumpers JP1R through JP6R select whether the return has a resistive or capacitive connection to SCOM.

All other configuration for the PSCA is done from the ToolboxST application. Electronic selection of the serial communications method, either RS-232, RS-422, or RS-485, is internal to the PSCA.

---

## ***DPWA Transducer Power Distribution***

### ***Functional Description***

The Transducer Power Distribution (DPWA) terminal board is a DIN-rail mounted power distribution board. It accepts input voltage of 28 V dc  $\pm 5\%$ , provided through a two-pin Mate-N-Lok<sup>®</sup> connector. Connectors are provided for two independent power sources to allow the use of redundant supplies. The input can accept power from a floating isolated voltage source. The input to DPWA includes two 1 k $\Omega$  resistors from positive and negative input power to SCOM. These center a floating power source on SCOM. Attenuated input voltage is provided for external monitoring. Output power of 12 V dc  $\pm 5\%$  is connected to external devices through a Euro- type terminal block, using screw terminals and AWG#18 twisted-pair wiring. DPWA provides three output terminal pairs with a total output rated at 0 to 1.2 A. The outputs are compatible with the XDSAG#AC interface board. Outputs are short circuit-protected and self-recovering.

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**Note** DPWA provides excitation power to LG-1237 Honeywell pressure transducers.

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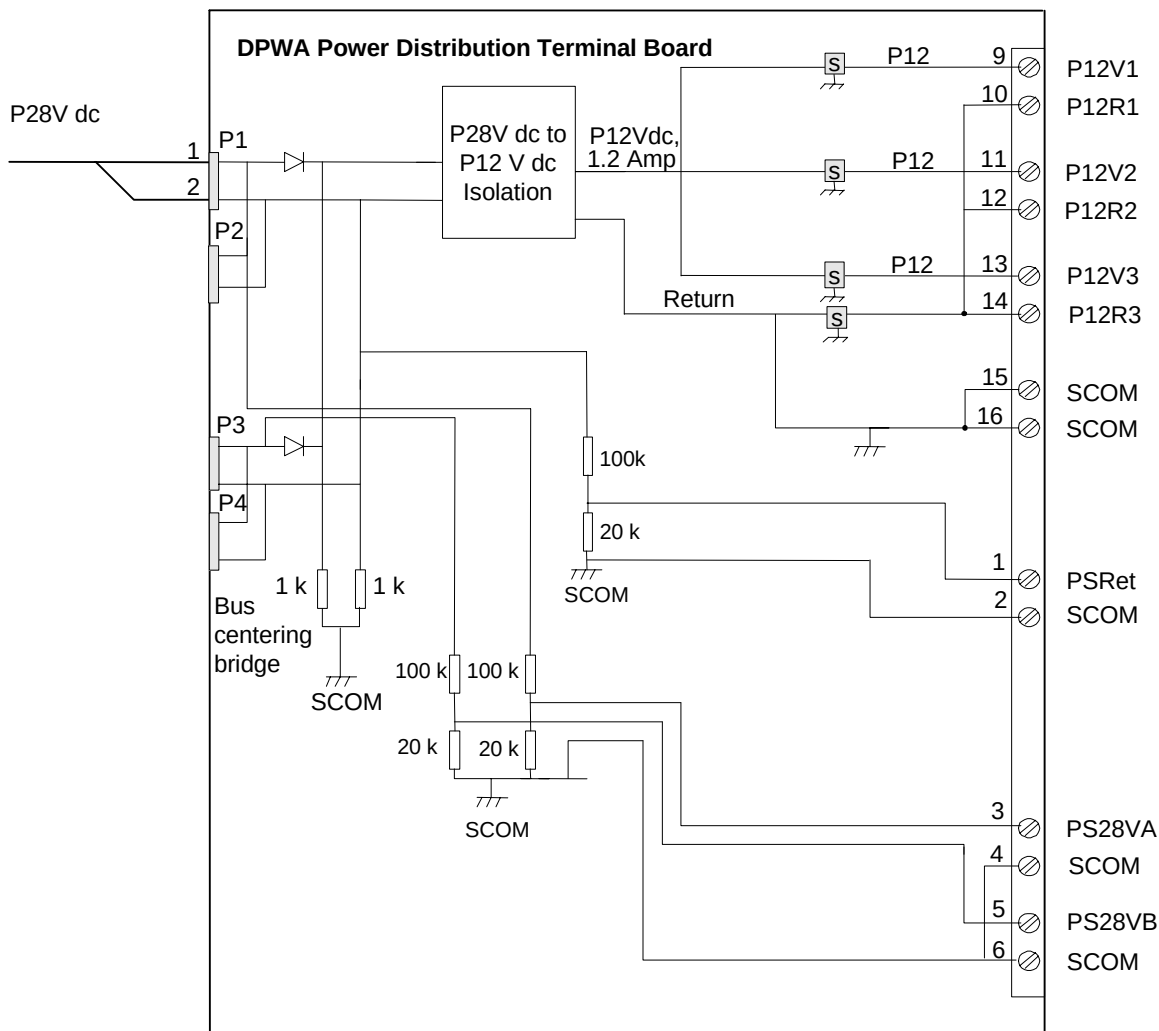


## Installation

Mount the DPWA assembly on a standard DIN-rail. Connect input power to connector P1. If multiple DPWA boards are used, use connector P2 as a pass-through connection point for the power to additional boards. If a redundant power input is provided, connect power to connector P3 and use connector P4 as the pass-through to additional boards.

Connect the wires for the three output power circuits on screw terminal pairs 9-10, 11-12, and 13-14.

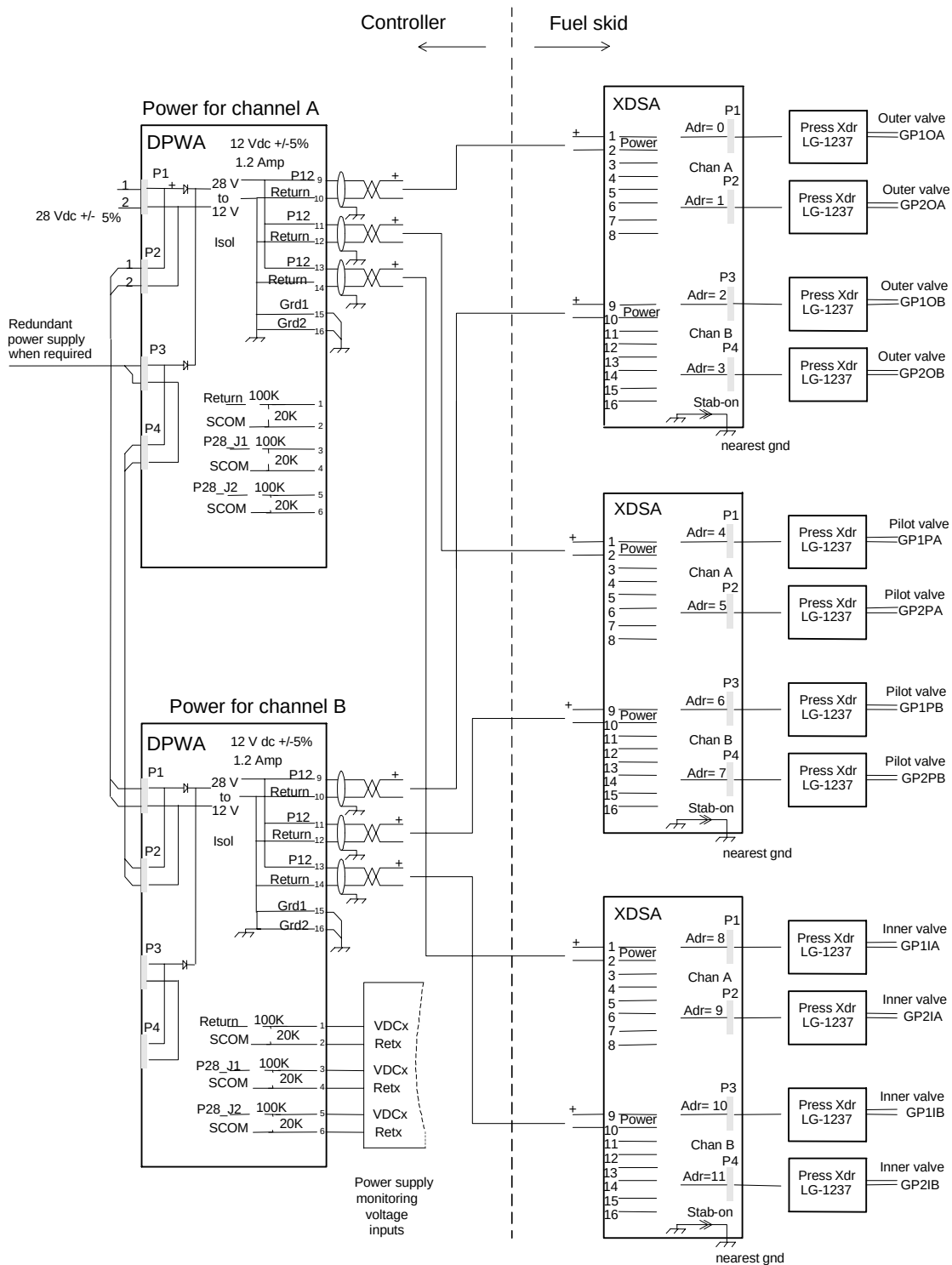
**Note** The DPWA terminal board includes two screw terminals, 15 and 16, for SCOM (ground) that must be connected to a good shield ground.



DPWA Board Block Diagram

## Operation

DPWA has an on-board power converter that changes the 28 V dc to 12 V dc for the transducers. A redundant 28 V dc supply can be added if needed. The following figure shows the DPWA power distribution system feeding power to 12 LG-1237 pressure transducers.



DPWA Power Distribution to XDSA and Smart Pressure Transducers

## Specifications

| Item               | Specification                                                                                    |
|--------------------|--------------------------------------------------------------------------------------------------|
| Number of Channels | Three power output terminal pairs                                                                |
| Input voltage      | 28 V dc $\pm 5\%$ , provisions for redundant source                                              |
| Input current      | Limited by protection to no more than 1.6 A steady state                                         |
| Output voltage     | 12 V dc $\pm 5\%$ , maximum total current of 1.2 A, short circuit protected, and self-recovering |
| Monitor voltages   | Attenuated by 6:1 ratio                                                                          |

## ***Diagnostics***

DPWA features three voltage outputs to permit monitoring of the board input power. The voltage monitor outputs are all attenuated by a 6:1 ratio to permit reading the 28 V dc using an input voltage with 5 V dc full scale input. Terminal 1 (PSRet) is the attenuated voltage present on the power input return line. Terminal 3 (PS28VA) is the attenuated voltage present on the P1 positive power input line. Terminal 5 (PS28VB) is the attenuated voltage present on the P3 positive power input line. Terminals 2, 4, and 6 provide a return SCOM path for the attenuator signals. In redundant systems, monitoring PS28VA and PS28VB permits the detection of a failed or missing redundant input. In systems with floating 28 V power, with the input centered on SCOM, the positive and return voltages should be approximately the same magnitude as a negative voltage on the return. If a ground fault is present in the input power, it may be detected by positive or return attenuated voltage approaching SCOM while the other signal doubles.

## ***Configuration***

There are no jumpers or hardware settings on the board.

---

# ***XDSA Transducer Interface***

## ***Functional Description***

The Transducer Interface (XDSA) terminal board is intended for installation adjacent to one or more type LG-1237 Honeywell<sup>®</sup> Smart Pressure Transducers featuring serial communications. The board accepts 12 V dc input power and serial data communications and routes the signals through four cables, with DB-25 connectors on each end, compatible with the Honeywell sensors. The board is designed with two independent circuits that support redundant sensor arrangements. Jumpers are provided to set sensor addresses and to select serial communications termination resistance. XDSA has features allowing connection of multiple XDSA boards in one system.

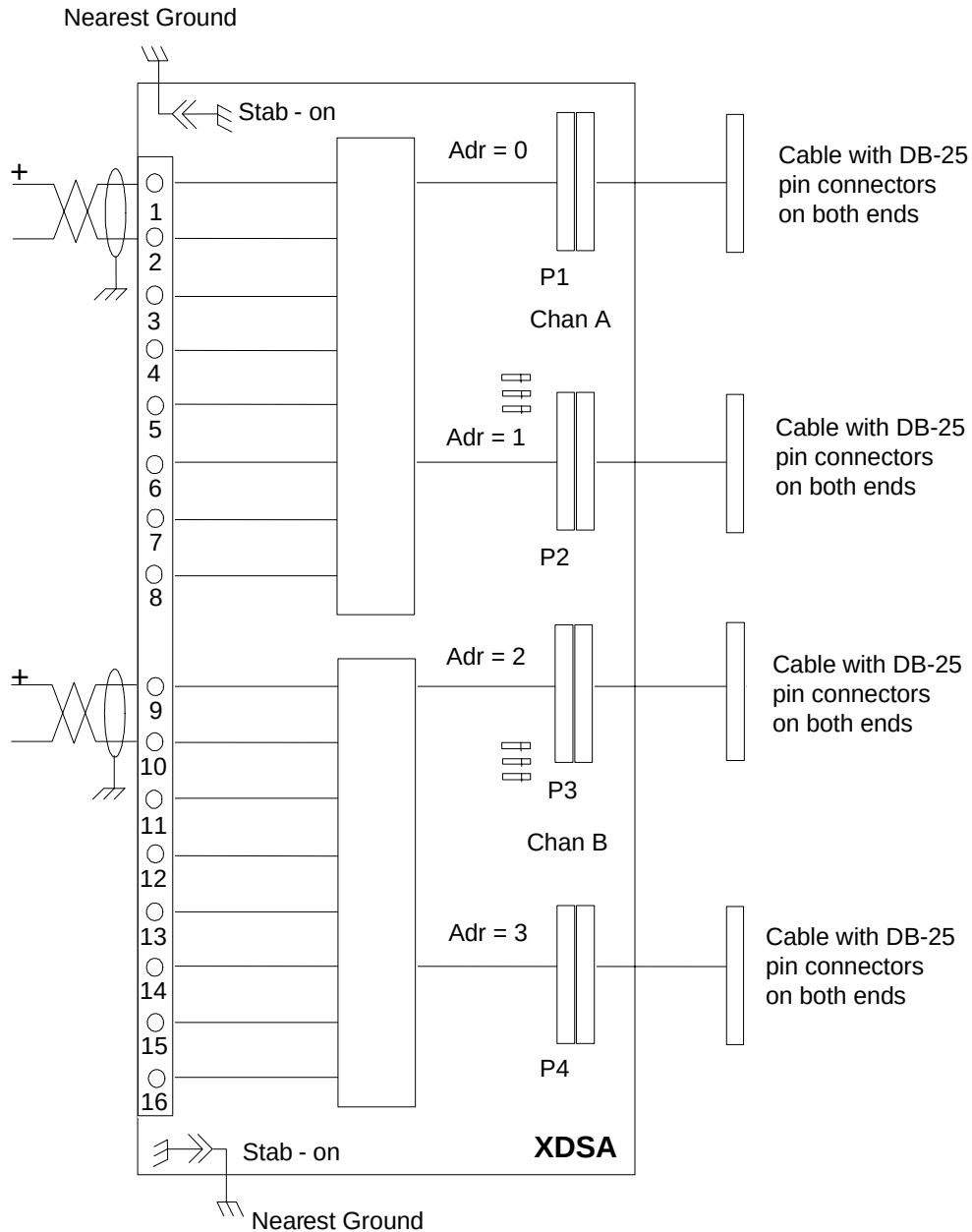
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**Note** XDSA provides signal routing to type LG-1237 Honeywell Smart Pressure Transducers.

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## Installation

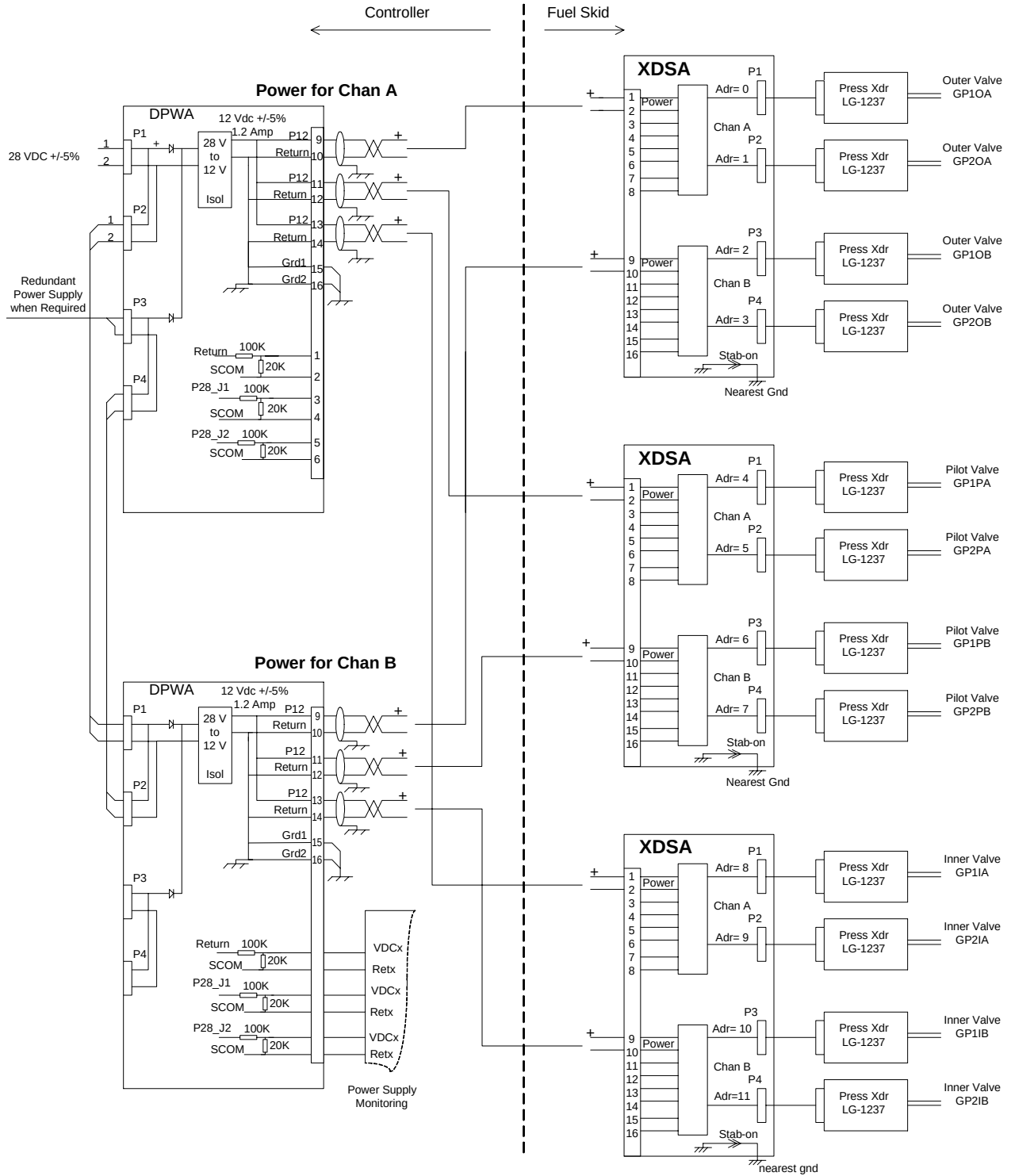
The following figure shows the wiring connections for the XDSA terminal board. Two DPWA terminal boards supply 12 V dc  $\pm 5\%$  to terminals 1, 2, 9, and 10. Terminals 3 through 8 and 11 through 16 are used for RS-422 multidrop communications. Each XDSA terminal board functions as two independent boards. A stab-on ground connection is located on each end of the board, one for each of the board sections. The board connects to four pressure sensors using cables with DB25 connectors on each end.



*XDSA Terminal Board Block Diagram*

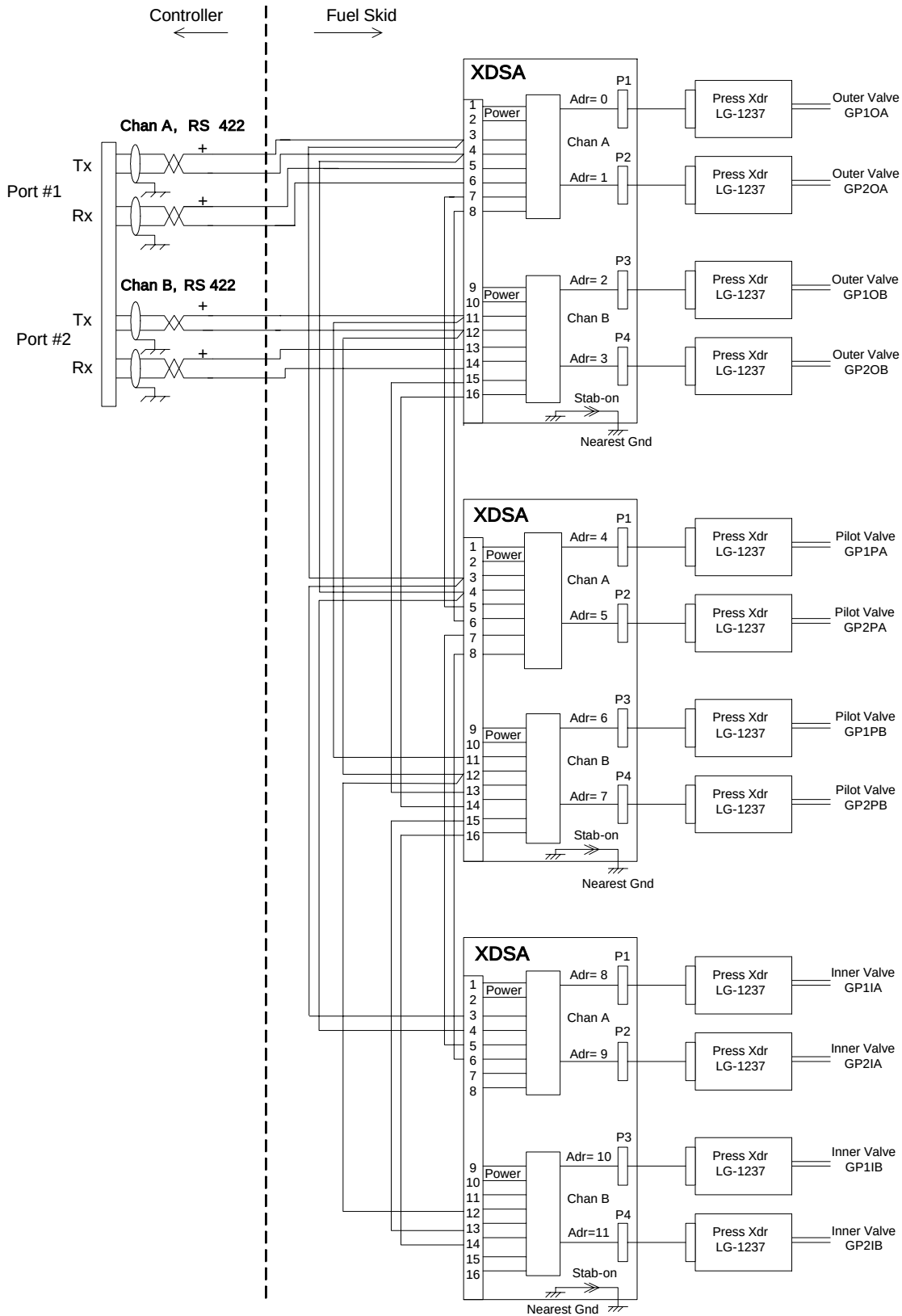
The following figure shows the power connection of three XDSA terminal boards and two DPWA boards. DPWA boards supply 12 V dc  $\pm 5\%$  using AWG#18 shielded twisted-pair wiring. Each XDSA terminal board supplies power for four LG-1237 pressure transducers using cables with DB-25 connectors on each end.

**Note** Power is separated between the two sections of the XDSA terminal board preserving the redundancy of the pressure sensing system. A separate ground is also provided for each section of the board.



DPWA Power Supplies and XDSA Terminal Boards

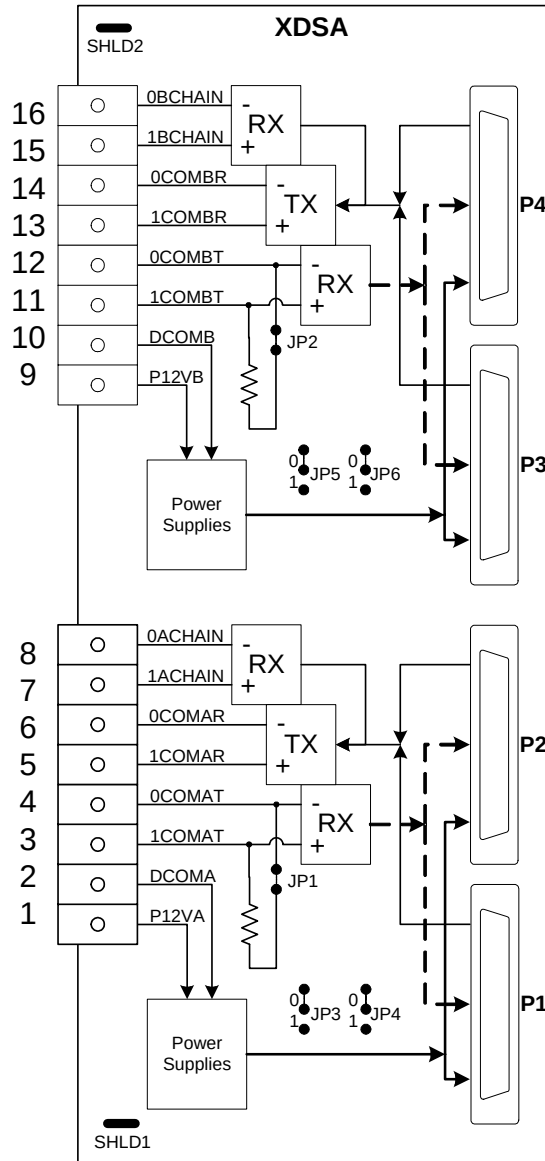
The following figure shows the serial communication wiring for three XDSA terminal boards connected to a pair of serial communication channels. The pass-through serial path is wired for signals from the sensors to the control. Refer to *Mark VI or Mark VIe Serial Communication Controller* documentation for specific connection points.



XDSA Serial Communication Wiring Diagram

## Operation

The following figure shows the functional block diagram for the XDSA terminal board. It shows the actual board layout. Input terminal 1 and output connector P1 are at the bottom of the board. Input power of 12 V dc  $\pm 5\%$  is applied to terminals 1 (positive) and 2 (negative). Serial transmissions from a control are received on terminals 3 (positive) and 4 (negative) with transmission path termination set by jumper JP1. Serial output from connected pressure sensors is on terminals 5 (positive) and 6 (negative). Terminals 7 (positive) and 8 (negative) provide a pass-through path for an additional XDSA board as shown in the *Installation* section. Device address selections are determined by jumpers JP3 and JP4. Device address selections are determined by jumpers JP3 and JP4.



DPWA Power Distribution to XDSA and Smart Pressure Transducers

## Specifications

| Item               | Specification                               |
|--------------------|---------------------------------------------|
| Number of Channels | DB-25 connections for four pressure sensors |
| Input voltage      | 12 V dc $\pm 5\%$ from DPWA or equivalent   |

## ***Diagnostics***

No diagnostic signals are obtained from the terminal board.

## ***Configuration***

Six jumpers are provided on the XDSA terminal board to select both RS-422 serial communication termination resistors and the address of the pressure sensors.

Jumpers JP1 and JP2 determine if the serial input terminating resistor is in or out. In is selected for the XDSA board that is at the end of the transmission path. Out is selected for all other XDSA boards within the signal path.

Jumpers JP3 through JP6 set the address of the sensors wired to P1 through P4. The sensor address is set by four signals on the DB-25 connector. The signals are a combination of fixed wiring and jumper positions on the two least significant bits. Each jumper has two positions, labeled 0 and 1. See the following table to determine the correct sensor address.

| Connector | A3 (8) | A2 (4) | A1 (2) | A0 (1) | Possible Values |
|-----------|--------|--------|--------|--------|-----------------|
| P1        | JP4    | JP3    | 0      | 0      | 0, 4, 8         |
| P2        | JP4    | JP3    | 0      | 0      | 1, 5, 9         |
| P3        | JP6    | JP5    | 1      | 0      | 2, 6, 10        |
| P4        | JP6    | JP5    | 1      | 1      | 3, 7, 11        |

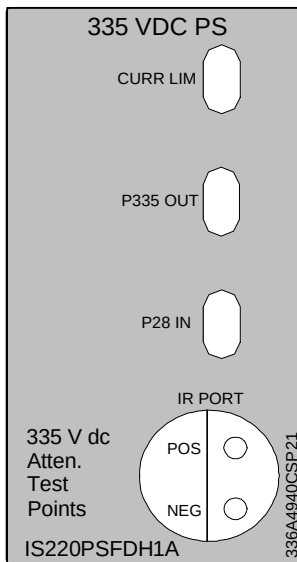


# PSFD Flame Detector Power Supply

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## PSFD Flame Detector Power Supply

### Functional Description



The Flame Detector Power Supply (PSFD) pack typically mounts above the primary gas turbine trip protection (TRPG) terminal board. The source power is 28 V dc, from a power distribution board (JPDL). The output is rated for 335 V dc, 5 mA. Three power supplies are connected to J3, J4, and J5 of the TRPG in a diode-ored, TMR configuration to power up to eight flame detectors. Each supply can power all eight flame detectors should the other two power supplies fail.

The main features of the pack include:

- Convection cooling – no cooling fans used
- Ambient temperature range is -30 to +65°C (-22 to +149 °F)
- 28 V dc input  $\pm 5\%$  (26.6 to 29.4 V dc)
- Unregulated output varies with input  $\pm 5\%$  (318 to 352 V dc)
- 1700 V dc isolation
- Output over voltage protection
- Test point pair to monitor Attenuated 335 V dc Output
- Three diagnostic LEDs
- Outputs can be diode-ored with external diode.
- Output current limit at 7 mA dc
- Soft start hot swap input limits inrush current to 550 mA peak.
- Input filtering limits emissions and reduces sensitivity to input interference

### Compatibility

The PSFD provides power to the flame detector circuit on TRPG through TRPG connectors J3, J4, and J5. The PSFD is typically mounted on sheet metal above the TRPG.

### Installation



To prevent electric shock, turn off power to the pack, then test to verify that no power exists on the module before touching it or any connected circuits.

#### Warning



To prevent equipment damage, do not remove, insert, or adjust any connections while power is applied to the equipment.

#### Caution

### ➤ To install the PSFD pack

- 1 Securely mount the TRPG and install the mounting plate for the PSFD. Typically, this mounting is on the upper level above the TRPG. To avoid risk of electrical shock, the mounting plant must be connected to chassis ground, typically FE (Field Earth).
- 2 Mechanically secure the PSFD using the threaded studs on the housing. The studs slide into a mounting brackets on the mounting plate.
- 3 Connect the 335 V dc cable between PSFD 2x2 connector P2 and J3, J4, or J5 on the TRPG.
- 4 Apply 28 V dc power to the pack by plugging in the 1x3 connector P1 on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.

## Operation

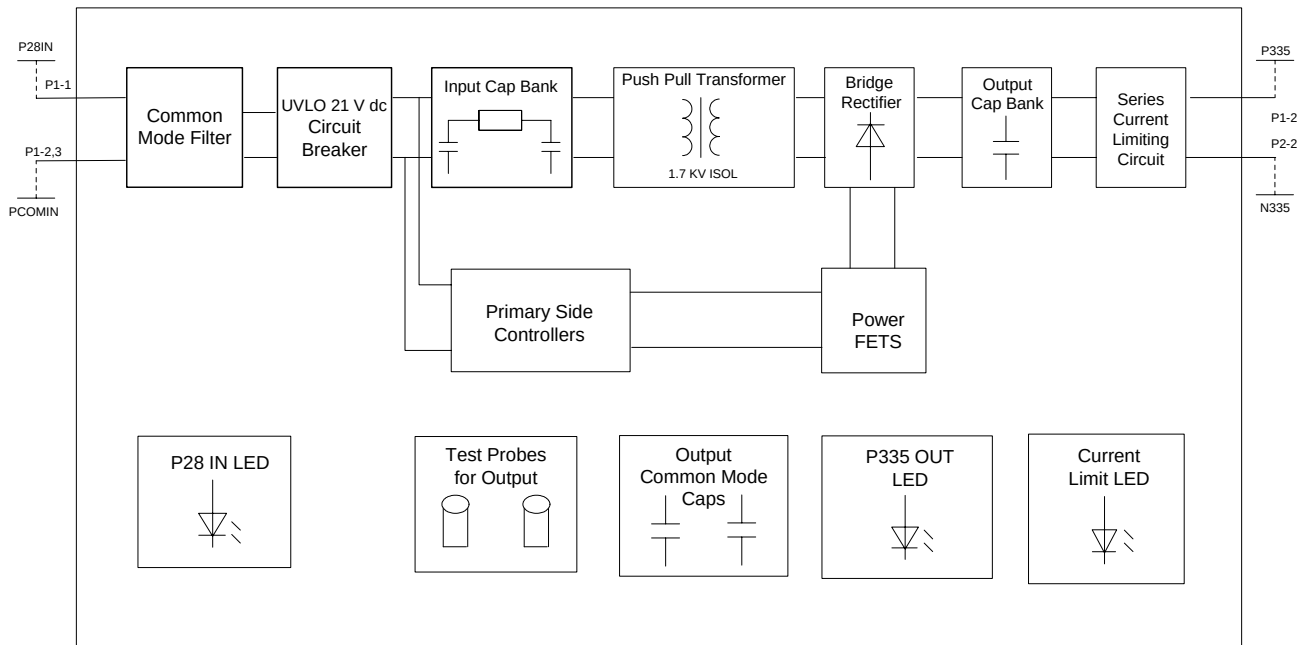
The PSFD produces 335 V dc from 28 V dc. The 28 V dc input is current limited and hot swap compatible. The input is transformer isolated from the floating output. The switching topology is a non-regulated fixed ratio push pull converter. The input and output are current limited and the input is also hot swappable.

The output voltage can be monitored locally using a differential pair of test points, attenuated 100:1.

The PSFD displays three status LEDs:

- Output current limit
- 335 V dc output present
- 28 V dc input present

The input and output LEDs do not indicate any particular voltage level and simply annunciate the presence of input or output voltage. Similarly, the current limit LED is for indication only and does not provide a measurement of the over current magnitude. The current limit LED is in series with the signal path for the activation signal. In the event that the current limit LEDs fails open, a circuit bypasses the LED and the limiter continues to function.



### Power Supply Block Diagram

This 25 kHz switching power supply topology is push-pull with no feedback, that is it is open loop. The output increases and decreases proportionately to the input voltage. The push pull transformer has a 1:12 turns ratio to raise the 28 V dc input to 336 V dc. Diode drops reduce the output voltage another 1.5 V dc, resulting in 334 to 335 V dc. The load regulation is good, even in this open loop design, because the current capacity of the power stage is much greater than the required load current.

The input circuit breaker provides inrush current protection as well as over current protection. During current limiting, the breaker modulates a series pass FET on and off to limit power dissipation. The PSFD is hot pluggable and will not disturb other sensitive loads if it is connected to an operating P28 V dc bus. If a circuit failure and short circuit occur downstream of the circuit breaker, the fast acting circuit breaker prevents this short from propagating onto the 28 V dc bus. An EMI filter reduces noise propagation onto the 28 V dc bus. A 33 V transorb, immediately after the input connector, protects the PSFD from voltage transients and momentary reverse bias connections.

The output limiter restricts the output current to 7 mA, even during a direct short. The output can stay shorted indefinitely even in a 65°C (149 °F) ambient. A 385 V MOV provides transient protection at the output.

## Specifications

| Item                                                    | PSFD Specification                                                      |
|---------------------------------------------------------|-------------------------------------------------------------------------|
| Maximum Input Voltage                                   | 29.4 V dc                                                               |
| Under voltage lockout (UVLO) range                      | 22.1 – 26.4 V dc                                                        |
| Inrush current limit                                    | 550 mA for 40 uS, 300 mA steady state                                   |
| Start up time at full load, 28 V dc                     | 34 mS                                                                   |
| Input current at full load, 28 V dc                     | 137 mA                                                                  |
| Input current ripple at full load, 28 V dc              | 66 mA at 50 kHz                                                         |
| Power consumption at full load, 28 V dc                 | 4.1 W                                                                   |
| Maximum power consumption at full load, 29.4 V dc input | 4.5 W                                                                   |
| Full load output                                        | 5 mA                                                                    |
| Output short circuit current limit with self recovery   | 7 mA                                                                    |
| Minimum output voltage, full load, 26.6 V dc input      | 317 V dc                                                                |
| Output voltage at full load, 28 V dc input              | 333 V dc                                                                |
| Maximum output voltage, no load, 29.4 V dc input        | 355 V dc                                                                |
| Output over voltage protection                          | 385 V MOV                                                               |
| Efficiency at full load                                 | 40%                                                                     |
| Load regulation                                         | -0.5%                                                                   |
| Typical output ripple at full load                      | 520 m Vp-p at 50 kHz                                                    |
| Line regulation                                         | 11%                                                                     |
| Nominal switching frequency                             | 25 ±6 kHz                                                               |
| Test point attenuation of 335 V dc                      | 100:1 Referenced to case                                                |
| Voltage isolation, output to input                      | 1700 V dc                                                               |
| Size                                                    | 8.26 cm high x 4.19 cm wide x 12.1cm deep (3.25 in x 1.65 in x 4.78 in) |
| Temperature, operating                                  | -30 to +65°C (-22 to +149 °F)                                           |
| Assembly technology                                     | Surface mount                                                           |

## ***Diagnostics***

### ***LEDs***

- Current Limit, Red, DS3 – activates at 6-7 mA.
- P335 Out, Green, DS2 – high voltage may be present at the output. A precise voltage level cannot be discerned from this LED.
- P28 In, Green, DS1 – voltage is present at the input. A precise voltage level cannot be discerned from this LED.

### ***Test Points***

The output voltage can be monitored locally using a differential pair of test points. The positive and negative test points connect to the positive and negative outputs through 100:1 attenuators which are referenced to the chassis for safety. Each test point can be touched without risk or electrical shock. Furthermore, each test point can be shorted to the chassis indefinitely. The test points are designated TP\_POS (inboard) and TP\_NEG (outboard). The test points are accessed by rotating the round plastic cover on the top.

### ***Configuration***

There are no jumpers or hardware settings on the board.

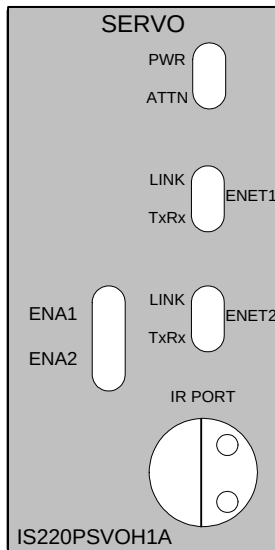
### ***Alarms***

The output voltage from each PSFD is attenuated and sensed on the TREG terminal board. The sensed voltage is monitored by the PPRO or VPRO modules. In a TMR configuration, if any of the three PSFD fails to provide 335 V dc, an alarm is annunciated in the ToolboxST\* application or HMI.

# PSVO Servo Control

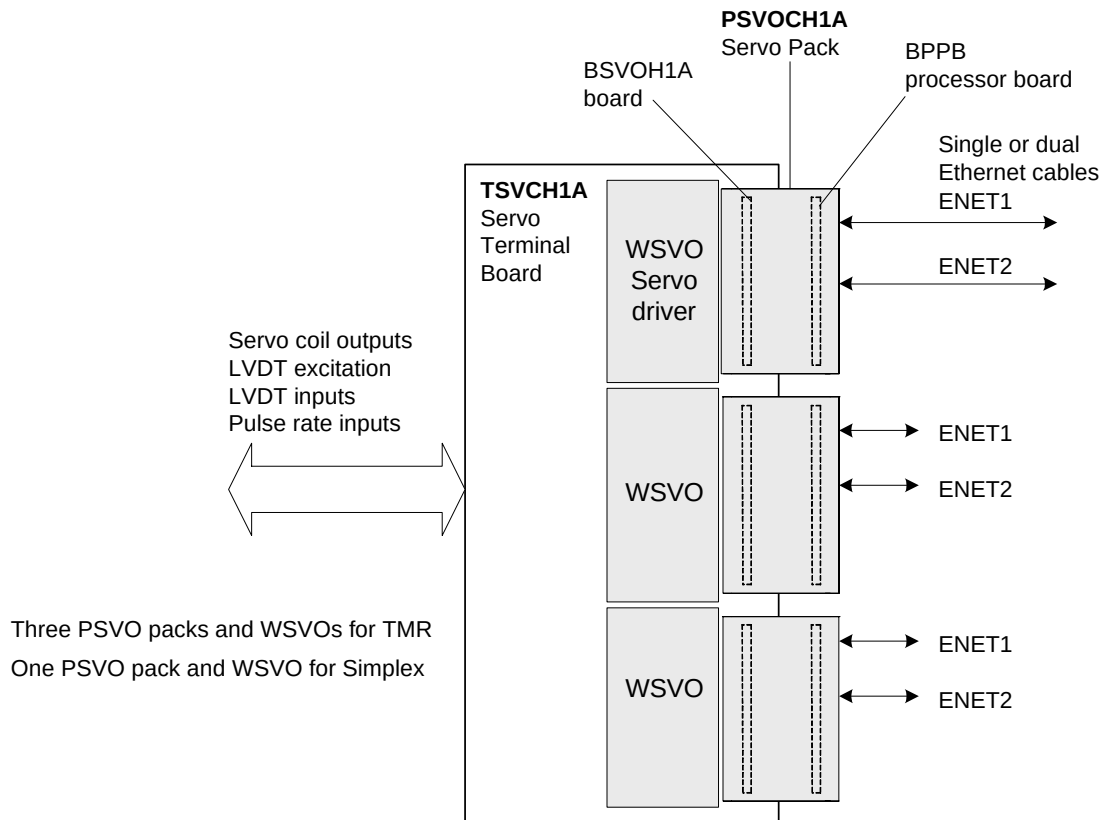
## PSVO Servo Control

### Functional Description



The Servo Control (PSVO) pack provides the electrical interface between one or two I/O Ethernet networks and a TSVO servo terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs and an I/O board specific to the servo function. The pack uses the adjacent WSVO servo driver module to handle two servo valve position loops, with a selection of five servo valve output currents from 10-120 mA dc. The pack supplies LVDT excitation, and accepts eight LVDT feedbacks and two pulse rate inputs from fuel flow meters.

Input to the pack is through dual RJ45 Ethernet connectors, and 28 V dc power is supplied from the terminal board. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PSVOH1A is compatible with the Servo Terminal Board TSVCH1A, but not the DIN-rail mounted DSVO board or the TSVOH1B. The following table gives details of the compatibility:

| Terminal Board | TSVCH1A     |            |         | TSVOH1B |    | DSVO | SSVO        |
|----------------|-------------|------------|---------|---------|----|------|-------------|
| Control mode   | Simplex-yes | Dual - yes | TMR-yes | No      | No | No   | Simplex-yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

## Installation

### ➤ To install the PSVO pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one (simplex) or three packs (for TMR) into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded inserts adjacent to the Ethernet ports. The inserts connect with a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug the WSVO servo driver assemblies into the J2 48-pin connectors and secure with the four screws.
- 5 Plug in one or two Ethernet cables depending on the system configuration. The pack operates over either port. If dual connections are used, standard practice is to hook ENET1 to the network associated with the R controller, however, the PSVO is not sensitive to Ethernet connections and negotiates proper operation over either port.
- 6 Apply power to the packs and drivers using the power switches on TSVO. Use SW3 for R, SW2 for S, and SW1 for T, and check the indicator lights.
- 7 Configure the I/O pack as necessary.

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**Note** The PSVO along with its associated WSVO servo driver assembly mounts directly to a Mark VIe TSVOH1D terminal board.

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# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## **BSVO Servo Board**

The BSVO board multiplexes 24 analog channels into a 16-bit A/D converter. The 100 kHz A/D has a  $\pm 10$  V dc range, and handles the servo current regulator signals, the LVDT inputs, and power supply monitoring. The current references for the analog current regulators on WSVO are generated on the BSVO by a 14-bit D/A converter. Excitation for the LVDTs is developed using a D/A converter outputs a sine wave with a frequency of 3.2 kHz. This is filtered and passed to the WSVO. The board provides signal conditioning for two pulse rate channels and passes the signals to the processor board to determine the pulse rate.

## **WSVO Servo Driver Assembly**

The servo driver assembly has a power supply that converts the P28 voltage input to a positive 15 V and negative 15 V output for the servo current regulator circuits. There are two servo current regulators working off the current references from the servo pack. The servo driver circuit has a selection of five configurable gains, and the assembly contains the servo suicide relays and excitation output driver circuits.

### **Verification**

The three ways to verify servo performance through stroking the actuator are manual, position ramping, and step current. In manual mode, the desired value is entered numerically and the performance monitored from the trend recorder. Select **Verify Position** to apply a ramp to the actuator, and select **Verify Current** to apply a step input to the actuator. The trend recorder displays any abnormalities in the actuator stroke.

### **ID Line**

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-62 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

### **Power Management**

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

### **Status LEDs**

A yellow LED labeled ENA1 is lit when Servo1 is enabled and not suicided.

A yellow LED labeled ENA2 is lit when Servo2 is enabled and not suicided.

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.



A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

### Connectors

- A DC-62 pin connector on the underside of the I/O pack connects directly to a discrete output terminal board.
- An RJ45 Ethernet connector named ENET1 on the pack side is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the pack side is the redundant or secondary system interface.

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**Note** The terminal board provides fused power output from a power source that is applied directly to the terminal board, not through this pack connector.

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## Specifications

The following table provides information specific to the PSVO pack and WSV0 driver.

| Item                        | Specification                                                                                                                                                                                                                                                                                  |
|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs            | Eight LVDT windings<br>Two pulse rate signals                                                                                                                                                                                                                                                  |
| Number of outputs           | Two servo valve currents<br>Two excitation sources for LVDTs<br>Two excitation sources for pulse rate transducers                                                                                                                                                                              |
| Power supply voltage        | Nominal 28 V dc                                                                                                                                                                                                                                                                                |
| LVDT accuracy               | 1% with 14-bit resolution                                                                                                                                                                                                                                                                      |
| LVDT input filter           | Low pass filter with 3 down breaks at 50 rad/sec $\pm 15\%$                                                                                                                                                                                                                                    |
| LVDT common mode rejection  | CMR is 1 V, 60 dB at 50/60 Hz                                                                                                                                                                                                                                                                  |
| LVDT excitation output      | Frequency of $3.2 \pm 0.2$ kHz<br>Voltage of $7.00 \pm 0.14$ V rms                                                                                                                                                                                                                             |
| Pulse rate accuracy         | 0.05% of reading with 16-bit resolution at 50 Hz frame rate<br>Noise of acceleration measurement is less than $\pm 50$ Hz/sec for a 10,000 Hz signal being read at 10 ms                                                                                                                       |
| Pulse rate input            | Minimum signal for proper measurement at 2 Hz is 33 mVpk, and at 12 kHz is 827 mVpk                                                                                                                                                                                                            |
| Magnetic PR pickup signal   | Generates 150 V p-p into 60 k $\Omega$                                                                                                                                                                                                                                                         |
| Active PR Pickup Signal     | Generates 5 to 27 V p-p into 60 k $\Omega$                                                                                                                                                                                                                                                     |
| Servo valve output accuracy | 2% with 12-bit resolution<br>Dither amplitude and frequency adjustable                                                                                                                                                                                                                         |
| Fault detection             | Servo current out of limits or not responding<br>Regulator feedback signal out of limits<br>Servo suicided<br>Calibration voltage range fault<br>The LVDT excitation is out of range<br>The input signal varies from the voted value by more than the TMR differential limit<br>Failed ID chip |
| <b>Physical</b>             |                                                                                                                                                                                                                                                                                                |
| Size                        | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in. x 1.65 in. x 4.78 in.)                                                                                                                                                                                                                    |
| Technology                  | Surface-mount                                                                                                                                                                                                                                                                                  |
| Temperature                 | Operating: -30 to 65°C (-22 to +149 °F)                                                                                                                                                                                                                                                        |

## ***Diagnostics***

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on preset (non-configurable) high and low levels near the end of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. The logic signal, L3DIAG\_XXXX, refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limits.
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

### IS200TSVC Variable Definitions

| Parameter                                      | Description                                                                                                                                                                                                                                                                              | Choices                                                                                        |
|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| <b>ServoOutput#</b><br><b>where # = 1 or 2</b> | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                                                                                       | <b>Point Edit (Input Real)</b>                                                                 |
| RegNumber                                      | Maps a specific regulator to a given servo output.                                                                                                                                                                                                                                       | Unused, Reg1, Reg2<br>(Default-Unused)                                                         |
| Servo_MA_Out                                   | Nominal servo current rating in milliamperes.                                                                                                                                                                                                                                            | 10ma, 20ma, 40ma, 80ma, 120ma<br>(Default-10mA)                                                |
| EnablCurSuic                                   | Enable Current Suicide Function                                                                                                                                                                                                                                                          | Enable, Disable<br>(Default-Disable)                                                           |
| EnablFbkSuic                                   | Enable Position Feedback Suicide Function                                                                                                                                                                                                                                                | Enable, Disable<br>(Default-Disable)                                                           |
| EnblAutGain                                    | Enable Auto Gain function. Approved for 4_LV_LM, 3_LVLXM and 4_LVLXM regulator configurations.                                                                                                                                                                                           | Enable, Disable<br>(Default-Disable)                                                           |
| Coil_RS_Only                                   | Configuration parameter is enabled when the PSVO is driving a 2-coil servo. For 2-coil servo, no load is connected to the SxTH/L where x = 1or 2 terminal screws.                                                                                                                        | Enable, Disable<br>(Default-Disable)                                                           |
| AV_Selector                                    | Configuration selector to map one of the specified variables to the PSVO variable, ServoxMonitorNV where x = 1 or 2.                                                                                                                                                                     | Coil_OHMs,<br>Compliance_Voltage<br>LM_Auto_Gain<br>MA_CMD_PCT<br>(Default-Compliance_Voltage) |
| Curr_Suicide                                   | Current command is compared to the actual feedback current. If the error exceeds the configuration limit, Curr_Suicide (%), then the Servo output will suicide.                                                                                                                          | 0 to 100<br>(Default-5)                                                                        |
| Fdbk_Suicide                                   | The position feedback, Regx_Fdbk (%) is compared against the value, 100% + Fdbk_Suicide (%). If Regx_Fdbk (%) where x = 1 or 2 exceeds that value, the regulator assumes the feedback has gone open loop and the servo must be suicided if this condition and the EnablFbkSuic = Enable. | 0 to 100<br>(Default-5)                                                                        |
| OpenCoilSuic                                   | If configuration parameter, OpenCoilSuic = Enable, then the servo coil open detection function will suicide the servo if the function detects an open ckt. Note: Set OpenCoildiag = Enable to receive a diagnostic message to why the servo suicide occurred.                            | Enable, Disable<br>(Default-Disable)                                                           |
| ShrtCoilSuic                                   | If configuration parameter, ShrtCoilSuic = Enable, then the servo coil short ckt. detection function will suicide the servo if the function detects a short ckt. Note: Set ShrtCoildiag = Enable to receive a diagnostic message to why the servo suicide occurred.                      | Enable, Disable<br>(Default-Disable)                                                           |
| OpenCoildiag                                   | If enabled, a specific diagnostic message is generated for why the servo suicide occurred; i.e. Servo x Suicide due to Open servo coil.                                                                                                                                                  | Enable, Disable<br>(Default-Disable)                                                           |
| ShrtCoildiag                                   | If enabled, a specific diagnostic message is generated for why the servo suicide occurred; i.e. Servo x Suicide due to Short circuit of servo coil.                                                                                                                                      | Enable, Disable<br>(Default-Disable)                                                           |

| Parameter                               | Description                                                                                                                                                                                                       | Choices                                                                                                                                              |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>ServoOutput#</b><br>where # = 1 or 2 | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                | <b>Point Edit (Input Real)</b>                                                                                                                       |
| TbmAJumpPos                             | TSVC terminal board mA jumper position selection. This should match the jumper selection on the TSVC to allow the open / short circuit servo coil detection to work correctly.                                    | 10ma, 20ma, 40ma, 80ma, 120ma_A, 120ma_B (Default-10mA)                                                                                              |
| RopenTimeLim                            | Time in seconds required for the open circuit condition of the servo coil to be in effect before a diagnostic and / or suicide of the servo (if enabled) occurs.                                                  | 0 to 100 (Default-1)                                                                                                                                 |
| RShrtTimeLim                            | Time in seconds required for the short circuit condition of the servo coil to be in effect before a diagnostic and / or suicide of the servo (if enabled) occurs.                                                 | 0 to 100 (Default-1)                                                                                                                                 |
| RcoilOpen                               | Defines the initial value for the open circuit resistance in ohms. After the LVDT calibration, the value for RcoilOpen = 2 * (Servo Compliance Voltage / Servo Current) measured during the calibration mode.     | 1 to 10E+09 (Default- 1000000)                                                                                                                       |
| RcoilShort                              | Defines the initial value for the short circuit resistance in ohms. After the LVDT calibration, the value for RcoilShort = 0.5 * (Servo Compliance Voltage / Servo Current) measured during the calibration mode. | 1 to 10E+09 (Default- 0)                                                                                                                             |
| TMR_DiffLimt                            | Diagnostic limit, TMR Input Vote difference in %                                                                                                                                                                  | 0 to 110 (Default-25)                                                                                                                                |
| <b>FlowRatex</b><br>where x = 1 or 2    | <b>Bipolar input = PRxH – PRxL,<br/>Unipolar = TTLx - PRxL</b>                                                                                                                                                    | <b>Point Edit (Input Real)</b>                                                                                                                       |
| PRTtype                                 | Define the pulse rate feedback type or basic speed range. And defines the span of pulses used to have the Free Running counter to collect time over.                                                              | Flow, Speed, Speed_High, Speed_HSNG, Speed_LM, Unused                                                                                                |
| SysLim1Enabl                            | If enabled, System Limit 1 is active.                                                                                                                                                                             | Enable, Disable (Default-Disable)                                                                                                                    |
| SysLim1Latch                            | If enabled, the System Limit 1 function will latch its state if the FlowRate exceeds the limit function defined by SysLim1Type and SysLimit1.                                                                     | Latch, NotLatch (Default-Latch)                                                                                                                      |
| SysLim1Type                             | Defines the compare function used in the Limit1 expression.                                                                                                                                                       | >=, <= (Default->=)                                                                                                                                  |
| SysLimit1                               | Defines Limit1 value to be used for the input, FlowRate.                                                                                                                                                          | 0 to 20,000 (Default-0)                                                                                                                              |
| SysLim2Enabl                            | If enabled, System Limit 2 is active.                                                                                                                                                                             | Enable, Disable (Default-Disable)                                                                                                                    |
| SysLim2Latch                            | If enabled, the System Limit 2 function will latch its state if the FlowRate exceeds the limit function defined by SysLim2Type and SysLimit2.                                                                     | Latch, NotLatch (Default-Latch)                                                                                                                      |
| SysLim2Type                             | Defines the compare function used in Limit 2's expression.                                                                                                                                                        | >=, <= (Default->=)                                                                                                                                  |
| SysLimit2                               | Defines Limit2 value to be used for the input, FlowRate.                                                                                                                                                          | 0 to 20,000 (Default-0)                                                                                                                              |
| TMR_DiffLimt                            | Diagnostic limit, TMR Input Vote difference in %                                                                                                                                                                  | 0 to 20,000 (Default-5)                                                                                                                              |
| <b>Regulator Parameters</b>             |                                                                                                                                                                                                                   |                                                                                                                                                      |
| <b>Common</b>                           | <b>The following parameters are common for all regulator</b>                                                                                                                                                      |                                                                                                                                                      |
| Reg_Type                                | Regulator Algorithm Type                                                                                                                                                                                          | Unused, no_fbk, 1_LVposition, 1_PulseRate, 2_LVpilotCyl, 2_LVposMAX, 2_LVposMIN, 2_PlsRateMAX, 3_LV_LMX, 3_LVposMID, 4_LV_LM, 4_LV_LMX, 4_LVp/cylMAX |

| Parameter                               | Description                                                                                                                                                                                                                                     | Choices                                                                            |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| <b>ServoOutput#</b><br>where # = 1 or 2 | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                                              | <b>Point Edit (Input Real)</b>                                                     |
| Dither_Freq                             | Dither rate in hertz.                                                                                                                                                                                                                           | 12_5hz, 25hz, 33_33hz, 50hz, 100hz, Unused<br>(Default-100hz)                      |
| DitherAmpl                              | Dither in % current                                                                                                                                                                                                                             | 0 to 10<br>(Default-2)                                                             |
| LVDT_Margin                             | Defines the over range in % for the LVDT input. A diagnostic is generated if this value is exceeded.                                                                                                                                            | 0 to 100<br>(Default-2)                                                            |
| LVDT1input                              | LVDT input selection                                                                                                                                                                                                                            | LVDT1, LVDT2, LVDT3, LVDT4, LVDT5, LVDT6, LVDT7, LVDT8, Unused<br>(Default-Unused) |
| RegGain                                 | Position loop Gain in % current / Eng Units or usually % current / % position.                                                                                                                                                                  | -200 to +200<br>(Default-1)                                                        |
| RegNullBias                             | Regulator Null Bias provides a fixed current command in percent to cancel or null the spring force of the valve which will close the valve if the servo suicides or shuts down.                                                                 | -100 to +100<br>(Default-0)                                                        |
| TMR_DiffLimt                            | Diagnostic limit, TMR Input Vote difference in %                                                                                                                                                                                                | 0 to 150<br>(Default-5)                                                            |
| <b>RegType</b>                          | <b>Pulse Rate Regulator used with a single LVDT Input.</b>                                                                                                                                                                                      | <b>= 1 LV position</b>                                                             |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150(Default-100)                                                            |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150(Default-0)                                                              |
| MnLVDT1_Vrms                            | LVDT1 Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDT1 Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1 (Default-1)                                                               |
| MxLVDT1_Vrms                            | LVDT1 Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDT1 Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1 (Default-1)                                                               |
| <b>RegType</b>                          | <b>Pulse Rate Regulator used with a single fuel flow divider feedback.</b>                                                                                                                                                                      | <b>= 1_PulseRate</b>                                                               |
| PRateInput1                             | Pulse Rate input selection                                                                                                                                                                                                                      | PR1, PR2, Unused<br>(Default-Unused)                                               |
| <b>RegType</b>                          | <b>Pilot Cylinder Regulator with two LVDT position feedbacks.</b>                                                                                                                                                                               | <b>= 2_LVpilotCyl</b>                                                              |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)                                                        |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)                                                          |
| MnLVDTx_Vrms<br>where x = 1 to 2        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                            |
| MxLVDTx_Vrms<br>where x = 1 to 2        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                            |

| Parameter                               | Description                                                                                                                                                                                                                                     | Choices                              |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| <b>ServoOutput#</b><br>where # = 1 or 2 | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                                              | <b>Point Edit (Input Real)</b>       |
| PilotGain                               | Pilot loop gain in % current / Eng. unit                                                                                                                                                                                                        | -200 to +200<br>(Default-1)          |
| <b>RegType</b>                          | <b>Position Regulator using the maximum select from 2 LVDT inputs for feedback.</b>                                                                                                                                                             | <b>= 2_LVposMAX</b>                  |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)          |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)            |
| MnLVDTx_Vrms<br>where x = 1 to 2        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)              |
| MxLVDTx_Vrms<br>where x = 1 to 2        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)              |
| <b>RegType</b>                          | <b>Position Regulator using the minimum select from 2 LVDT inputs for feedback.</b>                                                                                                                                                             | <b>= 2_LVposMIN</b>                  |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)          |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)            |
| MnLVDTx_Vrms<br>where x = 1 to 2        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)              |
| MxLVDTx_Vrms<br>where x = 1 to 2        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)              |
| <b>RegType</b>                          | <b>Pulse Rate Regulator using the maximum select from two fuel flow divider feedbacks.</b>                                                                                                                                                      | <b>= 2_PIsRateMAX</b>                |
| PRateInput1                             | Pulse Rate 1 input selection                                                                                                                                                                                                                    | PR1, PR2, Unused<br>(Default-Unused) |
| PRateInput2                             | Pulse Rate 2 input selection                                                                                                                                                                                                                    | PR1, PR2, Unused<br>(Default-Unused) |
| <b>RegType</b>                          | <b>Position Regulator using the median select from 3 LVDT inputs for feedback. Originally designed for the LMX100 gas turbine.</b>                                                                                                              | <b>= 3_LV_LMX</b>                    |
| CurBreak                                | Current break for nonlinear servo current                                                                                                                                                                                                       | 0 to 100<br>(Default-2)              |
| CurClpNg                                | Servo Current Clamp (%) Negative                                                                                                                                                                                                                | -300 to 300<br>(Default- -300)       |
| CurClpPs                                | Servo Current Clamp (%) Positive                                                                                                                                                                                                                | -300 to 300<br>(Default- 300)        |
| CurSlope1                               | Slope current gain modifier for low position error values                                                                                                                                                                                       | 0 to 10<br>(Default-1)               |

| Parameter                               | Description                                                                                                                                                                                                                                     | Choices                         |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|
| <b>ServoOutput#</b><br>where # = 1 or 2 | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                                              | <b>Point Edit (Input Real)</b>  |
| CurSlope2                               | Slope current gain modifier for position error > CurBreak limit                                                                                                                                                                                 | 0 to 10<br>(Default-1)          |
| DefltValue                              | If all position sensors or LVDTs are bad, the regulator feedback is assigned to this value in percent.                                                                                                                                          | 0 to 110<br>(Default-100)       |
| LagTau                                  | Position loop Lag Breakpoint (seconds), zero to disable                                                                                                                                                                                         | 0 to 10<br>(Default-0)          |
| LeadTau                                 | Position loop Lead Breakpoint (seconds), zero to disable                                                                                                                                                                                        | 0 to 10<br>(Default-0)          |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)     |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)       |
| MnLVDTx_Vrms<br>where x = 1 to 3        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)         |
| MxLVDTx_Vrms<br>where x = 1 to 3        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)         |
| SelectMinMax                            | If 2 of the 3 LVDTs are healthy, this parameter determines whether a minimum select or maximum select is made for the remaining two sensors.                                                                                                    | Max, Min<br>(Default-Max)       |
| SensorOofRTD                            | Sensor Out of Range Time Delay (seconds)                                                                                                                                                                                                        | 0 to 2000<br>(Default-10)       |
| SenSpreadMx                             | Sensor Spread Maximum (%)                                                                                                                                                                                                                       | -2000 to 2000<br>(Default-1000) |
| SensoSpreadTD                           | Sensor Spread Time Delay (seconds)                                                                                                                                                                                                              | 0 to 2000<br>(Default-10)       |
| <b>RegType</b>                          | <b>Position Regulator using the median select from 3 LVDT inputs for feedback. Originally designed for heavy-duty gas turbines.</b>                                                                                                             | <b>= 3_LVposMID</b>             |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)     |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)       |
| MnLVDTx_Vrms<br>where x = 1 to 3        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)         |
| MxLVDTx_Vrms<br>where x = 1 to 3        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)         |

| Parameter                               | Description                                                                                                                                                                                                                                     | Choices                             |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|
| <b>ServoOutput#</b><br>where # = 1 or 2 | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                                              | <b>Point Edit    (Input Real)</b>   |
| <b>RegType</b>                          | <b>Position Regulator selecting one of two ratio-metric LVDT pairs for the position feedback. Originally designed for the LM1600, LM2500 &amp; LM6000 gas turbines.</b>                                                                         | <b>=4_LV_LM</b>                     |
| CurBreak                                | Current break for nonlinear servo current                                                                                                                                                                                                       | 0 to 100<br>(Default-2)             |
| CurClpNg                                | Servo Current Clamp (%) Negative                                                                                                                                                                                                                | -300 to 300<br>(Default -300)       |
| CurClpPs                                | Servo Current Clamp (%) Positive                                                                                                                                                                                                                | -300 to 300<br>(Default- 300)       |
| CurSlope1                               | Slope current gain modifier for low position error values                                                                                                                                                                                       | 0 to 10<br>(Default-1)              |
| CurSlope2                               | Slope current gain modifier for position error > CurBreak limit                                                                                                                                                                                 | 0 to 10<br>(Default-1)              |
| DefltValue                              | If all position sensors or LVDTs are bad, the regulator feedback is assigned to this value in percent.                                                                                                                                          | 0 to 110<br>(Default-100)           |
| LagTau                                  | Position loop Lag Breakpoint (seconds), zero to disable                                                                                                                                                                                         | 0 to 10<br>(Default-0)              |
| LeadTau                                 | Position loop Lead Breakpoint (seconds), zero to disable                                                                                                                                                                                        | 0 to 10<br>(Default-0)              |
| LVDTVsumMarg                            | Allowable rang exceed error (%) for ratio-metric sum                                                                                                                                                                                            | 1 to 100<br>(Default-2)             |
| MaxPOSvalue                             | Position in Eng. Units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)         |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)           |
| MnLVDTx_Vrms<br>where x = 1 to 4        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)             |
| MxLVDTx_Vrms<br>where x = 1 to 4        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)             |
| PosDefltEnab                            | Position Default Enable / Disable                                                                                                                                                                                                               | Enable, Disable<br>(Default-Enable) |
| PosDiffcmp1                             | Position Difference Limit1 (%)                                                                                                                                                                                                                  | 0 to 110<br>(Default-3)             |
| PosDiffcmp2                             | Position Difference Limit2 (%)                                                                                                                                                                                                                  | 0 to 110<br>(Default-3)             |
| PosDifftime1                            | Position Difference Limit1 Timeout (seconds)                                                                                                                                                                                                    | 0 to 10<br>(Default-0.5)            |
| PosDifftime2                            | Position Difference Limit2 Timeout (seconds)                                                                                                                                                                                                    | 0 to 10<br>(Default-0.5)            |
| PosSelect                               | Position Selection Mode                                                                                                                                                                                                                         | Avg, Max, Min<br>(Default-Avg)      |



| Parameter                               | Description                                                                                                                                                                                                                                     | Choices                           |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| <b>ServoOutput#</b><br>where # = 1 or 2 | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                                              | <b>Point Edit    (Input Real)</b> |
| <b>RegType</b>                          | <b>Position Regulator selecting from 2 LVDT ratio-metric pairs for feedback.</b>                                                                                                                                                                | <b>= 4_LV_LMX</b>                 |
| CurBreak                                | Current break for nonlinear servo current                                                                                                                                                                                                       | 0 to 100<br>(Default-2)           |
| CurClpNg                                | Servo Current Clamp (%) Negative                                                                                                                                                                                                                | -300 to 300<br>(Default -300)     |
| CurClpPs                                | Servo Current Clamp (%) Positive                                                                                                                                                                                                                | -300 to 300<br>(Default- 300)     |
| CurSlope1                               | Slope current gain modifier for low position error values                                                                                                                                                                                       | 0 to 10<br>(Default-1)            |
| CurSlope2                               | Slope current gain modifier for position error > CurBreak limit                                                                                                                                                                                 | 0 to 10<br>(Default-1)            |
| DefltValue                              | If all position sensors or LVDTs are bad, the regulator feedback is assigned to this value in percent.                                                                                                                                          | 0 to 110<br>(Default-100)         |
| LagTau                                  | Position loop Lag Breakpoint (seconds), zero to disable                                                                                                                                                                                         | 0 to 10<br>(Default-0)            |
| LeadTau                                 | Position loop Lead Breakpoint (seconds), zero to disable                                                                                                                                                                                        | 0 to 10<br>(Default-0)            |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)       |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150 (Default-0)            |
| MnLVDTx_Vrms<br>where x = 1 to 4        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)           |
| MxLVDTx_Vrms<br>where x = 1 to 4        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)           |
| SelectMinMax                            | If 2 of the 3 LVDTs are healthy, this parameter determines whether a minimum select or maximum select is made for the remaining two sensors.                                                                                                    | Max, Min<br>(Default-Max)         |
| SensorOofRTD                            | Sensor Out of Range Time Delay (seconds)                                                                                                                                                                                                        | 0 to 2000 (Default-10)            |
| SenSpreadMx                             | Sensor Spread Maximum (%)                                                                                                                                                                                                                       | -2000 to 2000<br>(Default-1000)   |
| SensoSpreadTD                           | Sensor Spread Time Delay (seconds)                                                                                                                                                                                                              | 0 to 2000 (Default-10)            |
| SenSumChkTD                             | Volts RMS Sum Check Out of Range Time Delay (seconds)                                                                                                                                                                                           | 0 to 2000 (Default-10)            |
| <b>RegType</b>                          | <b>Pilot Cylinder Regulator with two LVDT position feedbacks.</b>                                                                                                                                                                               | <b>= 4_LVp/cylIMAX</b>            |
| MaxPOSvalue                             | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150 (Default-100)          |
| MinPOSvalue                             | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150 (Default-0)            |
| MnLVDTx_Vrms<br>where x = 1 to 4        | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)           |

| Parameter                               | Description                                                                                                                                                                                                                                     | Choices                        |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| <b>ServoOutput#</b><br>where # = 1 or 2 | <b>Servo Output X measured current in percent.</b>                                                                                                                                                                                              | <b>Point Edit (Input Real)</b> |
| MxLVDTx_Vrms<br>where x = 1 to 4        | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)        |
| PilotGain                               | Pilot loop gain in % current / Eng. unit                                                                                                                                                                                                        | -200 to +200<br>(Default-1)    |

| Parameter                   | Description                                                                                                                                                                                                                                     | Value Range / Default                                                                                                                                              |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>MonType</b>              | <b>Monx will equal sensor position expressed in percent assigned in the 4_LV_LM regulator where x = 1 to 8</b>                                                                                                                                  | <b>= 1_LMposition</b>                                                                                                                                              |
| LMPOSin                     | Maps RegxSenyPos in Dither rate in hertz.                                                                                                                                                                                                       | Reg1SenAPos,<br>Reg1SenBPos,<br>Reg1SenCPos,<br>Reg1SenDPos,<br>Reg2SenAPos,<br>Reg2SenBPos,<br>Reg2SenCPos,<br>Reg2SenDPos,<br>Unused<br>(Default-Unused)         |
| TMR_DiffLimt                | Diagnostic limit, TMR Input Vote difference in %                                                                                                                                                                                                | -10 to 150<br>(Default-5)                                                                                                                                          |
| <b>MonType</b>              | <b>Monx will equal sensor position expressed in Vrms assigned in the 4_LV_LM regulator where x = 1 to 8</b>                                                                                                                                     | <b>= 1_LMVRMS</b>                                                                                                                                                  |
| LMPOSin                     | Maps RegxSenyPos in Dither rate in hertz.                                                                                                                                                                                                       | Reg1SenAVrms,<br>Reg1SenBVrms,<br>Reg1SenCVrms,<br>Reg1SenDVrms,<br>Reg2SenAVrms,<br>Reg2SenBVrms,<br>Reg2SenCVrms,<br>Reg2SenDVrms,<br>Unused<br>(Default-Unused) |
| <b>MonType</b>              | <b>Monx will equal the scaled value from the LVDT assigned via LVDT1input where x = 1 to 8</b>                                                                                                                                                  | <b>= 1_LVposition</b>                                                                                                                                              |
| LVDT_Margin                 | Defines the over range in % for the LVDT input. A diagnostic is generated if this value is exceeded.                                                                                                                                            | 0 to 100 (Default-2)                                                                                                                                               |
| LVDTxinput<br>where x = 1   | LVDTx input selection                                                                                                                                                                                                                           | LVDT1, LVDT2, LVDT3,<br>LVDT4, LVDT5, LVDT6,<br>LVDT7, LVDT8, Unused<br>(Default-Unused)                                                                           |
| MaxPOSvalue                 | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150 (Default-100)                                                                                                                                           |
| MinPOSvalue                 | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150 (Default-0)                                                                                                                                             |
| MnLVDTx_Vrms<br>where x = 1 | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                                                                                                            |

| Parameter                        | Description                                                                                                                                                                                                                                     | Value Range / Default                                                              |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| MxLVDTx_Vrms<br>where x = 1      | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                            |
| <b>MonType</b>                   | <b>Monx will equal the maximum selected scaled value from two LVDTs assigned via LVDTyinput where x = 1 to 8 and y = 1 to 2.</b>                                                                                                                | <b>= 2_LVposMAX</b>                                                                |
| LVDT_Margin                      | Defines the over range in % for the LVDT input. A diagnostic is generated if this value is exceeded.                                                                                                                                            | 0 to 100 (Default-2)                                                               |
| LVDTxinput<br>where x = 1 to 2   | LVDTx input selection                                                                                                                                                                                                                           | LVDT1, LVDT2, LVDT3, LVDT4, LVDT5, LVDT6, LVDT7, LVDT8, Unused<br>(Default-Unused) |
| MaxPOSvalue                      | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)                                                        |
| MinPOSvalue                      | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)                                                          |
| MnLVDTx_Vrms<br>where x = 1 to 2 | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                            |
| MxLVDTx_Vrms<br>where x = 1 to 2 | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                            |
| TMR_DiffLimt                     | Diagnostic limit, TMR Input Vote difference in %                                                                                                                                                                                                | -10 to 150<br>(Default-5)                                                          |
| <b>MonType</b>                   | <b>Monx will equal the minimum selected scaled value from two LVDTs assigned via LVDTyinput where x = 1 to 8 and y = 1 to 2.</b>                                                                                                                | <b>= 2_LVposMIN</b>                                                                |
| LVDT_Margin                      | Defines the over range in % for the LVDT input. A diagnostic is generated if this value is exceeded.                                                                                                                                            | 0 to 100<br>(Default-2)                                                            |
| LVDTxinput<br>where x = 1 to 2   | LVDTx input selection                                                                                                                                                                                                                           | LVDT1, LVDT2, LVDT3, LVDT4, LVDT5, LVDT6, LVDT7, LVDT8, Unused<br>(Default-Unused) |
| MaxPOSvalue                      | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-100)                                                        |
| MinPOSvalue                      | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150<br>(Default-0)                                                          |
| MnLVDTx_Vrms<br>where x = 1 to 2 | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                            |
| MxLVDTx_Vrms<br>where x = 1 to 2 | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1<br>(Default-1)                                                            |
| TMR_DiffLimt                     | Diagnostic limit, TMR Input Vote difference in %                                                                                                                                                                                                | -10 to 150 (Default-5)                                                             |

| Parameter                        | Description                                                                                                                                                                                                                                     | Value Range / Default                                                           |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| <b>MonType</b>                   | <b>Monx will equal the median selected scaled value from three LVDTs assigned via LVDTyinput where x = 1 to 8 and y = 1 to 3.</b>                                                                                                               | <b>= 3_LVposMID</b>                                                             |
| LVDT_Margin                      | Defines the over range in % for the LVDT input. A diagnostic is generated if this value is exceeded.                                                                                                                                            | 0 to 100 (Default-2)                                                            |
| LVDTxinput<br>where x = 1 to 3   | LVDTx input selection                                                                                                                                                                                                                           | LVDT1, LVDT2, LVDT3, LVDT4, LVDT5, LVDT6, LVDT7, LVDT8, Unused (Default-Unused) |
| MaxPOSvalue                      | Position in Eng. units (usually %) at the maximum end stop of the valve.                                                                                                                                                                        | -15 to 150 (Default-100)                                                        |
| MinPOSvalue                      | Position in Eng. Units (usually %) at the minimum end stop of the valve.                                                                                                                                                                        | -15 to 150 (Default-0)                                                          |
| MnLVDTx_Vrms<br>where x = 1 to 3 | LVDTx Vrms at the minimum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1 (Default-1)                                                            |
| MxLVDTx_Vrms<br>where x = 1 to 3 | LVDTx Vrms at the maximum end stop of the valve. These values are normally set by the Auto-Calibrate function. For TMR, the first value is LVDTx Vrms from PSVO-R's perspective, the second from PSVO-S and the last from PSVO-T's perspective. | 0 to 7.1 (Default-1)                                                            |
| TMR_DiffLimt                     | Diagnostic limit, TMR Input Vote difference in %                                                                                                                                                                                                | -10 to 150 (Default-5)                                                          |

#### PSVO Variable Definitions

| Name                | Description                                             | Description Type               |
|---------------------|---------------------------------------------------------|--------------------------------|
| L3DIAG_PSVO         | PSVO I/O Diagnostic indication                          | Input non-voted Boolean-3 bits |
| LINK_OK_PSVO        | PSVO I/O Link OK indication                             | Input non-voted Boolean-3 bits |
| ATTN_PSVO           | PSVO I/O Attention indication                           | Input non-voted Boolean-3 bits |
| PS18V_PSVO          | PSVO I/O 18V Power Supply indication                    | Input non-voted Boolean-3 bits |
| PS28V_PSVO          | PSVO I/O 28V Power Supply indication                    | Input non-voted Boolean-3 bits |
| IOPack_Tmpr         | PSVO I/O Pack Temperature (deg F)                       | Analog Input non-voted Real    |
| Rx_SuicideNV        | ServoOutputx Suicide relay status where x = 1 or 2      | Input non-voted Boolean-3 bits |
| RegxFbkFail         | Regulator x feedback fault status where x = 1 or 2      | Input voted Boolean            |
| RegxSensorSpreadAlm | Regulator x Sensor Spread Alarm status where x = 1 or 2 | Input voted Boolean            |
| Reg1Suicide         | ServoOutput1 Suicide relay status                       | Input voted Boolean            |
| Reg2Suicide         | ServoOutput2 Suicide relay status                       | Input voted Boolean            |
| Reg1_PosAFlt        | Regulator 1 4_LV_LM Position A failure                  | Input voted Boolean            |
| Reg2_PosAFlt        | Regulator 2 4_LV_LM Position A failure                  | Input voted Boolean            |
| Reg1_PosBFlt        | Regulator 1 4_LV_LM Position B failure                  | Input voted Boolean            |
| Reg2_PosBFlt        | Regulator 1 4_LV_LM Position B failure                  | Input voted Boolean            |
| Reg1_PosDif1        | Regulator 1 4_LV_LM Position Difference 1 failure       | Input voted Boolean            |
| Reg2_PosDif1        | Regulator 2 4_LV_LM Position Difference 1 failure       | Input voted Boolean            |
| Reg1_PosDif2        | Regulator 1 4_LV_LM Position Difference 2 failure       | Input voted Boolean            |
| Reg2_PosDif2        | Regulator 2 4_LV_LM Position Difference 2 failure       | Input voted Boolean            |

| Name                     | Description                                                                                       | Description Type            |
|--------------------------|---------------------------------------------------------------------------------------------------|-----------------------------|
| Reg1SenAFlt              | Regulator 1 Sensor A fault                                                                        | Input voted Boolean         |
| Reg1SenBFlt              | Regulator 1 Sensor B fault                                                                        | Input voted Boolean         |
| Reg1SenCFlt              | Regulator 1 Sensor C fault                                                                        | Input voted Boolean         |
| Reg1SenDFlt              | Regulator 1 Sensor D fault                                                                        | Input voted Boolean         |
| Reg2SenAFlt              | Regulator 2 Sensor A fault                                                                        | Input voted Boolean         |
| Reg2SenBFlt              | Regulator 2 Sensor B fault                                                                        | Input voted Boolean         |
| Reg2SenCFlt              | Regulator 2 Sensor C fault                                                                        | Input voted Boolean         |
| Reg2SenDFlt              | Regulator 2 Sensor D fault                                                                        | Input voted Boolean         |
| RegCalMode               | Regulator under Calibration                                                                       | Input voted Boolean         |
| Reg1SenA2LVSumFlt        | Regulator 1 Sensor A 2LV Summation Fault                                                          | Input voted Boolean         |
| Reg1SenB2LVSumFlt        | Regulator 1 Sensor B 2LV Summation Fault                                                          | Input voted Boolean         |
| Reg2SenA2LVSumFlt        | Regulator 2 Sensor A 2LV Summation Fault                                                          | Input voted Boolean         |
| Reg2SenB2LVSumFlt        | Regulator 2 Sensor B 2LV Summation Fault                                                          | Input voted Boolean         |
| Reg1_Fdbk                | Regulator 1 position feedback                                                                     | Analog Input voted REAL     |
| Reg2_Fdbk                | Regulator 2 position feedback                                                                     | Analog Input voted REAL     |
| MiscFdbk1a               | Regulator 1 Position A when 4_LV_LM,<br>Pilot when one of the Pilot Cylinder regs.                | Analog Input voted REAL     |
| MiscFdbk1b               | Regulator 1 Position B when 4_LV_LM,<br>Pilot when one of the Pilot Cylinder regs.                | Analog Input voted REAL     |
| MiscFdbk2a               | Regulator 2 Position A when 4_LV_LM,<br>Pilot when one of the Pilot Cylinder regs.                | Analog Input voted REAL     |
| MiscFdbk2b               | Regulator 2 Position B when 4_LV_LM,<br>Pilot when one of the Pilot Cylinder regs.                | Analog Input voted REAL     |
| Reg1_Error               | Position error for the Regulator 1 position loops and<br>pulse rate error for the Pulse Rate reg. | Analog Input voted REAL     |
| Reg2_Error               | Position error for the Regulator 2 position loops and<br>pulse rate error for the Pulse Rate reg. | Analog Input voted REAL     |
| Accel1                   | Acceleration value of the card point FlowRate1                                                    | Analog Input voted REAL     |
| Accel2                   | Acceleration value of the card point FlowRate2                                                    | Analog Input voted REAL     |
| Monx<br>where x = 1 to 8 | Value assigned to Monx based on configuration<br>parameters found in the Monitor Tab.             | Analog Input voted REAL     |
| Excit_Monx               | Excitation Monitor x (Vrms) where x = 1 or 2                                                      | Analog Input voted REAL     |
| Reg1FdbkSelState         | 3LVLMX or 4LVLMX Regulator 1 Sensor Tri-select<br>State                                           | Input DINT                  |
| Reg2FdbkSelState         | 3LVLMX or 4LVLMX Regulator 2 Sensor Tri-select<br>State                                           | Input DINT                  |
| ServoOutxNV              | Servo Output x measured current (%) where x = 1 or 2                                              | Analog Input non-voted Real |
| ServoxMonitorNV          | Servo x AvSelection Monitor where x = 1 or 2                                                      | Analog Input non-voted Real |
| CalibEnab1               | Enable Calibration Regulator 1                                                                    | Output Boolean              |
| CalibEnab2               | Enable Calibration Regulator 2                                                                    | Output Boolean              |
| SuicidForcex             | Force Suicide on Servo x where x = 1 or 2                                                         | Output Boolean              |
| PosDiffEnabx             | Position Difference Enable for Regulator 1 when<br>configured as 4_LV_LM where x = 1 or 2         | Output Boolean              |
| Reg1SenxFReq             | Force a Sensor A fault on Regulator 1 configured as<br>4LVLMX or 3LVLMX where x = A, B, C & D     | Output Boolean              |
| Reg2SenxFReq             | Force a Sensor A fault on Regulator 2 configured as<br>4LVLMX or 3LVLMX where x = A, B, C & D     | Output Boolean              |
| XSuicServo1              | X pack Force Suicide for Servo 1 where X = R, S & T                                               | Output Boolean              |
| XsuicServo2              | X pack Force Suicide for Servo 2 where X = R, S & T                                               | Output Boolean              |
| Regx_Ref                 | Regulator x Position reference (%) where x = 1 or 2                                               | Output Boolean              |
| Regx_NullCor             | Regulator x Null Bias Correction (%) where x = 1 or 2                                             | Output Boolean              |

# Alarms

## PSVO Specific Alarms

| Alarm ID | Alarm Description                                     | Possible Cause                                                                                                                                                                                                                        | Solution                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 33-40    | Lvdt #[ ] rms voltage for Regulator [ ] out of limits | Excitation to LVDT, bad transducer, or open or short-circuit OR LVDT [ ] input to the analog to digital converter exceeded the converter limits. LVDT scaling configuration (MnLVDT[ ]_Vrms, MxLVDT[ ]_Vrms) has not been calibrated. | Check field wiring including shields & LVDT Excitation. Problem is usually not a PSVO or terminal board failure if other LVDT inputs are working correctly. Calibrate regulator with the proper LVDTs. Verify the configuration limits, MnLVDT[ ]_Vrms and MxLVDT[ ]_Vrms for the affected regulator.                                                                                                                                                                         |
| 45       | Calibration Mode Enabled                              | The variable CalibEnab# is set to True and user has selected the "Calibration Mode" button in the "Calibrate Valve" dialog.                                                                                                           | This alarm is an indication that there is a regulator that is in Calibration mode.                                                                                                                                                                                                                                                                                                                                                                                            |
| 46       | PSVO card not online, Servos Suicided                 | The servo outputs have been suicided because the IOPack has gone off-line.                                                                                                                                                            | Verify that the controller is online. Verify that network connections to the pack are ok.                                                                                                                                                                                                                                                                                                                                                                                     |
| 47-48    | Servo current #[ ] disagrees w/ ref, Suicided         | Servo current feedback doesn't match servo current command within specified (Cur_Suicide) percentage and EnablCurSuic is enabled. Possible current transient. Servo is not tuned correctly (Regulator gain too low).                  | Possible open circuit in servo current loop. Check field wiring. Verify proper setting of configuration parameters and tuning of servo.                                                                                                                                                                                                                                                                                                                                       |
| 52-53    | Servo current #[ ] short circuit                      | Servo short circuit detection is enabled (ShrtCoildiag) and low resistance was measured. Possible shorted servo coil. Shorted coil threshold (RcoilShort) or shorted coil time limit (RShrtTimeLim) is set incorrectly.               | Measure servo ohm value to verify that it is the proper value. Verify RcoilShort is set to proper value. Re-calibrate. Verify Servo_MA_Out parameter is set to proper current setting. Verify terminal board jumpers match configuration. Set AV_Selector to the value Coil_OHMS (build/download) and view the measured coil resistance displayed in Servo#MonitorNV_R,S,T. Verify that the measured resistance matches actual coil resistance and is above RcoilShort value. |
| 57-58    | Servo current #[ ] open circuit                       | Servo short circuit detection is enabled (OpenCoildiag) and low resistance was measured. Possible open servo coil. Open coil threshold (RcoilOpen) or open coil time limit (RopenTimeLim) is set incorrectly.                         | Check field wiring for possible open circuit. Measure servo ohm value to verify that it is the proper value. Verify RcoilOpen is set to proper value. Re-calibrate. Set AV_Selector to the value Coil_OHMS (build/download) and view the measured coil resistance displayed in Servo#MonitorNV_R,S,T. Verify that the measured resistance matches actual coil resistance and is below RcoilOpen value.                                                                        |
| 62-63    | Servo posit. #[ ] fdbk out of range, Suicided         | LVDT position feedback is outside of the specified range. LVDT inputs have not been calibrated or Vrms limits are incorrect.                                                                                                          | Check the LVDT configuration settings, calibration, field wiring.                                                                                                                                                                                                                                                                                                                                                                                                             |
| 67-68    | ConfigMsg error for regulator #[ ]                    | Configuration settings are incorrect for specified regulator type.                                                                                                                                                                    | Verify regulator configuration settings. Verify that Max/Min limits are correct for selected regulator type. Verify that the configured regulators are used by the proper servos.                                                                                                                                                                                                                                                                                             |
| 72       | On card calibration voltage range fault               | On board voltage reference values are out of range.                                                                                                                                                                                   | Replace IOPack hardware.                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

| Alarm ID | Alarm Description                            | Possible Cause                                                                                                                                                | Solution                                                                                                                                                   |
|----------|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 73-74    | Lvdt excitation #[ ]<br>voltage out of range | Possible short in excitation voltage.<br>Excitation voltage is too low.                                                                                       |                                                                                                                                                            |
| 77       | Servo Output<br>Assignment<br>Mismatch       | Regulator types 2_LVpilotCyl and<br>4_LVp/cylMAX require that 2 servos are<br>assigned to the regulator. These servos<br>must match in configured parameters. | Verify that both servos specify the<br>configured regulator.<br>Verify servo configuration parameters<br>(Servo_MA_Out) are both set to the same<br>value. |
| 78       | R Detects S<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 78       | S Detects R<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 78       | T Detects R<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 79-80    | R Detects S<br>ComError on channel<br>[ ]    | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 79-80    | S Detects R<br>ComError on channel<br>[ ]    | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 79-80    | T Detects R<br>ComError on channel<br>[ ]    | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 81       | R Detects T<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 81       | S Detects T<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 81       | T Detects S<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 82-83    | R Detects T<br>ComError on channel<br>[ ]    | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 82-83    | S Detects T<br>ComError on channel<br>[ ]    | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 82-83    | T Detects S<br>ComError on channel<br>[ ]    | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 84       | R Detects R<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 84       | S Detects S<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 84       | T Detects T<br>ComFailure on<br>channels 1+2 | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |
| 85-86    | R Detects R<br>ComError on channel<br>[ ]    | Communication to specified pack has<br>failed. Specified pack has rebooted or is<br>not connected                                                             |                                                                                                                                                            |

| Alarm ID | Alarm Description                                   | Possible Cause                                                                                                                               | Solution                                                                                                            |
|----------|-----------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| 85-86    | S Detects S ComError on channel [ ]                 | Communication to specified pack has failed. Specified pack has rebooted or is not connected                                                  |                                                                                                                     |
| 85-86    | T Detects T ComError on channel [ ]                 | Communication to specified pack has failed. Specified pack has rebooted or is not connected                                                  |                                                                                                                     |
| 90-97    | Power supply [ ] V is out of range, voltage = [ ]   | The specified internal power supply voltage is incorrect.                                                                                    |                                                                                                                     |
| 100-107  | Lvdt #[ ] rms voltage for Monitor [ ] out of limits | LVDT position feedback for Monitor [ ] is outside of the specified range. LVDT inputs have not been calibrated or Vrms limits are incorrect. | Check the LVDT configuration settings, field wiring. Verify proper Vrms monitor limits.                             |
| 108-109  | Lvdt Config error on Regulator #[ ]                 | For regulators 4_LV_LM and 4_LV_LMX, the configured LVDT Vrms limits are configured incorrectly for ratiometric LVDTs.                       | Verify that ratiometric LVDT pairs have opposite Vrms value in the Min/Max limits.                                  |
| 110-111  | Servo Coil #[ ] not within resistance limits        | During calibration, the measured servo coil resistance was out of range.                                                                     | Verify that Servo_MA_Out setting matches terminal board jumpers. Verify servo coil resistance. Verify field wiring. |
| 112-119  | Regulator #[ ] Sensor #[ ] out of range             | The regulator position sensor LVDT is out of the specified range.                                                                            | Check the LVDT configuration settings, field wiring. Verify proper Vrms monitor limits.                             |
| 120-121  | Servo #[ ] Suicided                                 | The servo is suicided.                                                                                                                       |                                                                                                                     |

### ***I/O Pack Alarms***

| Fault | Fault Description                                         | Possible Cause                                                                                                                                            |
|-------|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                  | Board firmware programming error (board will not go online)                                                                                               |
| 3     | CRC failure override is active                            | Board firmware programming error (board is allowed to go online)                                                                                          |
| 4     | I/O pack in stand alone mode                              | Invalid command line option                                                                                                                               |
| 5     | I/O pack in remote I/O mode                               | Invalid command line option                                                                                                                               |
| 6     | Special user mode active. Now [ ]                         | Invalid command line option                                                                                                                               |
| 7     | I/O pack – The I/O pack has gone to the offline state     | Lost communication with controller                                                                                                                        |
| 16    | System limit checking is disabled                         | System checking was disabled by configuration                                                                                                             |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                  | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                      | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                | Supply voltage below 26.5 V dc                                                                                                                            |
| 257   | I/O pack power supply voltage is low                      | Supply voltage below 18 V dc                                                                                                                              |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                |
| 261   | Unable to read configuration file from flash              | Need to download configuration to the pack                                                                                                                |
| 262   | Bad configuration file detected                           | Configuration file not compatible, re-download                                                                                                            |
| 263   | I/O pack configuration – bad name detected                | Wrong configuration file for I/O pack                                                                                                                     |
| 264   | I/O pack configuration – bad config compatibility code    | Wrong configuration revision for I/O pack                                                                                                                 |
| 265   | I/O pack mapper – EGD header size mismatch                | Controller EGD revision code not supported                                                                                                                |
| 266   | I/O pack configuration – configuration size mismatch      | Incorrect configuration file size received                                                                                                                |
| 267   | FPGA – name mismatch detected                             | Wrong configuration for FPGA in I/O pack                                                                                                                  |

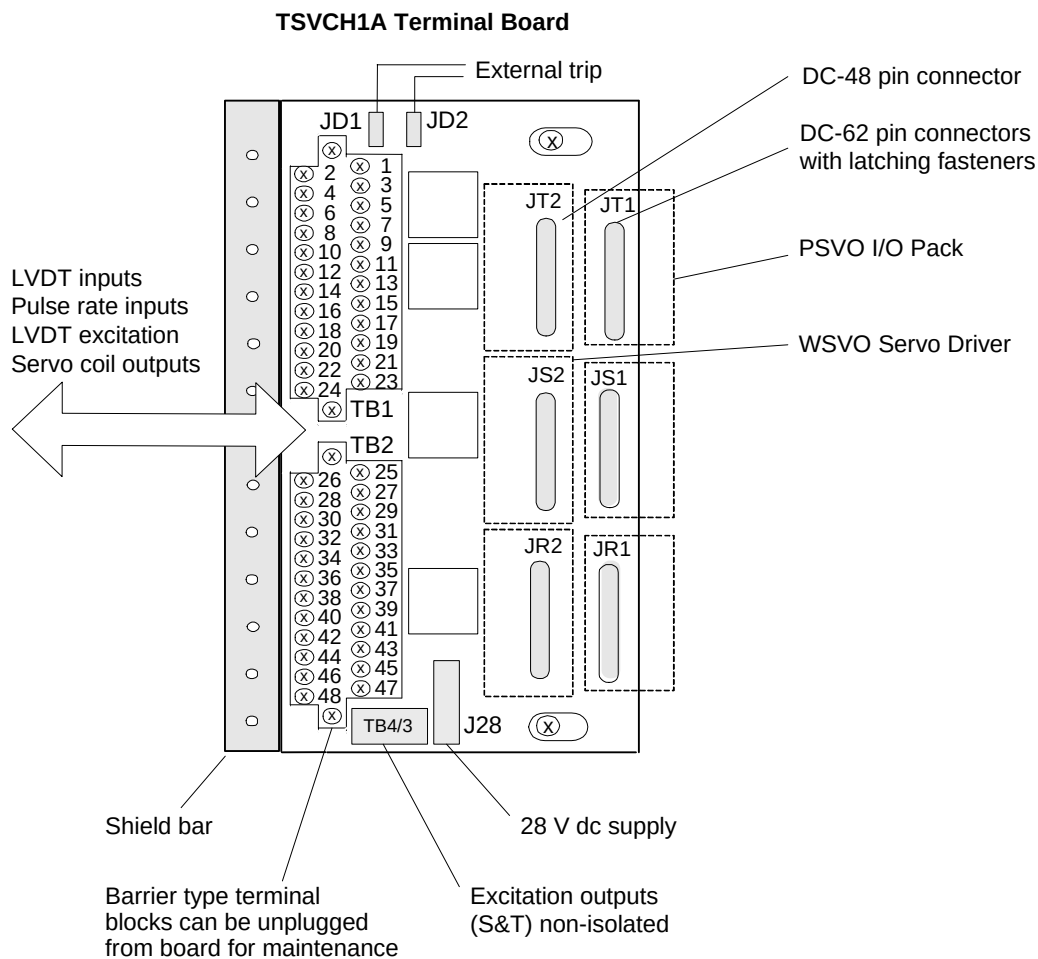


| <b>Fault</b> | <b>Fault Description</b>                                                    | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 268          | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                         |
| 269          | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                   |
| 270          | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                |
| 271          | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                        |
| 272          | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                           |
| 273          | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                            |
| 274          | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                    |
| 275          | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                            |
| 276          | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                |
| 277          | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                |
| 278          | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                           |
| 293          | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                             |
| 301          | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                |
| 314          | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                           |
| 315          | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                             |
| 316          | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected         |
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ]             | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                                   | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated                           | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                             | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch                          | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                             | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                                    | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                                  | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                                | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                             | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                               | Config Shmem CRC changed                                                                |

# TSVC Servo Input/Output

## Functional Description

The Servo Input/Output (TSVC) terminal board interfaces to two electro-hydraulic servo valves that actuate the steam/fuel valves. Valve position is measured with linear variable differential transformers (LVDT). TSVC is designed specially for the PSVO I/O pack and the WSVO servo driver, and will not work with the VSVO processor. The terminal board supports simplex, dual, and TMR control. Three 28 V dc supplies come in through plug J28. Plugs JD1 or JD2 are for an external trip from the protection module.

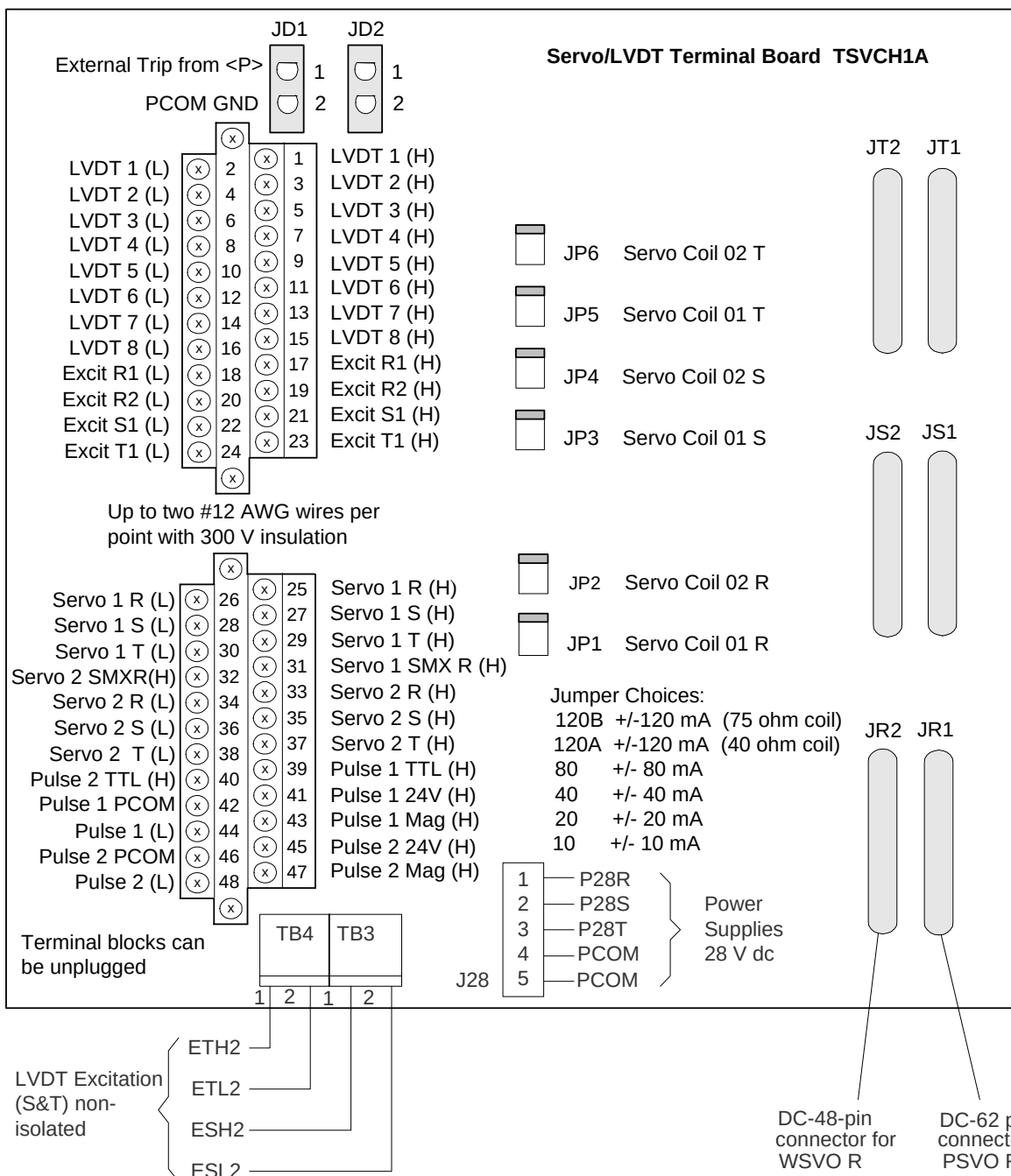


TSVC Servo Terminal Board

## Installation

Sensors and servo valves are wired directly to two I/O terminal blocks. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wiring. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block. External trip wiring is plugged into either JD1 or JD2.

Each servo output can have three coils in TMR configuration. The size of each coil current is jumper selected using JP1, 3, 5 for Servo 1, and JP2, 4, 6 for servo 2.



*Servo/LVDT Terminal Board Wiring*

Three 28 V dc power supplies for the R, S, and T board functions are connected to J28. Two non-isolated LVDT excitations sources for S and T are wired to terminal block TB3 and TB4.

## **PSVO**

The three J1 connectors for the PSVO I/O packs are <R>, <S>, and <T>. These plug into the DC-37 pin connector with latching fasteners, and bolt to a side bracket holding the packs in place.

## **WSVO**

The three J2 connectors for the WSVO servo drivers are R, S, and T. Each WSVO is held down with four screws. The WSVO servo driver and PSVO I/O pack are ordered as a set and should be replaced if diagnostics indicate a servo problem.

The PSVO pack and WSVO driver can be replaced with the unit running by removing power from the failed channel with the corresponding manual enable switch, SW1, or SW2, or SW3. Power to each channel is indicated with LEDs on the board and LEDs on each solid-state power switch.

## **Operation**

The TSVC servo terminal board provides two channels consisting of bi-directional servo current outputs, LVDT position feedback, LVDT excitation, and pulse rate flows inputs. It provides excitation for, and accepts inputs from, up to eight LVDT valve position inputs. There is a choice of one, two, three, or four LVDTs for each servo control loop. The two pulse rate inputs are used for gas turbine fuel flow measurement.

Each servo output is equipped with an individual suicide relay under firmware control that shorts the PSVO output signal to signal common when de-energized, and recovers to nominal limits after a manual reset command is issued. Diagnostics monitor the output status of each servo voltage, current, and suicide relay.

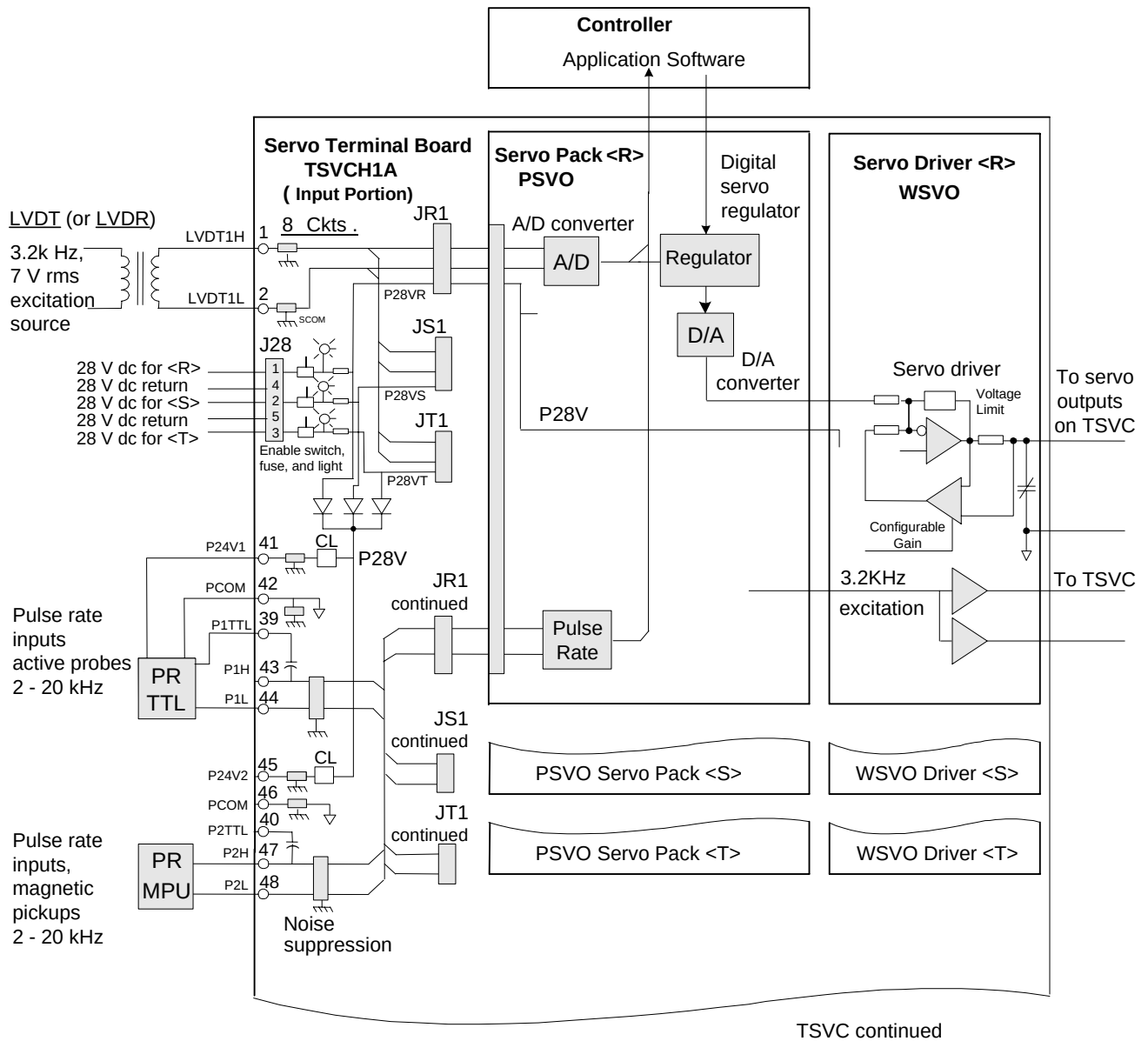
Each of the servo output channels can drive either one or two-coil servos in simplex applications, or two or three-coil servos in TMR applications. The two-coil TMR applications are for 200# oil gear systems where each of two control pack drive one coil each, and the third control pack has no servo coil interface. Servo cable lengths up to 300 m (984 ft) are supported with a maximum two-way cable resistance of 15  $\Omega$ . Since there are many types of servo coils, a variety of bi-directional current sources are jumper selectable.

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**Note** The primary and emergency overspeed systems will trip the hydraulic solenoids independent of this circuit

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A trip override relay K1 is provided on the terminal board, which is driven from the <P> protection pack. If an emergency overspeed condition is detected in the protection module, the K1 relay will energize and disconnect the servo output and apply a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high, and is functional only with respect to the servo coils driven from <R>.

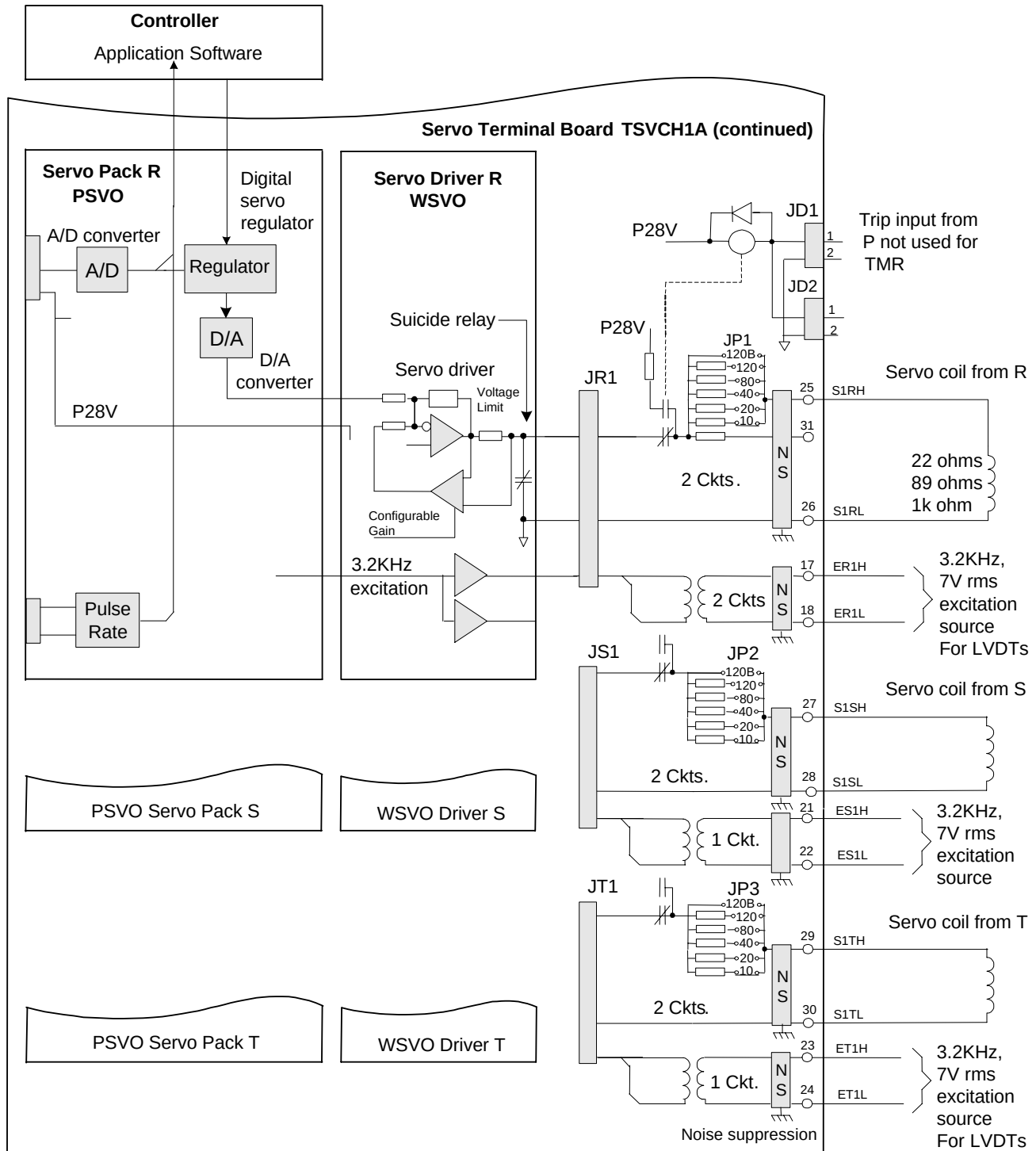


LVDT and Pulse Rate Inputs (Part 1 of 2)

**Note** Only two pulse rate probes on one TSVC are used.

In TMR applications, the LVDT signals fan out to three packs through JR1, JS1, and JT1. Three connectors also bring power into TSVC where the three voltages are diode high-selected and current limited to supply 24 V dc to the pulse rate active probes.

For TMR systems, each servo channel has connections to three output coils with a range of current ratings up to 120 mA, selected by jumper.



TSVC Servo Coil Outputs and LVDT Excitation (Part 2 of 2)

| Jumper Label<br>Coil Type | Nominal<br>Current | Coil<br>Resistance<br>(Ohms) | Internal<br>Resistance (Ohms) | Application     |
|---------------------------|--------------------|------------------------------|-------------------------------|-----------------|
| 101                       | ±10 mA             | 1,000                        | 180                           | Simplex and TMR |
| 202                       | ± 20 mA            | 125                          | 442                           | Simplex         |
| 403                       | ± 40 mA            | 62                           | 195                           | Simplex         |
| 404                       | ± 40 mA            | 89                           | 195                           | TMR             |
| 805                       | ± 80 mA            | 22                           | 115                           | TMR             |
| 120A6                     | ± 120 mA (A)       | 40                           | 46                            | Simplex         |
| 120B7                     | ± 120 mA (B)       | 75                           | 10                            | TMR             |

The table above defines the standard servo coil resistance and their associated internal resistance, selected with the terminal board jumpers shown in the figure. In addition to these standard servo coils, it is possible to drive non-standard coils by using a non-standard jumper setting. For example, an 80 mA, 125  $\Omega$  coil could be driven by using a jumper setting 120B.

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**Note** The excitation source is isolated from signal common (floating) and is capable of operation at common mode voltages up to 35 V dc, or 35 V rms, 50/60 Hz.

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Control valve position is sensed with either a four-wire LVDT or a three-wire linear variable differential reluctance (LVDR). Redundancy implementations for the feedback devices is determined by the application software to allow the maximum flexibility. LVDT/Rs can be mounted up to 300 m (984 ft) from the turbine control with a maximum two-way cable resistance of 15  $\Omega$ .

Two LVDT/R transformer isolated excitation sources are located on the terminal board for simplex applications and another two transformer isolated excitation sources for TMR applications. A fifth and sixth non-isolated excitation source are provided for the customer's use. Excitation voltage is 7 V rms and the frequency is 3.2 kHz with a total harmonic distortion of less than 1% when loaded.

A typical LVDT/R has an output of 0.7 V rms at the zero stroke position of the valve stem, and an output of 3.5 V rms at the designed maximum stroke position (some applications have these reversed). The LVDT/R input is converted to dc and conditioned with a low pass filter. Diagnostics perform a high/low (hardware) limit check on the input signal and a high/low system (software) limit check.

Inputs support both passive magnetic pickups and active pulse rate transducers (TTL type) interchangeable without configuration. Normally, these inputs are not used on steam turbine applications, but are usually for liquid fuel flow measurement, and monitoring flow divider feedback in gas turbine applications. Pulse rate inputs can be located up to 300 m (984 ft) from the turbine control cabinet. This assumes shielded-pair cable is used with typically 70 nF single ended or 35 nF differential capacitance and 15  $\Omega$  resistance.

A frequency range of 2 to 30 kHz can be monitored at a normal sampling rate of either 10 or 20 ms. Magnetic pickups typically have an output resistance of 200  $\Omega$  and an inductance of 85 MHz excluding cable characteristics. The transducer is a high-impedance source, generating energy levels insufficient to cause a spark.

## ***Specifications***

| <b>Item</b>               | <b>Specification</b>                                                                                                                                                                                                                                       |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs          | Eight LVDT windings<br>Two pulse rate signals, magnetic or TTL<br>External trip signal to shut off servo outputs                                                                                                                                           |
| Number of outputs         | Two servo valves, three coils each, $\pm(10, 20, 40, 80, 120)$ mA<br>Four excitation sources for LVDTs (transformer isolation)<br>Two excitation sources for LVDTs (no transformer isolation)<br>Two 24 V dc excitation sources for pulse rate transducers |
| Power supply voltage      | Nominal 24 V dc from three supplies P28R, P28S, P28T                                                                                                                                                                                                       |
| Power supply current      | 5 A dc (Poly-Fuse or current limit rating for each input is 1 A dc)                                                                                                                                                                                        |
| LVDT excitation output    | Frequency of $3.2 \pm 0.2$ kHz<br>Voltage of $7.00 \pm 0.14$ V rms                                                                                                                                                                                         |
| Pulse rate input          | Minimum signal for proper measurement at 2 Hz is 33 mVpk, and at 12 kHz is 827 mVpk                                                                                                                                                                        |
| Magnetic PR pickup signal | Generates 150 V p-p into $60 \Omega$                                                                                                                                                                                                                       |
| Active PR pickup signal   | Generates 5 to 27 V p-p into $60 \Omega$                                                                                                                                                                                                                   |
| Fault detection           | Servo current out of limits or not responding<br>Regulator feedback signal out of limits<br>Failed ID chip                                                                                                                                                 |
| <b>Physical</b>           |                                                                                                                                                                                                                                                            |
| Size                      | 33.02 cm high x 17.8 cm wide (13 in x 7 in)                                                                                                                                                                                                                |
| Technology                | Surface-mount                                                                                                                                                                                                                                              |
| Temperature               | Operating: $-30$ to $65^{\circ}\text{C}$ ( $-22$ to $+149^{\circ}\text{F}$ )                                                                                                                                                                               |

## ***Diagnostics***

PSVO makes diagnostic checks on the terminal board components as follows:

- The output servo current is out of limits or not responding, creating a fault.
- The regulator feedback (LVDT) signal is out of limits, creating a fault. If the associated regulator has two sensors, the bad sensor is removed from the feedback calculation and the good sensor is used.
- If any one of the above signals go unhealthy a composite diagnostic alarm, L#DIAG\_PSVO occurs. Details of the individual diagnostics are available from the ToolboxST\* application. The diagnostic signals can be individually latched, and reset with the RESET\_DIA signal if they go healthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O processor. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the J connector location. When this chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.



## Configuration

In a simplex system, servo 1 is configured for the correct coil current with jumper JP1, and servo 2 is configured with jumper JP4. In a TMR system, each servo output can have three coils. In this case, each coil current is jumper selected using JP 1-3 for servo 1, and JP 4-6 for servo 2. All other servo board configuration is done from the ToolboxST application.

Power must be applied to the three channels, so check that all three switches SW1, SW2, and SW3 are ON, and the power indicators for P28R, S, and T are lit.

## Alarms

| Fault | Fault Description                                                                                                                        | Possible Cause                                                       |
|-------|------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|
| 32    | LVDT [ ] rms voltage out of limits.                                                                                                      |                                                                      |
| 33    | PSVO card not online, servos suicided.                                                                                                   |                                                                      |
| 34    | Servo current [ ] disagrees with reference, suicided.                                                                                    |                                                                      |
| 35    | Servo current [ ] short circuit.                                                                                                         |                                                                      |
| 36    | Servo current [ ] open circuit. The servo voltage is greater than 5V and the measured current is less than 10%.                          | A cable/wiring open circuit, or board problem.                       |
| 37    | Servo position [ ] feedback out of range, suicided. regulator number [ ] position feedback is out of range, causing the servo to suicide | LVDT or board problem                                                |
| 41    | LVDT excitation [ ] voltage out of range.                                                                                                |                                                                      |
| 279   | System could not determine platform type from hardware.                                                                                  | Board Ids not programmed. Pack is plugged into wrong terminal board. |

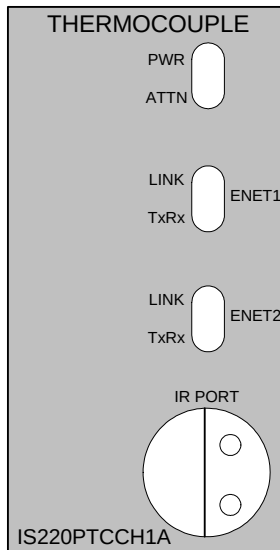
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## ***Notes***

# PTCC Thermocouple Input

## PTCC Thermocouple Input

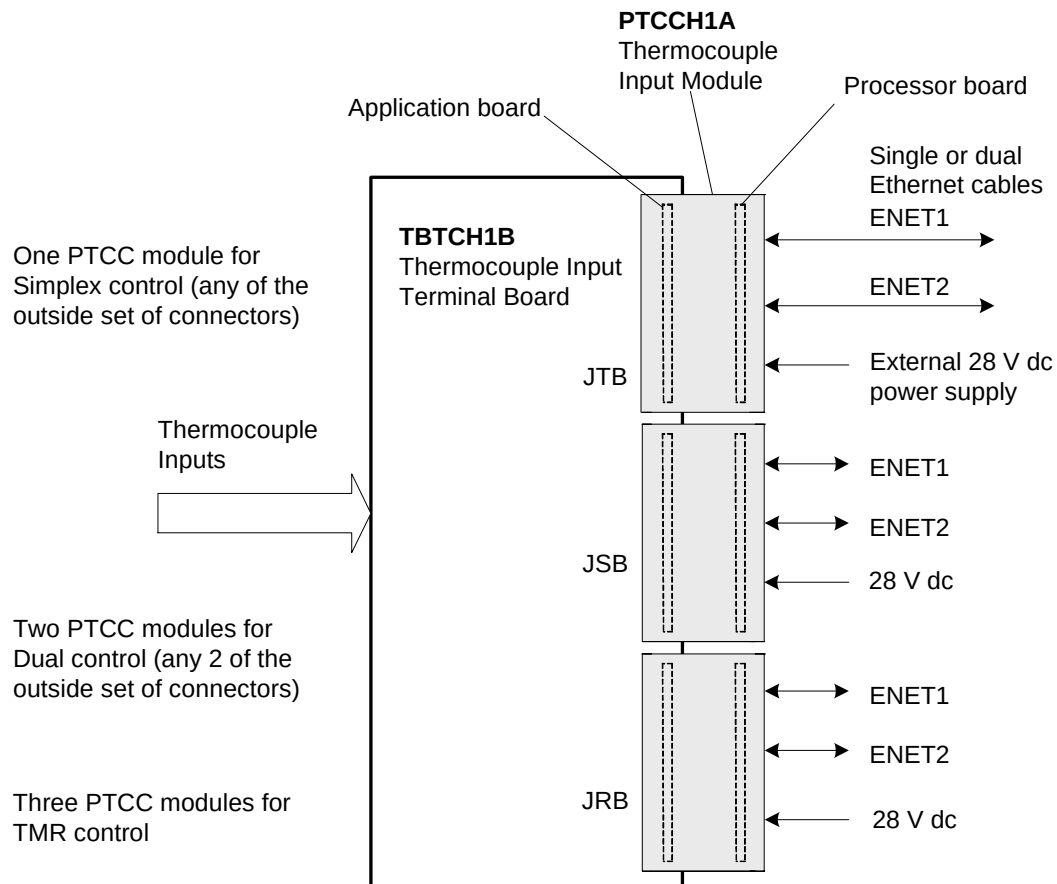
### Functional Description



The Thermocouple Input (PTCC) pack provides the electrical interface between one or two I/O Ethernet networks and a thermocouple input terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs and an acquisition board specific to the thermocouple input function. The pack is capable of handling up to 12 thermocouple inputs. Two packs can handle 24 inputs on TBTCH1C. In the TMR configuration with the TBTCH1B terminal board, three packs are used with three cold junctions, but only 12 thermocouples are available. Input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Output is through a DC-37 pin connector that mates directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.

PTCCH1 supports E,J,K,S,T types of standard thermocouples and mV inputs. The mV span is  $-8\text{mV}$  to  $+45\text{mV}$ .

PTCCH2 supports E,J,K,S,T as well as B, N and R types of standard thermocouples and mV inputs. The mV span for PTCCH2 is  $-20\text{mV}$  to  $+95\text{mV}$ .



## Compatibility

PTCCH1A/PTCCH2A is compatible with the thermocouple input terminal board TBTC, and the STTC board, but not the DIN-rail mounted DTTC board. The following table gives details of the compatibility.

| Terminal Board   | TBTC                                |                 |                 | STTC            |
|------------------|-------------------------------------|-----------------|-----------------|-----------------|
| Version & Inputs | TBTCH1B (12 TC)<br>TBTCH1C (24 TC)* | TBTCH1B (12 TC) | TBTCH1B (12 TC) | STTCH1A (12 TC) |
| Control Mode     | Simplex - Yes                       | Dual - Yes      | TMR - Yes       | Simplex - Yes   |

\*Support of 24 thermocouple inputs on TBTC requires the use of two PTCC packs.

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

## Installation

### ➤ To install the PTCC pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PTCC I/O pack for simplex or three PTCC I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC37 connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.

---

**Note** The PTCC mounts directly to a Mark VIe terminal board. Simplex terminal boards (TBTCH1C) have two DC-37 pin connectors that receive the PTCC, one for each set of 12 TC inputs. TMR capable terminal boards (TBTCH1B) have three DC-37 pin connectors. These can be used in dual mode if two packs are installed, and in simplex mode if only one PTCC is installed. The PTCC directly supports all of these connections.

---

# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

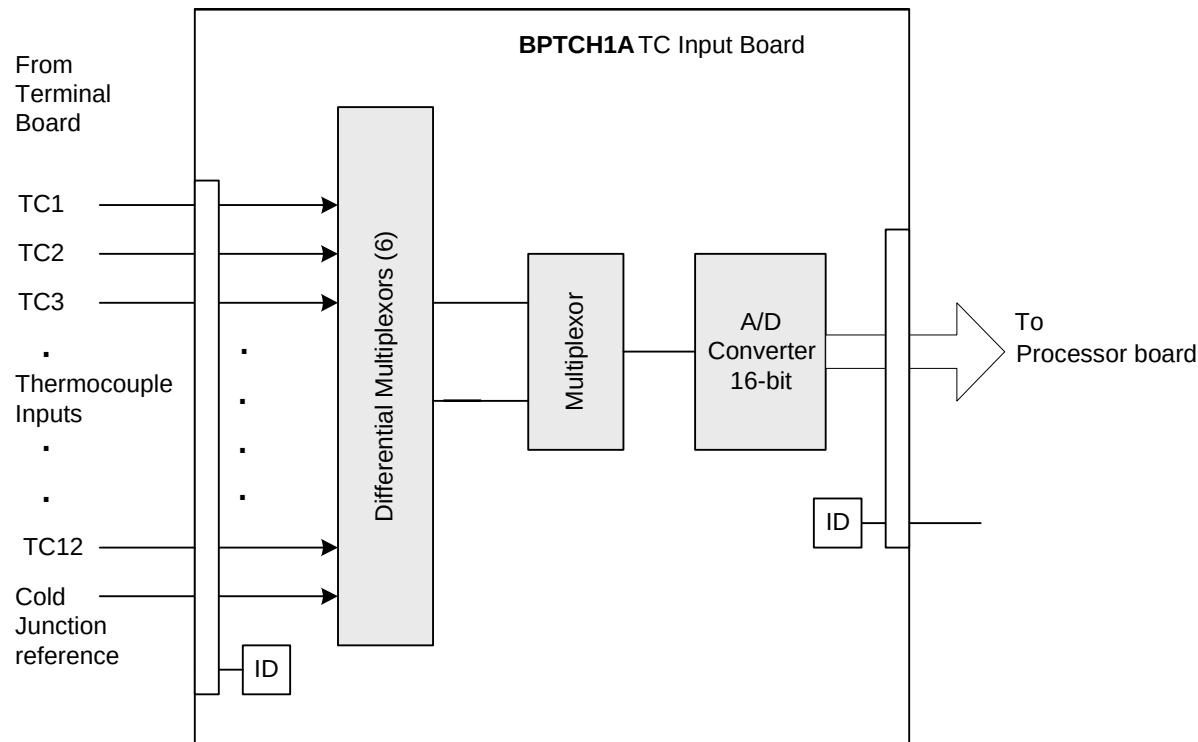
An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## **Analog Input Hardware**

The PTCC input board accepts 12 signals at mV levels from the thermocouples wired to the terminal board. The analog input section consists of six differential multiplexers, a main multiplexer, and a 16-bit analog to digital converter that sends the digital data to the adjacent processor board. Each input has hardware and firmware filters, and the converter samples at up to 120 Hz.

Type E, J, K, S, and T thermocouples can be used with PTCCH1, and they can be grounded or ungrounded. Type E, J, K, S, T, B, N and R thermocouples can be used with PTCCH2, and they can be grounded or ungrounded. Thermocouples can be located up to 300 meters (984 feet) from the turbine I/O panel with a maximum two-way cable resistance of 450 Ω.

Linearization for individual thermocouple types is performed in software by the I/O pack board. A thermocouple, which is determined to be out of the hardware limits, is removed from the scanned inputs in order to prevent adverse affects on other input channels. If two packs are used, and both Cold Junction (CJ) devices are within the configurable limits, then the average of the two is used for CJ compensation.



### Thermocouple Limits

#### TBTC with PTCCH1 or VTCC

Thermocouple inputs support a full-scale input range of -8.0 mV to + 45.0 mV. The following table shows typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from -30 to 65°C (-22 to +149 °F).

| Thermocouple Type PTCCH1                        | E      | J      | K      | S      | T      |
|-------------------------------------------------|--------|--------|--------|--------|--------|
| Low range, °F                                   | -60    | -60    | -60    | 0      | -60    |
| °C                                              | -51    | -51    | -51    | -17.78 | -51    |
| mV at low range with reference at 70°C (158 °F) | -7.174 | -6.132 | -4.779 | -0.524 | -4.764 |
| High range, °F                                  | 1100   | 1400   | 2000   | 3200   | 750    |
| °C                                              | 593    | 760    | 1093   | 1760   | 399    |
| mV at high range with reference at 0°C (32 °F)  | 44.547 | 42.922 | 44.856 | 18.612 | 20.801 |

## TBTC with PTCCH2

Thermocouple inputs support a full-scale input range of -20.0 mV to + 95.0 mV. The following table shows typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from -30 to 65°C (-22 to +149 °F).

| Thermocouple Type PTCCH2                        | E      | J      | K      | S      | T      |
|-------------------------------------------------|--------|--------|--------|--------|--------|
| Low range, °F                                   | -60    | -60    | -60    | 0      | -60    |
| °C                                              | -51    | -51    | -51    | -17.78 | -51    |
| mV at low range with reference at 70°C (158 °F) | -7.174 | -6.132 | -4.779 | -0.524 | -4.764 |
| High range, °F                                  | 1832   | 2192   | 2372   | 3200   | 752    |
| °C                                              | 1000   | 1200   | 1300   | 1760   | 400    |
| mV at high range with reference at 0°C (32 °F)  | 76.373 | 69.553 | 52.41  | 18.612 | 20.869 |

| Thermocouple Type PTCCH2                        | B       | N      | R      |
|-------------------------------------------------|---------|--------|--------|
| Low range, °F                                   | 32      | -60    | 0      |
| °C                                              | 0       | -51    | -17.78 |
| mV at low range with reference at 70°C (158 °F) | -0.0114 | -3.195 | -0.512 |
| High range, °F                                  | 3272    | 2282   | 3092   |
| °C                                              | 1800    | 1250   | 1700   |
| mV at high range with reference at 0°C (32 °F)  | 13.593  | 45.694 | 20.220 |

## Cold Junctions

The CJ signals go into signal space and are available for monitoring. Normally the average of the two is used. Acceptable limits are configured, and if a CJ goes outside the limit, a logic signal is set. A 1 °F error in the CJ compensation will cause a 1 °F error in the thermocouple reading.

Hard-coded limits are set at -40 to 85°C (-40 to +185 °F), and if a CJ goes outside this, it is regarded as bad. Most CJ failures are open or short circuit. If the CJ is declared bad, the backup value is used. This backup value can be derived from CJ readings on other terminal boards, or can be the configured default value (refer to signals in the section, *Configuration*).

## ID Line

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## Power Management

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Specifications

| Item                               | Specification                                                                                                           |
|------------------------------------|-------------------------------------------------------------------------------------------------------------------------|
| Number of channels                 | 12 channels per pack                                                                                                    |
| Thermocouple types                 | E, J, K, S, T thermocouples, and mV inputs for PTCCH1<br>E, J, K, S, T, B, N, R thermocouples, and mV inputs for PTCCH2 |
| Span                               | -8 mV to +45 mV for PTCCH1<br>-20 mV to +95 mV for PTCCH2                                                               |
| A/D converter                      | Sampling type 16-bit A/D converter                                                                                      |
| Cold junction compensation         | Reference junction temperature measured in each module<br>TMR board has three cold junction references                  |
| Cold junction temperature accuracy | Cold junction accuracy 1.1°C (2 °F)                                                                                     |
| Conformity error                   | Maximum software error 0.14°C (0.25 °F)                                                                                 |



| Item                  | Specification                                                                                                                                                                                                                                                                                         |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Measurement accuracy  | PTCCH1 = 53 $\mu$ V (excluding cold junction reading).<br>Example: For type K, at 1000 °F, including cold junction contribution, RSS error= 3 °F<br>PTCCH2 = 115 $\mu$ V (excluding cold junction reading).<br>Example: For type K, at 1000 °F, including cold junction contribution, RSS error= 6 °F |
| Common mode rejection | AC common mode rejection 110 dB @ 50/60 Hz, for balanced impedance input. Both hardware and firmware filtering                                                                                                                                                                                        |
| Common mode voltage   | $\pm$ 5 Volts                                                                                                                                                                                                                                                                                         |
| Normal mode rejection | Rejection of 250 mV Rms at 50/60 Hz, $\pm$ 5%,<br>Both hardware and firmware filtering provides a total of 80 dB NMRR                                                                                                                                                                                 |
| Scan time             | All inputs are sampled at up to 120 times per second per input                                                                                                                                                                                                                                        |
| Fault detection       | High/low (hardware) limit check<br>High/low system (software) limit check<br>Monitor readings from all TCs, CJs, calibration voltages, and calibration zero readings                                                                                                                                  |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- A comparison is made between the commanded state of each relay drive and the feedback from the command output circuit.
- Relay board specific feedback is read by the pack and processed. The information varies depending on the relay board type. Refer to relay terminal board documentation for feedback specifics.

Details of the individual diagnostics are available in the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter         | Description                                            | Choices                  |
|-------------------|--------------------------------------------------------|--------------------------|
| PTCC_Mod_Config   |                                                        |                          |
| SysFreq           | System frequency (used for noise rejection)            | 50 or 60 Hz              |
| SystemLimits      | Enables or disables all system limit checking          | Enable, Disable          |
| Auto Reset        | Automatic restoring of thermocouples removed from scan | Enable, Disable          |
| Redundancy        | Redundancy mode of the pack                            | Simplex, Dual, TMR       |
| PTCC Point Config |                                                        |                          |
| ThermCpl1         | First of 24 thermocouples, point signal                | Point Edit (Input FLOAT) |

| Parameter                                       | Description                                                                                                                                                                                                                                                                                            | Choices                                                                              |
|-------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| ThermoCpl Type                                  | Select thermocouples type or mV input<br>Unused inputs are removed from scanning, mV inputs are primarily for maintenance, but can also be used for custom remote CJ compensation. Standard remote CJ compensation also available.                                                                     | For PTCCH1- Unused, mV, T,K,J,E, or S<br>For PTCCH2- Unused, mV, T,K,J, E,S,B,N or R |
| LowPassFiltr                                    | Enable 2 Hz low pass filter                                                                                                                                                                                                                                                                            | Enable, Disable                                                                      |
| SysLim1 Enabl                                   | Enable system limit 1 fault check<br>A temperature limit, which can be used to create an alarm                                                                                                                                                                                                         | Enable, Disable                                                                      |
| SysLim1 Latch                                   | Latch system limit 1 fault<br>Determines whether the limit condition will latch or unlatch; reset used to unlatch                                                                                                                                                                                      | Latch, unlatch                                                                       |
| SysLim1 Type                                    | System limit 1 check type<br>Limit occurs when the temperature is greater than or equal (>=), or less than or equal to (<=) a preset value                                                                                                                                                             | Greater than or equal, less than or equal                                            |
| SysLimit 1                                      | System limit 1°F or mV<br>Enter the desired value                                                                                                                                                                                                                                                      | Engineering units                                                                    |
| SysLim2 Enabled                                 | Enable system limit 2 fault check<br>A temperature limit, which can be used to create an alarm                                                                                                                                                                                                         | Enable, disable                                                                      |
| SysLim2 Latch                                   | Latch system limit 1 fault<br>Determines whether the limit condition will latch or unlatch; reset used to unlatch                                                                                                                                                                                      | Latch, unlatch                                                                       |
| SysLim2 Type                                    | System limit 1 check type                                                                                                                                                                                                                                                                              | Greater than or equal, Less than or equal                                            |
| SysLimit 2                                      | System limit 2 °F or mV<br>Enter the desired value                                                                                                                                                                                                                                                     | Engineering units                                                                    |
| TMR DiffLimt                                    | Diagnostic limit, TMR input vote difference<br>Limit condition occurs if three temperatures in R,S,T differ by more than a preset value (°F); this creates a voting alarm condition.                                                                                                                   | -60 to 2,000                                                                         |
| Only for PTCCH2 Reporting for Open thermocouple | Configuration to report <i>open</i> thermocouple as too cold or too hot. If it is set to <i>Fail_Hot</i> then temperature reported for open thermocouple is 2000 degrees C. If it is set to <i>Fail_Cold</i> then temperature reported is the minimum temperature for that thermocouple if it is open. | Fail_Cold<br>Fail_Hot                                                                |
| PTCC_CJ_Config                                  | Cold junction reference similar configuration as for thermocouples but no low pass filter                                                                                                                                                                                                              |                                                                                      |
| Cold Junction Type                              | Select CJ type                                                                                                                                                                                                                                                                                         | Remote, Local                                                                        |
| SysLimit1                                       | System limit 1, °F (Cold Junction limits)                                                                                                                                                                                                                                                              | 32.0 ... 158.0                                                                       |
| SysLimit2                                       | System limit 2, °F (Cold Junction limits)                                                                                                                                                                                                                                                              | 32.0 ... 158.0                                                                       |

| Points (Signals) | Description - Point Edit (Enter Signal Connection Name) | Direction | Type  |
|------------------|---------------------------------------------------------|-----------|-------|
| L3DIAG_PTCC      | I/O diagnostic indication                               | Input     | BIT   |
| LINK_OK_PTCC     | I/O link okay indication                                | Input     | BIT   |
| ATTN_PTCC        | I/O attention indication                                | Input     | BIT   |
| IOPackTmpr       | IO pack temperature                                     | Input     | FLOAT |
| SysLim1TC1       | System limit 1 for thermocouple 1                       | Input     | BIT   |
| :                | :                                                       | Input     | BIT   |
| SysLim1TC12      | System limit 1 for thermocouple 12                      | Input     | BIT   |
| SysLim1CJ1       | System limit 1 for cold junction                        | Input     | BIT   |
| SysLim2JC1       | System limit 2 for cold junction                        | Input     | BIT   |
| SysLim2TC1       | System limit 2 for thermocouple 1                       | Input     | BIT   |
| :                | :                                                       | Input     | BIT   |

| Points (Signals) | Description - Point Edit (Enter Signal Connection Name) | Direction | Type  |
|------------------|---------------------------------------------------------|-----------|-------|
| SysLim2TC12      | System limit 2 for thermocouple 12                      | Input     | BIT   |
| CJ Backup        | Cold junction backup                                    | Output    | FLOAT |
| CJ Remote        | Cold junction remote                                    | Output    | FLOAT |
| ThermCpl1        | Thermocouple reading                                    | Input     | FLOAT |
| :                | :                                                       | Input     | FLOAT |
| ThermCpl12       | Thermocouple reading                                    | Input     | FLOAT |
| ColdJunc1        | Cold junction for TCs 1-12                              | Input     | FLOAT |

## Alarms

### PTCC Specific Alarms

| Alarm ID | Alarm Description                        | Possible Cause                                                                                                                                                                                      | Solution                                                                                                                                                                                                                             |
|----------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 32-43    | Thermocouple [ ] Raw Counts High         | Thermocouple [ ] input to the analog to digital converter exceeded the converter limits and will be removed from scan.                                                                              | Check field wiring including shields. Check installation of I/O pack on terminal board. Problem is usually not a I/O pack or terminal board failure if other thermocouples are working correctly.                                    |
| 56-67    | Thermocouple [ ] Raw Counts Low          | Thermocouple [ ] input to the analog to digital converter exceeded the converter limits and will be removed from scan                                                                               | The board has detected a thermocouple open and has applied a bias to the circuit driving it to a large negative number, or the TC is not connected, or a condition such as stray voltage or noise caused the input to exceed -63 mV. |
| 80       | Cold Junction 1 raw counts high          | Cold junction input to the A/D converter has exceeded the limits of the converter. If a cold junctions fail, a predetermined value is used.                                                         | Check mounting of I/O pack on terminal board. Replace terminal board. Replace I/O pack.                                                                                                                                              |
| 82       | Cold Junction 1 raw counts low           | Cold junction input to the A/D converter has exceeded the limits of the converter. If a cold junctions fail, a predetermined value is used.                                                         | Check mounting of I/O pack on terminal board. Replace terminal board. Replace I/O pack.                                                                                                                                              |
| 84-85    | Calibration reference 1 raw counts high. | Every scan the I/O pack uses the internal analog/digital converter to read a precision voltage reference. This reference input exceeded the converter specified limits indicating a hardware fault. | The precision reference voltage, signal multiplexing, or A/D converter in the I/O pack has failed.                                                                                                                                   |
| 86-87    | Calibration reference 1 raw counts Low.  | Every scan the I/O pack uses the internal analog/digital converter to read a precision voltage reference. This reference input exceeded the converter specified limits indicating a hardware fault. | The precision reference voltage, signal multiplexing, or A/D converter in the I/O pack has failed.                                                                                                                                   |
| 88-89    | Null reference 1 raw counts high         | Every scan the I/O pack uses the internal analog/digital converter to read a zero voltage reference. This reference input exceeded the converter specified limits indicating a hardware fault.      | The signal multiplexing or A/D converter on the I/O pack has failed.                                                                                                                                                                 |

| Alarm ID | Alarm Description                                      | Possible Cause                                                                                                                                                                                 | Solution                                                                                                                                                                                                  |
|----------|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 90-91    | Null reference 1 raw counts low                        | Every scan the I/O pack uses the internal analog/digital converter to read a zero voltage reference. This reference input exceeded the converter specified limits indicating a hardware fault. | The signal multiplexing or A/D converter on the I/O pack has failed.                                                                                                                                      |
| 92-103   | Thermocouple [ ] Linearization Table High              | Thermocouple input [ ] has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's maximum value.                                     | The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the cold junction compensation is wrong.                                     |
| 116-127  | Thermocouple [ ] Linearization Table Low               | Thermocouple input [ ] has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's minimum value.                                     | The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the cold junction compensation is wrong, or the thermocouple wiring is open. |
| 128      | Logic Signal [ ] Voting Mismatch                       | This alarm should never occur.                                                                                                                                                                 |                                                                                                                                                                                                           |
| 160      | 15V Power supply Not Ok                                | One of the power supplies internal to the pack is not working properly. All thermocouple readings are suspect.                                                                                 | Replace the pack                                                                                                                                                                                          |
| 161      | Reference Voltage exceeded upper limits                | The reference voltage for the analog inputs is more than 5% above the expected value. Verify that the acquisition card for the pack is still functional                                        | Replace the pack                                                                                                                                                                                          |
| 162      | Reference Voltage exceeded lower limits                | The reference voltage for the analog inputs is more than 5% below the expected value. Verify that the acquisition card for the pack is still functional                                        | Replace the pack                                                                                                                                                                                          |
| 163      | Null Voltage exceeded upper limits                     | The Null voltage for the analog inputs is more than 5% above the expected value. Verify that the acquisition card for the pack is still functional                                             | Replace the pack                                                                                                                                                                                          |
| 164      | Null Voltage exceeded lower limits                     | The Null voltage for the analog inputs is more than 5% below the expected value. Verify that the acquisition card for the pack is still functional                                             | Replace the pack                                                                                                                                                                                          |
| 224-236  | Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ] | The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit.                                                                                          | A problem with the input. This could be the device, the wire to the terminal board, or the terminal board.                                                                                                |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

## ***TBTC Thermocouple Input***

### ***Functional Description***

The Thermocouple Input (TBTC) terminal board accepts 24-type E, J, K, S, or T thermocouple inputs. It accepts additional B, N and R types of thermocouple inputs only when used with PTCCH2 in Mark VIe. These inputs are wired to two barrier-type blocks on the terminal board. TBTC communicates with the I/O processor through DC-type connectors. Two types of the TBTC are available, as follows:

- TBTC1C for simplex applications has two DC-type connectors.
- TBTC1B for TMR applications has six DC-type connectors.

### ***Mark VI Systems***

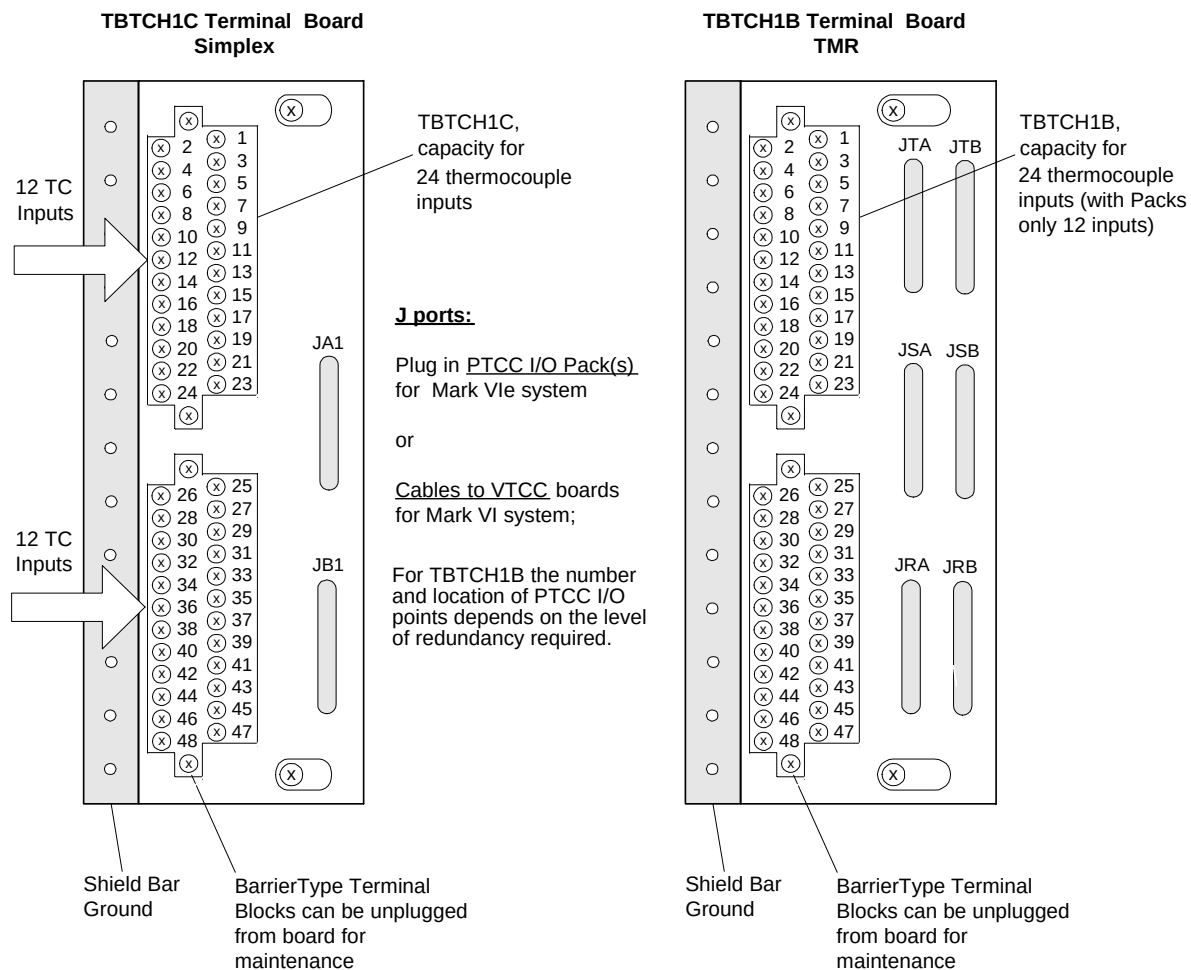
In the Mark VI system, TBTC works with the VTCC processor and supports simplex and TMR applications. One TBTC1C connects to the VTCC with two cables. In TMR systems, TBTC1B connects to three VTCC boards with six cables.

### ***Mark VIe Systems***

In the Mark VIe system, TBTC works with the PTCC I/O pack and supports simplex, dual, and TMR applications. In simplex systems, two PTCC packs plug into the TBTC1C for a total of 24 inputs. With the TBTC1B, one, two, or three PTCC packs can be connected, supporting a variety of system configurations.

- Simplex pack – 12 inputs
- Simplex packs – 24 inputs
- TMR packs – 12 inputs

The Thermocouple Input (TBTC) terminal board accepts 24-type E, J, K, S, or T thermocouple inputs for PTCCCH1 pack and 24-type E, J, K, S, T, B, N or R thermocouple inputs for PTCCCH2 pack.



*Thermocouple Terminal Board, I/O Processor, and Cabling*

## Installation

Connect the thermocouple wires directly to the two I/O terminal blocks. These removable blocks are mounted on the terminal board and held down with two screws. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located on the left side of each terminal block.

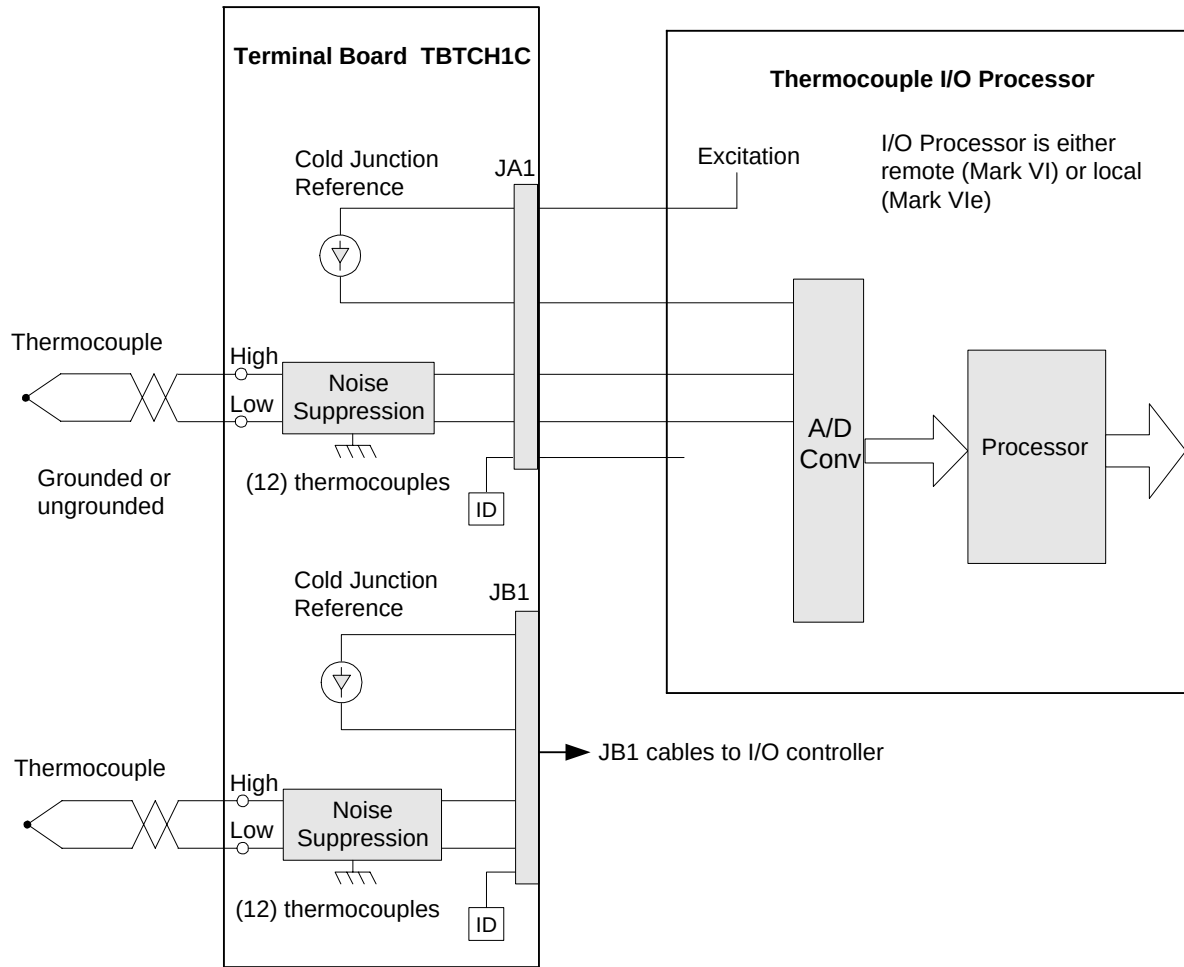
In Mark VI systems, cable the TBTC J-type connectors to the I/O processors in the VME rack.

In Mark VIe systems, plug the I/O packs directly into the TBTC J-type connectors. The number of cables or I/O packs depends on the level of redundancy required.

## Operation

The 24 thermocouple inputs can be grounded or ungrounded. They can be located up to 300 m (984 ft) from the turbine control panel with a maximum two-way cable resistance of 450  $\Omega$ . TBTC features high-frequency noise suppression and two CJ reference devices, as shown in following figure. The I/O processor performs the analog-to-digital conversion and the linearization for individual thermocouple types.

In Mark VI simplex systems using TBTCH1C, one VTCC is used. In Mark VIe simplex systems, two PTCC packs plug into TBTC, obtaining 24 thermocouple inputs.

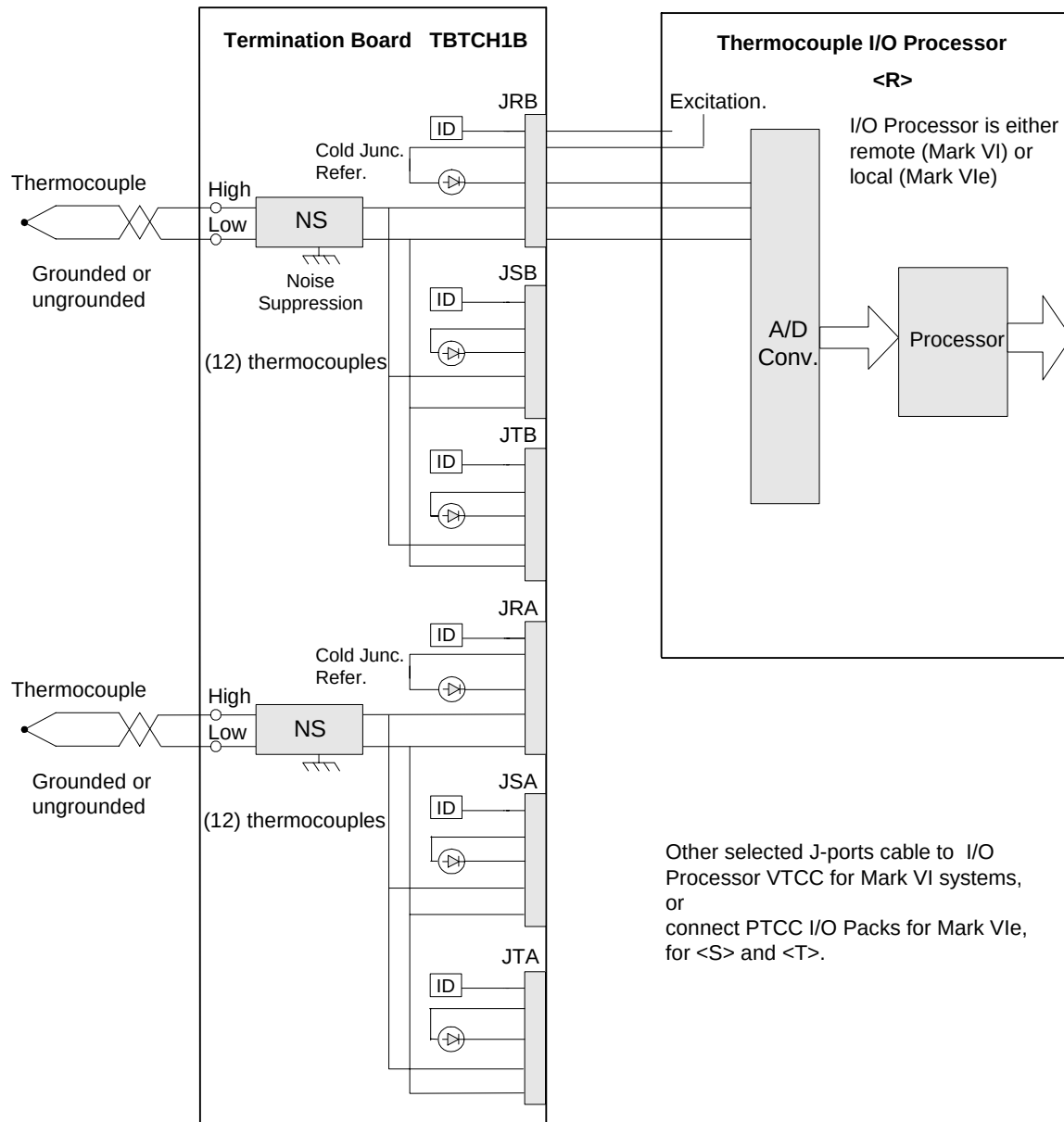


*Thermocouple Inputs and I/O Processor, Simplex*



For TMR systems using TBTC1B, the thermocouple signals fan out to three J-connectors. The Mark VI system accommodates 24 inputs and the Mark VIe system accommodates 12 inputs.

The TBTC terminal board supports all thermocouple spans documented for the associated thermocouple I/O processor.



*Thermocouple Inputs and I/O Processor, TMR systems*

## Thermocouple Limits

### TBTC with PTCCH1 or VTCC

Thermocouple inputs support a full-scale input range of -8.0 mV to + 45.0 mV. The following table shows typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from -30 to 65°C (-22 to +149 °F).

| Thermocouple Type PTCCH1                        | E      | J      | K      | S      | T      |
|-------------------------------------------------|--------|--------|--------|--------|--------|
| Low range, °F                                   | -60    | -60    | -60    | 0      | -60    |
| °C                                              | -51    | -51    | -51    | -17.78 | -51    |
| mV at low range with reference at 70°C (158 °F) | -7.174 | -6.132 | -4.779 | -0.524 | -4.764 |
| High range, °F                                  | 1100   | 1400   | 2000   | 3200   | 750    |
| °C                                              | 593    | 760    | 1093   | 1760   | 399    |
| mV at high range with reference at 0°C (32 °F)  | 44.547 | 42.922 | 44.856 | 18.612 | 20.801 |

### TBTC with PTCCH2

Thermocouple inputs support a full-scale input range of -20.0 mV to + 95.0 mV. The following table shows typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from -30 to 65°C (-22 to +149 °F).

| Thermocouple Type PTCCH2                        | E      | J      | K      | S      | T      |
|-------------------------------------------------|--------|--------|--------|--------|--------|
| Low range, °F                                   | -60    | -60    | -60    | 0      | -60    |
| °C                                              | -51    | -51    | -51    | -17.78 | -51    |
| mV at low range with reference at 70°C (158 °F) | -7.174 | -6.132 | -4.779 | -0.524 | -4.764 |
| High range, °F                                  | 1832   | 2192   | 2372   | 3200   | 752    |
| °C                                              | 1000   | 1200   | 1300   | 1760   | 400    |
| mV at high range with reference at 0°C (32 °F)  | 76.373 | 69.553 | 52.41  | 18.612 | 20.869 |

| Thermocouple Type PTCCH2                        | B       | N      | R      |
|-------------------------------------------------|---------|--------|--------|
| Low range, °F                                   | 32      | -60    | 0      |
| °C                                              | 0       | -51    | -17.78 |
| mV at low range with reference at 70°C (158 °F) | -0.0114 | -3.195 | -0.512 |
| High range, °F                                  | 3272    | 2282   | 3092   |
| °C                                              | 1800    | 1250   | 1700   |
| mV at high range with reference at 0°C (32 °F)  | 13.593  | 45.694 | 20.220 |

## Cold Juncions

The CJ signals go into signal space and are available for monitoring. Normally the average of the two is used. Acceptable limits are configured, and if a CJ goes outside the limit, a logic signal is set. A 1 °F error in the CJ compensation will cause a 1 °F error in the thermocouple reading.

Hard-coded limits are set at -40 to 85°C (-40 to +185 °F), and if a CJ goes outside this, it is regarded as bad. Most CJ failures are open or short circuit. If the CJ is declared bad, the backup value is used. This backup value can be derived from CJ readings on other terminal boards, or can be the configured default value (refer to signals in the section, *Configuration*).

## Specifications

| Item                               | Specification                                                                                                                                                                       |
|------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels                 | 24 channels per terminal board                                                                                                                                                      |
| Thermocouple types                 | E, J, K, S, T thermocouples, and mV inputs if TBTC is connected to PTCCH1 or VTCCH1<br>E, J, K, S, T, B, N ,R thermocouples, and mV inputs if TBTC is connected to PTCCH2 or VTCCH2 |
| Span                               | -8 mV to +45 mV if TBTC is connected to PTCCH1 or VTCCH1<br>-20 mV to +95 mV if TBTC is connected to PTCCH2 or VTCCH2                                                               |
| Cold junction compensation         | Reference junction temperature measured at two locations on each H1C terminal board<br>TMR H1B board has six CJ references. Only three available with Mark VIe I/O packs.           |
| Cold junction temperature accuracy | CJ accuracy 1.1°C (2 °F)                                                                                                                                                            |
| Fault detection                    | High/low (hardware) limit check<br>Monitor readings from all TCs, CJs, calibration voltages, and calibration zero readings.                                                         |

## Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- Each thermocouple type has hardware-limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the inputs hardware limits is set, it creates a composite diagnostic alarm.
- Each terminal board connector has its own ID device that is interrogated by the I/O board. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the J connector location. If a mismatch is encountered, a hardware incompatibility fault is created.
- When operating with the I/O processor a very small current is injected into each thermocouple path. This is done to detect open circuits and is of a polarity to create a low temperature reading should a thermocouple open.

## Configuration

There are no jumpers or hardware settings on the board.

---

# ***STTC Simplex Thermocouple Input***

## ***Functional Description***

The Simplex Thermocouple Input (STTC) terminal board is a compact terminal board designed for DIN-rail or flat mounting. The board has 12 thermocouple inputs and connects to the PTCC thermocouple processor board. The on-board signal conditioning and cold junction reference is identical to those on the larger TBTC board. High-density Euro-Block type terminal blocks are mounted to the board, and two types are available. An on-board ID chip identifies the board to the processor for system diagnostic purposes.

## ***Mark VIe Systems***

In the Mark\* VIe systems, the PTCC I/O pack works with the STTC. The I/O pack plugs into the DC-37 pin connector and communicates with the controller over Ethernet. Only simplex systems are supported.

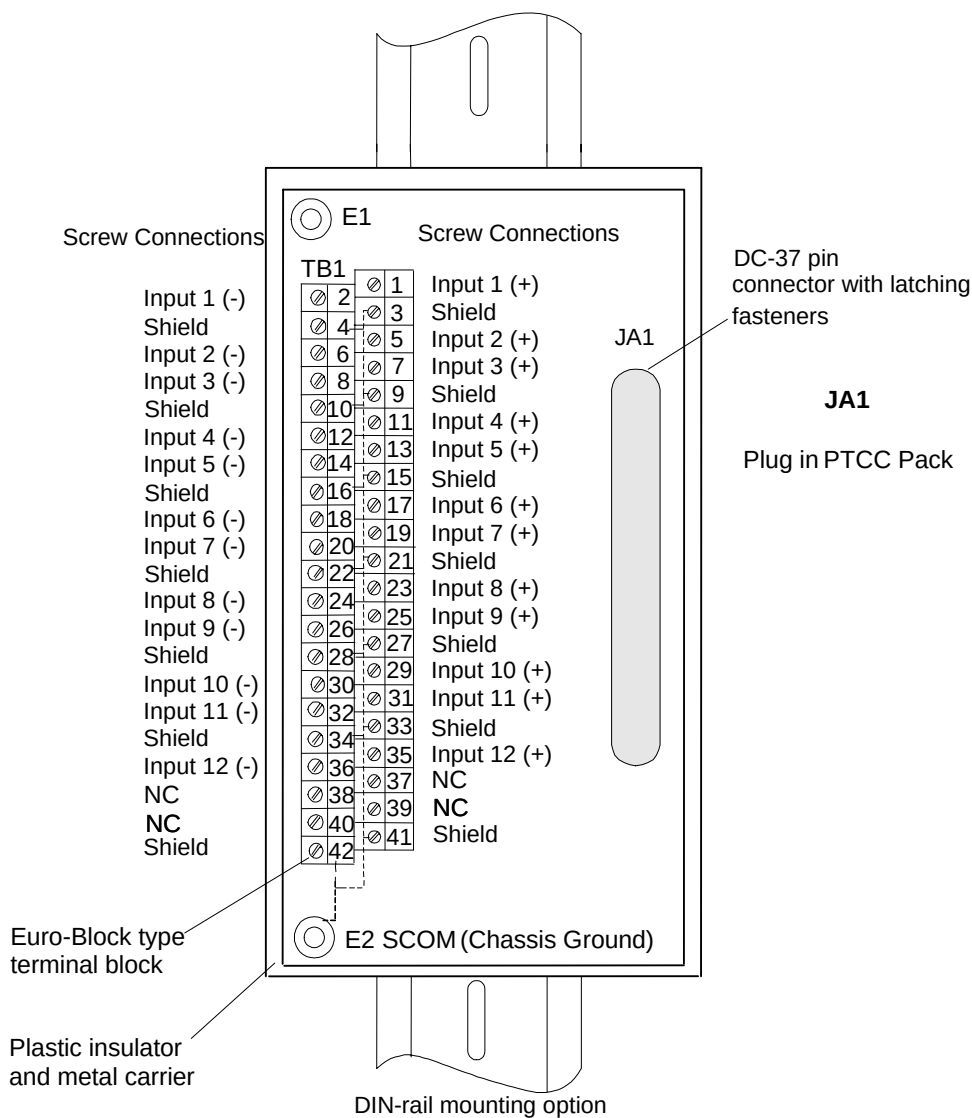
## Installation

The STTC and a plastic insulator mount on a sheet metal carrier, which mounts on a DIN rail. The STTC and insulator mount on a sheet metal assembly that bolts directly in a panel. Thermocouples are wired directly to the terminal block using typical #18 AWG wires. The Euro-Block type terminal block has 42 terminals that can be fixed or removable.

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**Note** Shield screws are provided on this board, internally connected to SCOM.

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STTC Thermocouple Terminal Board

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**Note** Shields should be terminated on designated terminals on TB1.

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Two types of Euro-Block terminal blocks are available as follows:

- Terminal board STTCH1 has a permanently mounted terminal block with 42 terminals.
- Terminal board STTCH2 has a right-angle header accepting a range of commercially available plugged terminal blocks, with a total of 42 terminals.

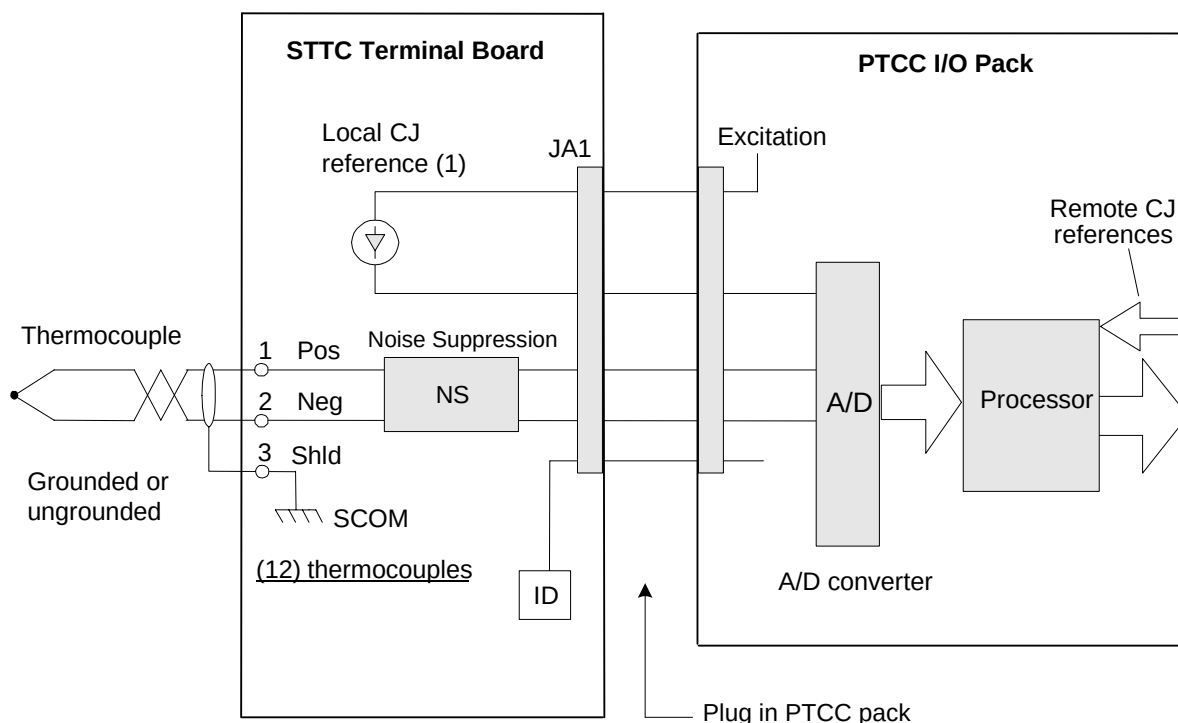
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**Note** E1 and E2 are holes for chassis grounding screws.

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## Operation

Connection of the STTC to the I/O pack or board that contains the A/D converter is shown in the following figure. The I/O pack or board provides excitation for the cold junction (CJ) reference on the terminal board. The 12 thermocouple signals plus the CJ signal and the connection to the identity chip (ID) come through connector JA1.



STTC and I/O Processor

## Specifications

| Item                               | Specification                                                                                                                                                   |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of channels                 | 12 channels per terminal board                                                                                                                                  |
| Thermocouple types                 | E, J, K, S, T thermocouples, and mV inputs if STTC is connected to PTCCH1<br>E, J, K, S, T, B, N, R thermocouples, and mV inputs if STTC is connected to PTCCH2 |
| Span                               | -8 mV to +45 mV if STTC is connected to PTCCH1<br>-20 mV to +95 mV if STTC is connected to PTCCH2                                                               |
| Cold junction compensation         | Reference junction temperature measured at one location                                                                                                         |
| Cold junction temperature accuracy | Cold junction accuracy -17°C (2 °F)                                                                                                                             |
| Fault detection                    | High/low (hardware) limit check<br>Check ID chip on JA1 connector                                                                                               |

## ***Diagnostics***

Diagnostic tests to components on the terminal boards are as follows:

- Each thermocouple type has hardware-limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the inputs hardware limits is set, it creates a composite diagnostic alarm.
- Each terminal board connector has its own ID device that is interrogated by the I/O board. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the J connector location. If a mismatch is encountered, a hardware incompatibility fault is created.
- When operating with the I/O processor a very small current is injected into each thermocouple path. This is done to detect open circuits and is of a polarity to create a low temperature reading should a thermocouple open.

## ***Configuration***

There are no jumpers or hardware settings on the board.

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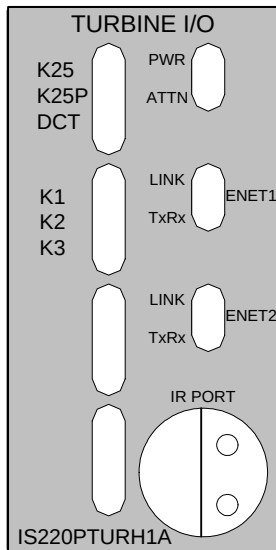
## ***Notes***



# PTUR Turbine Specific Primary Trip

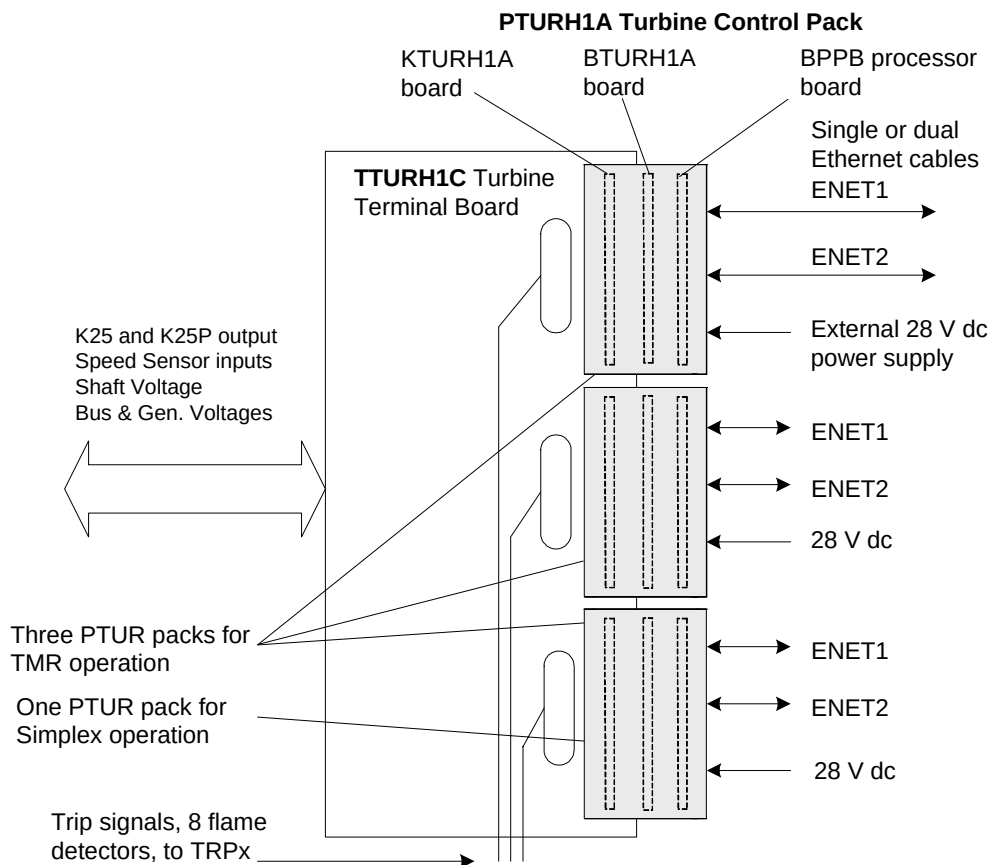
## PTUR Primary Turbine Protection

### Functional Description



The Primary Turbine Protection (PTUR) pack provides the electrical interface between one or two I/O Ethernet networks and a turbine control terminal board. The pack contains a processor board common to all Mark\* V1e distributed I/O packs, a board specific to the turbine control function, and an analog acquisition daughterboard. The pack plugs into the TTURH1C terminal board and handles four speed sensor inputs, bus and generator voltage inputs, shaft voltage and current signals, eight flame sensors, and outputs to the main breaker. Input to the pack is through dual RJ45 Ethernet connectors and a three-pin power input. Output is through a DC-62 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are through an infrared port.

As an alternative to TTURH1C, three PTUR packs may be plugged directly into a TRPAH1A terminal board. This arrangement handles four speed inputs per PTUR, or alternately fans the first four inputs into all three PTURs. Two solid-state primary trip relays are provided by TRPA. This arrangement does not support bus and generator voltage inputs, shaft voltage or current signals, flame sensors, or main breaker output. Refer to TRPAH1A documentation for additional details.



## Compatibility

PTURH1A is compatible with the Turbine Terminal Board TTURH1C, and the STUR board, but not the DIN rail-mounted DTUR or other TTUR boards. The following table gives details of the compatibility:

| Terminal Board | TTURH1C, TRPAH1A and H2A | DTUR | STURH1A       |
|----------------|--------------------------|------|---------------|
| Control mode   | Simplex - no             | No   | Simplex - yes |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections
- TMR uses three I/O packs with one network connection on each

## ***Installation***

### **➤ To install the PTUR pack**

- 1** Securely mount the desired terminal board.
- 2** Directly plug one PTUR I/O pack for simplex or three PTUR I/O packs for TMR into the terminal board connectors.
- 3** Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4** Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5** Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6** Configure the I/O pack as necessary.

---

**Note** The PTUR mounts directly to a Mark VIe TTURH1C terminal board. The TMR capable terminal board has three DC-62 pin connectors for I/O packs, and can also be used in simplex mode if only one PTUR is installed. The PTUR directly supports all of these connections.

---

## ***Operation***

### ***Processor***

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

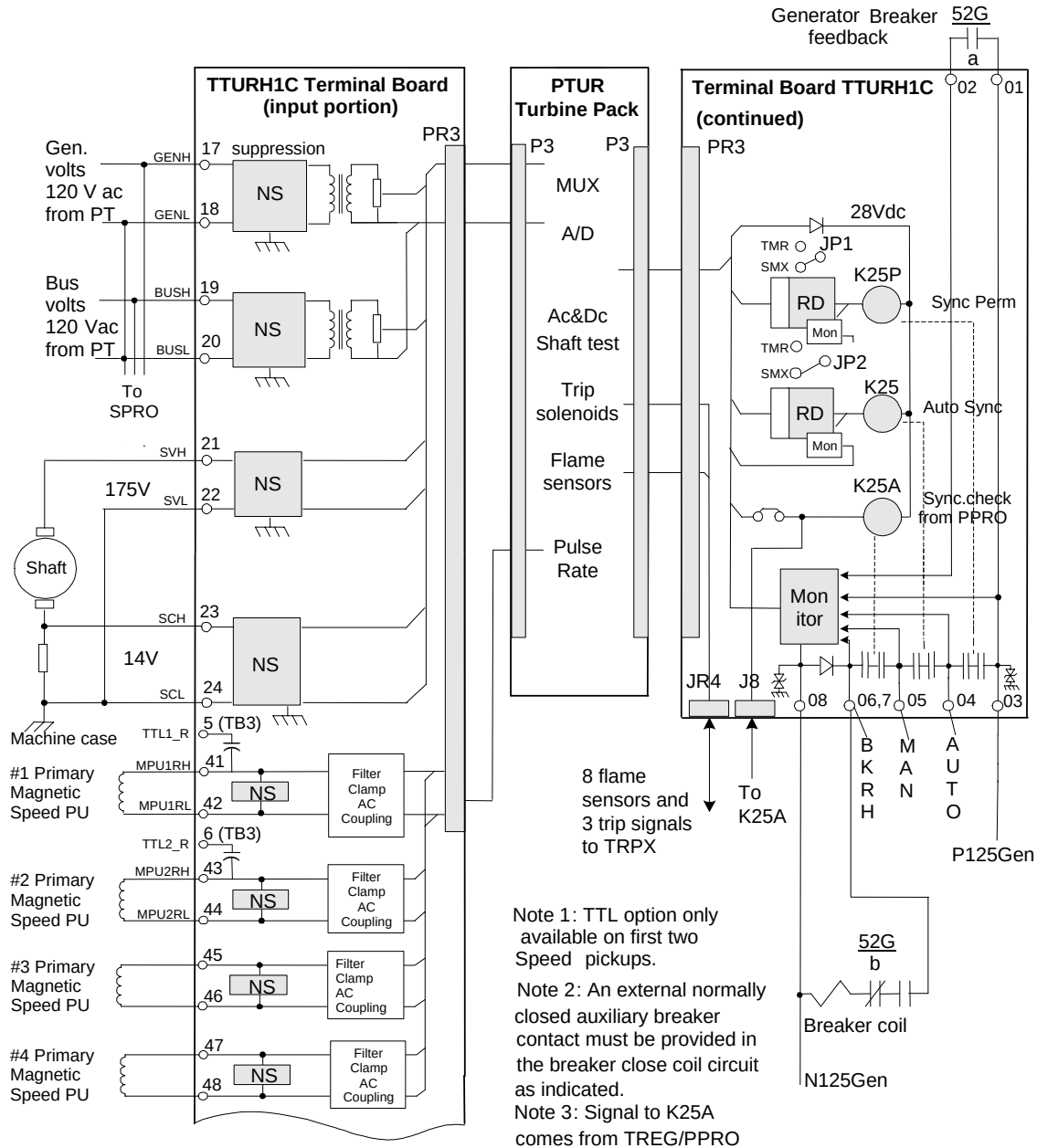
The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

### ***Analog Input Hardware***

In the simplex application, up to four pulse rate signals may be used to measure turbine speed. Circuits to convert pulse rate to digital speed are in the PTUR pack. Generator and bus voltages are brought into PTUR for automatic synchronizing in conjunction with the turbine controller and GE excitation system. TTUR has permissive generator synchronizing relays and controls the main breaker relay coil 52G. Shaft voltage is picked up with brushes and monitored along with the current to the machine case. PTUR alarms high voltages and tests the integrity and continuity of the circuitry.

In TMR applications there are separate sets of four speed inputs for each PTUR, R, S, and T. All other I inputs fan to the three PTUR packs. Control signals from R, S, and T are voted before they actuate permissive relays K25 and K25P. Relay K25A is controlled by the I/O controller and TREG boards. All three relays have two normally open contacts in series with the breaker close coil.



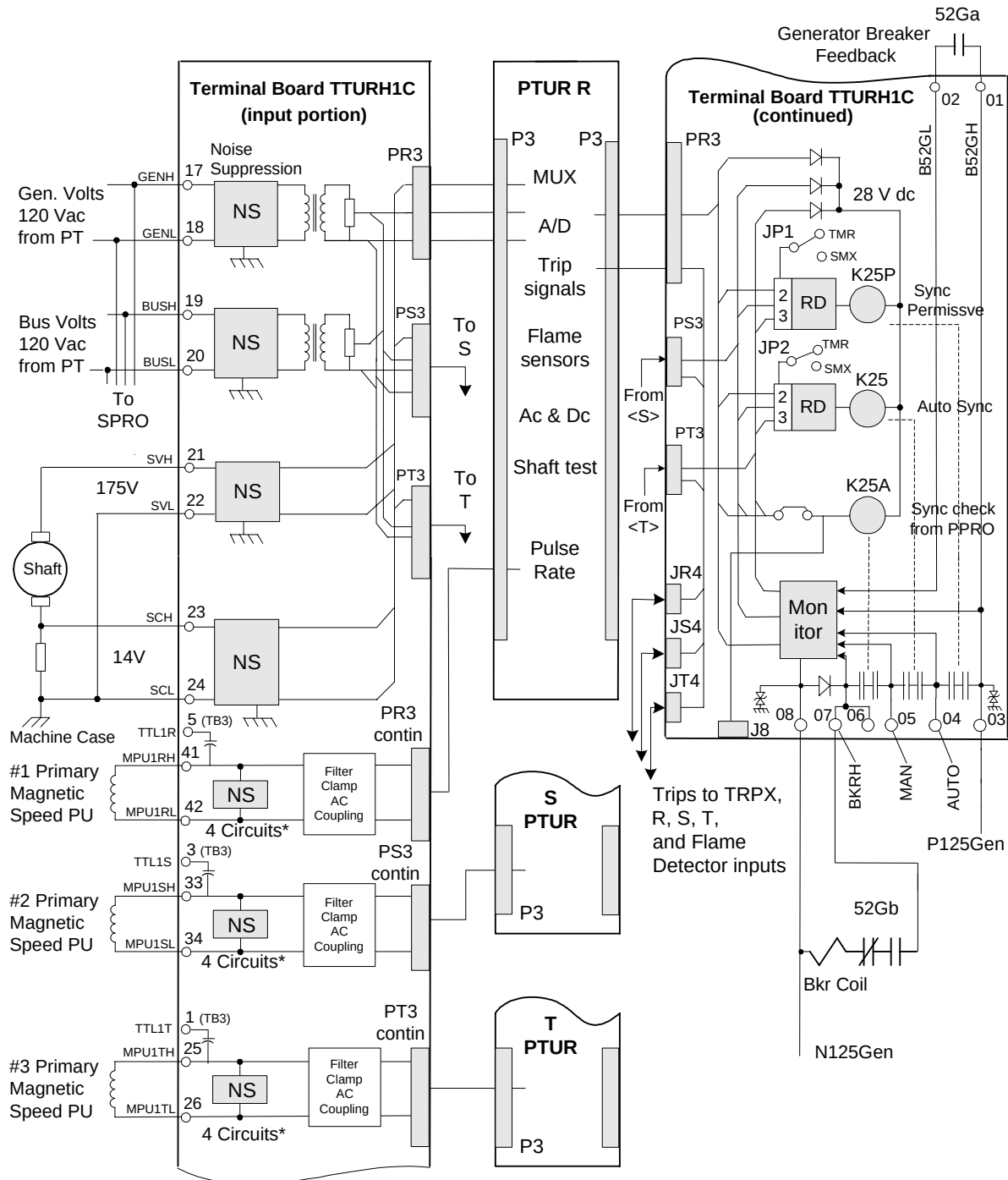
PTUR Pack with TTURH1C Terminal Board, Simplex System

## Speed Pickups

**Note** The median speed signal is used for speed control and for the primary overspeed trip signal.

An interface is provided for four passive, magnetic speed inputs with a frequency range of 2 to 20,000 Hz. Using passive pickups on a sixty-tooth wheel, circuit sensitivity allows detection of 2-RPM turning gear speed to determine if the turbine is stopped (zero speed). If automatic turning gear engagement is provided in the turbine control, this signal initiates turning gear operation.

The primary overspeed trip calculations are performed in the controller using algorithms similar to (but not the same as) those in the PPRO protection board. The fast trip option used on gas turbines runs in PTUR.



**Note 1:** TTL option only available on the first two circuits of each group of 4 pickups.

*PTUR Packs with TTURH1C Terminal Board, TMR System*

## ***Primary Trip Solenoid Interface***

The normal primary overspeed trip is calculated in the controller and passed to the PTUR and then to the chosen primary trip terminal board. TRPx contains relays for interface with the electrical trip devices (ETD). TRPx typically works in conjunction with an emergency trip board (TREG) to form the primary and emergency sides of the interface to the ETDs. PTUR supports up to three ETDs driven from each TRPx/TREx combination.

There are a number of different trip boards supported by PTUR. TRPG is targeted at gas turbine applications and works in conjunction with TREG for emergency trip. TRPS is used for small and medium size steam turbine systems and is controlled by the PTUR I/O pack. TRPL is intended for large steam turbine systems and is controlled by the PTUR I/O pack for emergency trip. Additional trip boards are being developed for other specific applications.

In support of the trip board operation, PTUR provides a number of discrete inputs used to monitor signals such as trip relay position, synchronizing relay coil drive, and ETD power status.

---

**Note** The reset signal applied to this function is not edge triggered. A continuously applied reset can result in output cycling in the presence of an intermittent trip signal. The duration of the reset should only be sufficient to allow the reset to complete and should not be maintained.

---

## ***Automatic Synchronizing***

All synchronizing connections are located on the TTUR terminal board. The generator and bus voltages are provided by two, single phase, potential transformers (PTs) with a fused secondary output supplying a nominal 115 V rms. Measurement accuracy between the zero crossing for the bus and generator voltage circuits is 1 degree.

Turbine speed is matched against the bus frequency. The generator and bus voltages are matched by adjusting the generator field excitation voltage from commands sent between the turbine controller and the EX2000 over the Unit Data Highway (UDH). A command is given to close the breaker when all permissions are satisfied. The breaker is predicted to close within the calculated phase/slip window. Feedback of the actual breaker closing time is provided by a 52G/a contact from the generator breaker (not an auxiliary relay) to update the database. An internal K25A sync check relay is provided on the TTUR; the independent backup phase/slip calculation for this relay is performed in the <P> protection module. Diagnostics monitor the relay coil and contact closures to determine if the relay properly energizes or de-energizes upon command.

## Synchronizing Modes

There are three basic synchronizing modes. Traditionally, these modes are selected from a generator panel mounted selector switch:

- **Off** The breaker cannot be closed by the controller. The check relay will not pick up.
- **Manual** The operator initiates breaker close, which is still subject to the K25A Sync Check contacts driven by the PPRO. The manual close is initiated from an external contact on the generator panel, normally connected in series with a sync mode in manual contact.
- **Auto** The system automatically matches voltage and speed, and then closes the breaker at the right time to hit top dead center on the synchroscope. All three of the following functions must agree for this closure to occur:
  - K25A - sync check relay, checks the allowable slip/phase window, from PPRO
  - K25 - auto sync relay, provides precision synchronization, from PTUR
  - K25P - sync sequence permissive, checks the turbine sequence status, from PTUR

The K25A relay should close before the K25 or else the sync check function will interfere with the auto sync optimizing. If this sequence is not executed, a diagnostic alarm is posted, a lockout signal is set true in signal space, and the application code may prevent any further attempts to synchronize until a reset is issued and the correct coordination is set up. Details of the various checks are discussed in the following sections.

## Hardware

The synchronizing system interfaces to the breaker close coil via the TTURH1C terminal board. Three Mark VIe relays must be picked up, plus external permissions must be true before a breaker can be closed.

The K25P relay is directly driven from the controller application code. In a TMR system, it is driven from R, S, and T, using 2/3 logic voting. For a simplex system, it may be configured by jumper to be driven from R only.

The K25 relay is driven from the PTUR auto sync algorithm, which is managed by the controller application code. In a TMR system, it is driven from R, S, and T, using 2/3 logic voting. Again for a simplex system, it may be configured by jumper to be driven from R only.

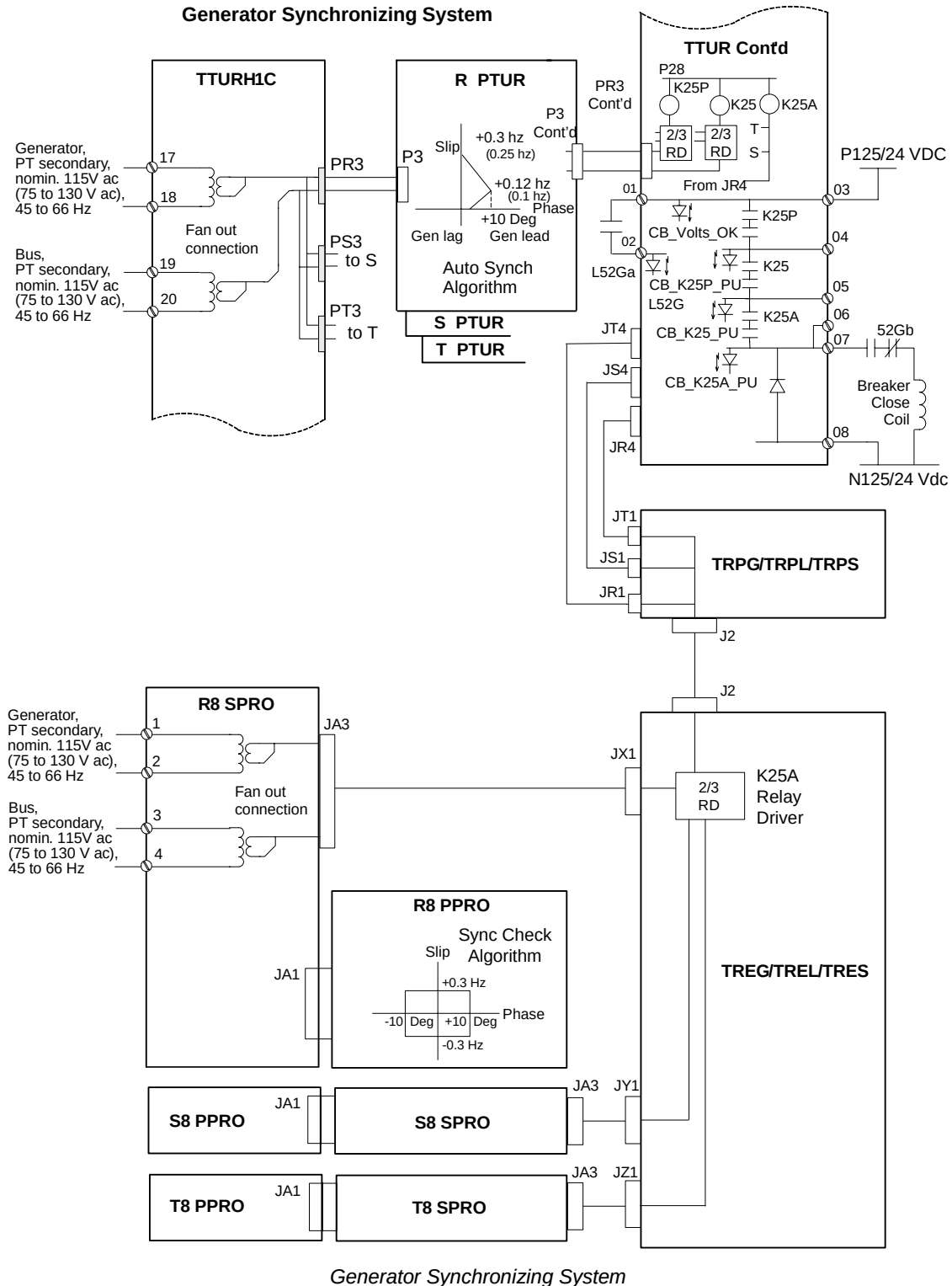
The K25A relay is located on TTUR, but is driven from the PPRO sync check algorithm, which is managed by the controller application code. The relay is driven from PPRO, R8, S8, and T8, using 2/3 logic voting in TREG/L/S.

The sync check relay driver (located on TREG/L/S) is connected to the K25A relay coil (located on TTUR) through cabling through J2 to TRPG/L/S. It then goes through JR1 (and JS1, JT1) to JR4 (and JS4, JT4) on TTUR.

Both sides of the breaker close coil power bus must be connected to the TTUR board. This provides diagnostic information and measures the breaker closure time, through the normally open breaker auxiliary contact, for optimization.



The breaker close circuit is rated to make (close) **10 A at 125 V dc**, but to open **only 0.6 A**. A normally open auxiliary contact on the breaker is required to interrupt the closing coil current.



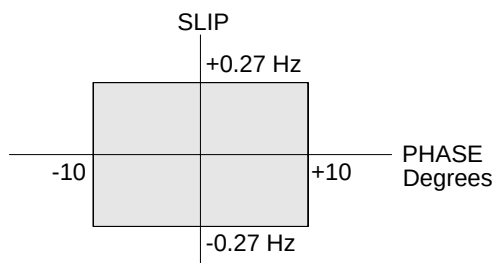
*Generator Synchronizing System*

## Sync Check

The K25A sync check function is based on phase lock loop techniques. The PPRO performs the calculations for this function, but interfaces to the breaker close circuit are located on the TTUR board, not TPRO. Limit checks are performed against adjustable constants as follows:

- Generator under-voltage
- Bus under-voltage
- Voltage error
- Frequency error (slip), with a maximum value of 0.33 Hz, typically set to 0.27 Hz
- Phase error with a maximum value of 30 °, typically set to 10 °.

In addition, sync check arms logic to enable the function, and provides bypass logic for deadbus closure. The sync window below is based on typical settings:

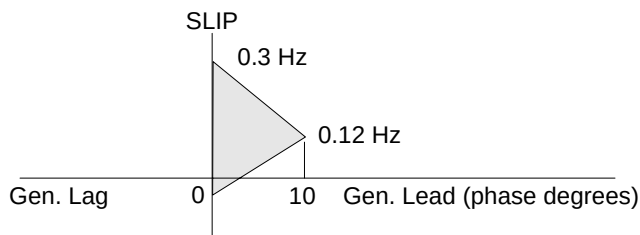


*Typical Sync Window*

## Auto Sync

The Auto Sync K25 function uses zero voltage crossing techniques. It compensates for the breaker time delay, which is defined by two adjustable constants with logic selection between the two (for two breaker applications). PTUR performs the calculations for phase, slip, acceleration, and anticipated time lead for the breaker delay. The time delay parameter is adjusted (up to certain limits) based on the measured breaker close time.

In addition, auto sync arms logic to enable the function, and bypasses logic to provide for deadbus or manual closure. The auto sync projected sync window is shown below, where positive slip indicates that the generator frequency is higher than the bus frequency.



*Auto Sync Projected Window*

The projected window is based on current phase, current slip, and current acceleration. The generator must currently be lagging and have been lagging for the last 10 consecutive cycles, and projected (anticipated) to be leading when the breaker actually reaches closure. Auto sync does not allow the breaker to close with negative slip; speed matching typically aims at around + 0.12 Hz slip.

## Synchronization Display

A special synchronization screen is available on the HMI with a real-time graphical phase display and control pushbutton. The display items are listed in table.

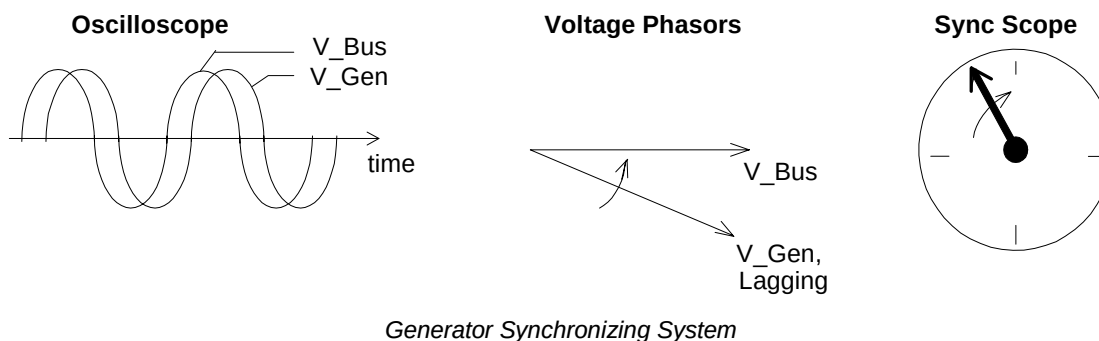
| Sync Display        | Description                                                                                                                                                                                                                                 |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Dynamic Parameters  | Voltages: Generator, Bus, Difference<br>Frequencies: Generator, Bus, Slip (difference)<br>Phase: Difference angle, degrees                                                                                                                  |
| Status Indication   | Mode: Sync OFF, MANUAL, AUTO<br>Sync Monitor: OFF, ON<br>Dead bus breaker: Open/close<br>Second breaker if applicable: Open/close<br>Sync permissive: K25P<br>Auto sync enabled<br>Speed adjust: Raise/lower<br>Voltage adjust: Raise/lower |
| Sync Permissive     | Gen voltage: OK/not OK<br>Bus voltage: OK/not OK<br>Gen frequency: OK/not OK<br>Bus frequency: OK/not OK<br>Difference volts: OK/not OK<br>Difference frequ:OK/not OK<br>Phase: K25, OK/not OK<br>K25A, OK/not OK                           |
| Limit Constants     | Upper and lower limits for the above permissive                                                                                                                                                                                             |
| Breaker Performance | Diagnostics: Slow check relay<br>Sync relay lockup<br>Breaker #1 close time out of limits<br>Breaker #2 close time out of limits<br>Relay K25P trouble<br>Breaker closing voltage (125 V dc) missing                                        |
| Control Pushbuttons | Sync monitor: ON, OFF<br>Speed adjust: RAISE, LOWER<br>Voltage adjust:RAISE, LOWER                                                                                                                                                          |

## Application Code

The application code must sequence the turbine and bring it to a state where it is ready for the generator to synchronize with the system bus. For automatic synchronization, the code must:

- Match speeds
- Match voltages
- Energize the sync permissive relay, K25P
- Arm (grant permission to) the sync check function (PPRO, K25A)
- Arm (grant permission to) the auto sync function (PTUR, K25)

The following illustrations represent positive slip (Gen) and negative phase (Gen).



## Algorithm Descriptions

This section describes the synchronizing algorithms in the PTUR I/O pack, and in the PPRO I/O pack.

### Automatic Synchronization Control in PTUR (K25)

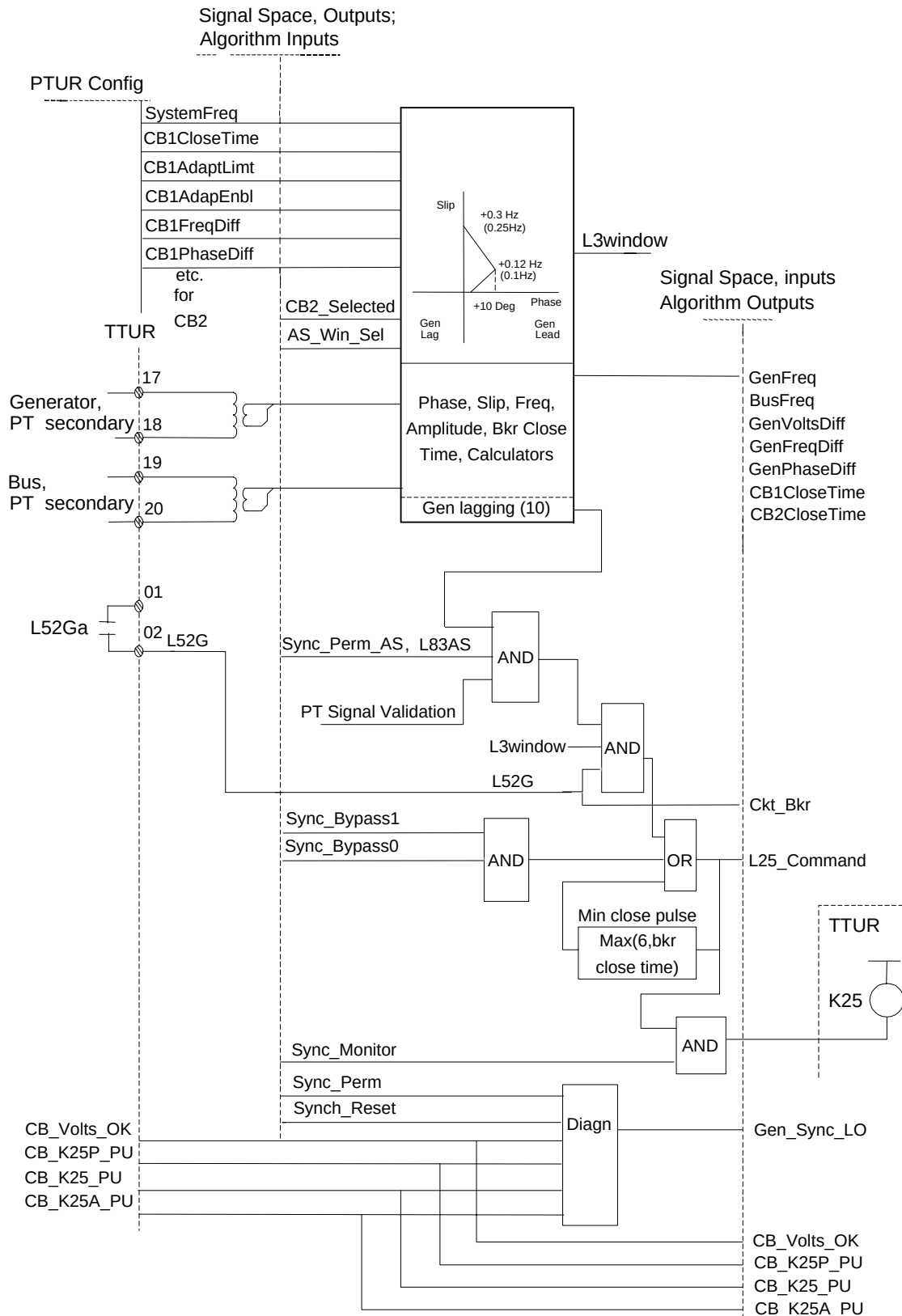
PTUR runs the auto sync algorithm. Its basic function is to monitor two Potential Transformer (PT) inputs, generator and bus, to calculate phase and slip difference, and when armed (enabled) from the application code, and when the calculations anticipate top center, to attempt a breaker closure by energizing relay K25. The algorithm uses the zero voltage crossing technique to calculate phase, slip, and acceleration. It compensates for breaker closure time delay (configurable), with self-adaptive control when enabled, with configurable limits. It is interrupt driven and must have generator voltage to function. The configuration can manage the timing on two separate breakers. For details, refer to the figure.

The algorithm has a bypass function, two signals for redundancy, to provide dead bus and Manual Breaker Closures. It anticipates top dead center; therefore, it uses a projected window, based on current phase, slip, acceleration, and breaker closure time. To pickup K25, the generator must be currently lagging, have been lagging for the last 10 consecutive cycles, and projected (anticipated) to be leading when the breaker actually reaches closure. Auto sync will not allow the breaker to close with negative slip. In this fashion, assuming the correct breaker closure time has been acquired, and the sync check relay is not interfering, breaker closures with less than 1 degree error can be obtained.

Slip is the difference frequency (Hz), positive when the generator is faster than the bus. Positive phase means the generator is leading the bus; the generator is ahead in time, or the right hand side on the synchroscope. The standard window is fixed and is not configurable. However, a special window has been provided for synchronous condenser applications where a more permissive window is needed. It is selectable with a signal space Boolean and has a configurable slip parameter.

The algorithm validates both PT inputs with a requirement of 50% nominal amplitude or greater; that is, they must exceed approximately 60 V rms before they are accepted as legitimate signals. This is to guard against cross talk under open circuit conditions. The monitor mode is used to verify that the performance of the system is correct, and to block the actual closure of the K25 relay contacts; it is used as a confidence builder. The signal space Input Gen\_Sync\_Lo will become true if the K25 contacts are closed when they should not be closed, or if the Sync Check K25A is not picked up before the Auto Sync K25. It is latched and can be reset with Sync\_Reset.

The algorithm compensates for breaker closure time delay, with a nominal breaker close time, provided in the configuration in milliseconds. This compensation is adjusted with self-adaptive control, based upon the measured breaker close time. The adjustment is made in increments of one cycle (16.6/20 ms) per breaker closure and is limited in authority to a configurable parameter. If the adjustment reaches the limit, a diagnostic alarm Breaker Slower/Faster than limits allows is posted.



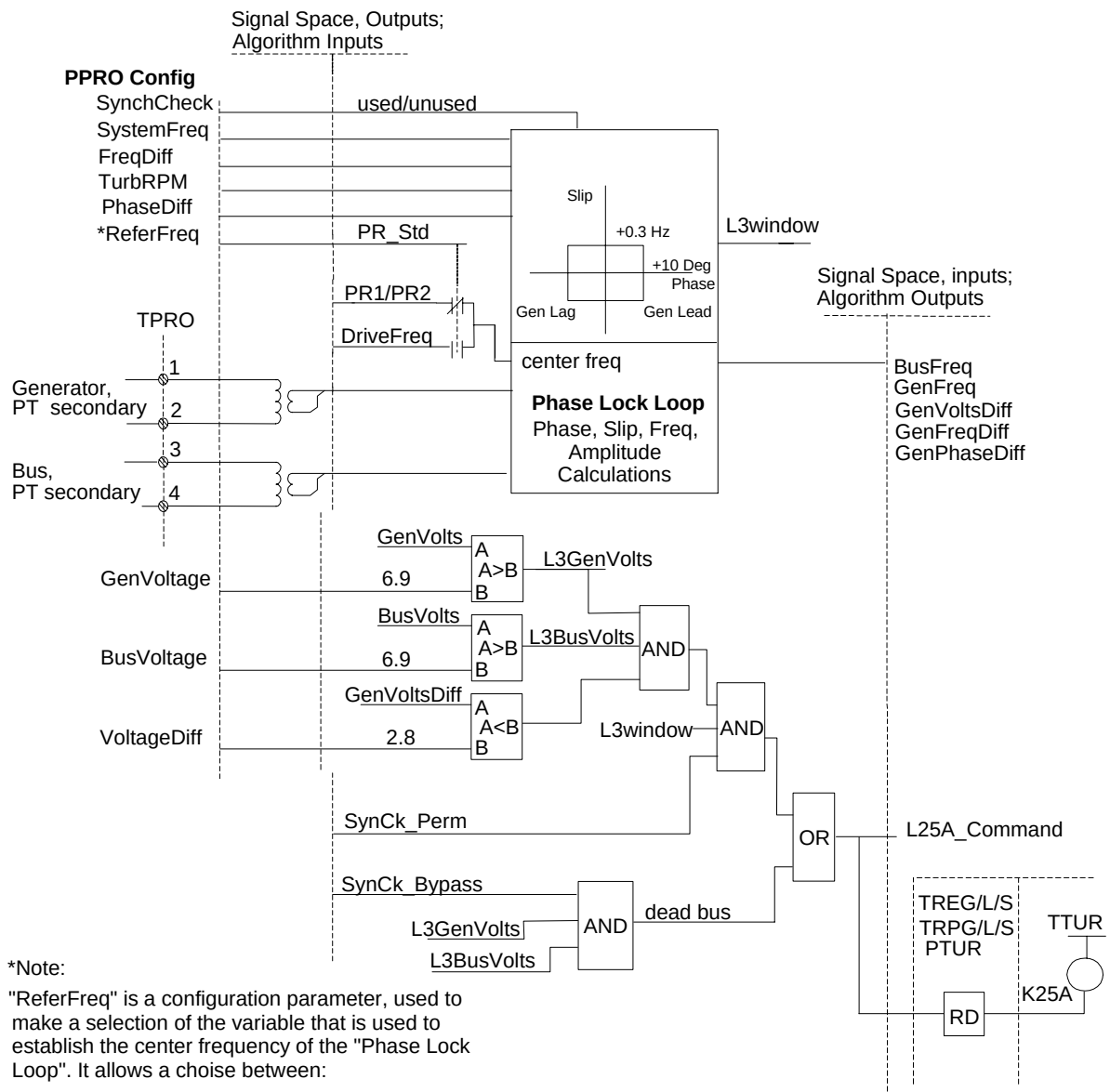
## ***Synchronization Check in PPRO (K25A)***

The sync check algorithm is performed in the PPRO I/O packs. Its basic function is to monitor two Potential Transformer (PT) inputs, and to calculate generator and bus voltage amplitudes and frequencies, phase, and slip. When it is armed (enabled) from the application code, and when the calculations determine that the input variables are within the requirements, the relay K25A will be energized. The above limits are configurable. The algorithm uses the phase lock loop technique to derive the above input variables, and has a bypass function to provide dead bus closures. The window in this algorithm is the current window, not the projected window (as used on the auto sync function), therefore it does not include anticipation.

The Sync Check will allow the breaker to close with negative slip. The window is configurable for phase and slip.

The following diagnostics relating to the auto sync function are generated by PPRO:

- K25A Relay (sync check) Driver mismatch requested state. This means the I/O controller cannot establish a current path from PPRO to the TREx terminal board.
- K25A Relay (sync check) Coil trouble, cabling to P28V on TTUR. This means the K25A relay is not functional; it could be due to an open circuit between the TREx and the TTUR terminal boards or to a missing P28 V source on the TTUR terminal board.



PPRO Sync Check

## Hardware Verification Procedure

The hardware interface may be verified by forcing the three synchronizing relays, individually or in combination. If the breaker close coil is connected to the TTUR terminal board, then the breaker must be disabled so as not to actually connect the generator to the system bus.

- 1 Operate the K25P relay by forcing output signal *Sync Perm* found under PTUR, card points. Verify that the K25P relay is functional by probing TTUR screws 3 and 4. The application code has direct control of this relay.
- 2 Simulate generator voltage on TTUR screws 17 and 18. Operate the K25 relay by forcing TTUR, card point output signals *Sync\_Bypass1* =1, and *Sync\_Bypass0* = 0. Verify that the K25 relay is functional by probing screws 4 and 5 on TTUR.
- 3 Simulate generator voltage on SPRO screws 1 and 2. Operate the K25A relay by forcing SPRO, card point output signals *SynCK\_Bypass* =1, and *SynCk\_Perm* 1. The bus voltage must be zero (dead bus) for this test to be functional. Verify that the K25A relay is functional by probing screws 5 and 6 on TTUR.

## Synchronization Simulation

### ➤ To simulate a synchronization

- 1 Disable the breaker
- 2 Establish the center frequency of the PPRO PLL; this depends on the VPRO configuration, under J3:IS200TREx, signal K25A\_Fdbk, ReferFreq.
  - a If ReferFreq is configured PR\_Std, and <P> is configured for a single shaft machine, then apply rated speed (frequency) to input PulseRate1; that is SPRO screw pairs 31/32, 37/38, and 43/44.
  - b If ReferFreq is configured PR\_Std and <P> is configured for a multiple shaft machine, then apply rated speed (frequency) to input PulseRate 2, that is SPRO screw pairs 33/34, 39/40, and 45/46.
  - c If ReferFreq is configured SgSpace, force PPRO signal space output DriveRef to 50 or 60 (Hz), depending on the system frequency.
- 3 Apply the bus voltage, a nominal 115 V ac, 50/60 Hz, to TTUR screws 19 and 20, and to SPRO screws 3 and 4.
- 4 Apply the generator voltage, a nominal 115 V ac, adjustable frequency, to TTUR screws 17 and 18 and to SPRO screws 1 and 2. Adjust the frequency to a value giving positive slip, that is PTUR signal GenFreqDiff of 0.1 to 0.2 Hz. (10 to 5 sec scope).
- 5 Force the following signals to the TRUE state:
  - PTUR, Sync\_Perm, then K25P should pick up
  - PTUR, Sync\_Perm\_AS, then K25 should pulse when the voltages are in phase
  - PPRO, SynCK\_Perm, then K25A should pulse when the voltages are in phase
- 6 Verify that the TTUR breaker close interface circuit, screws 3 to 7, is being made (contacts closed) when the voltages are in phase.
- 7 Run a trend chart on the following signals:
  - PPRO: GenFreqDiff, GenPhaseDiff, L25A\_Command, K25A\_Fdbk
  - PTUR: GenFreqDiff, GenPhaseDiff, L25\_Command, CB\_K25\_PU, CB\_K25A\_PU
- 8 Use an oscilloscope, voltmeter, synchroscope, or a light to verify that the relays are pulsing at approximately the correct time.



- 9 Examine the trend chart and verify that the correlation between the phase and the close commands is correct.
- 10 Increase the slip frequency to 0.5 Hz and verify that K25 and K25A stop pulsing and are open.

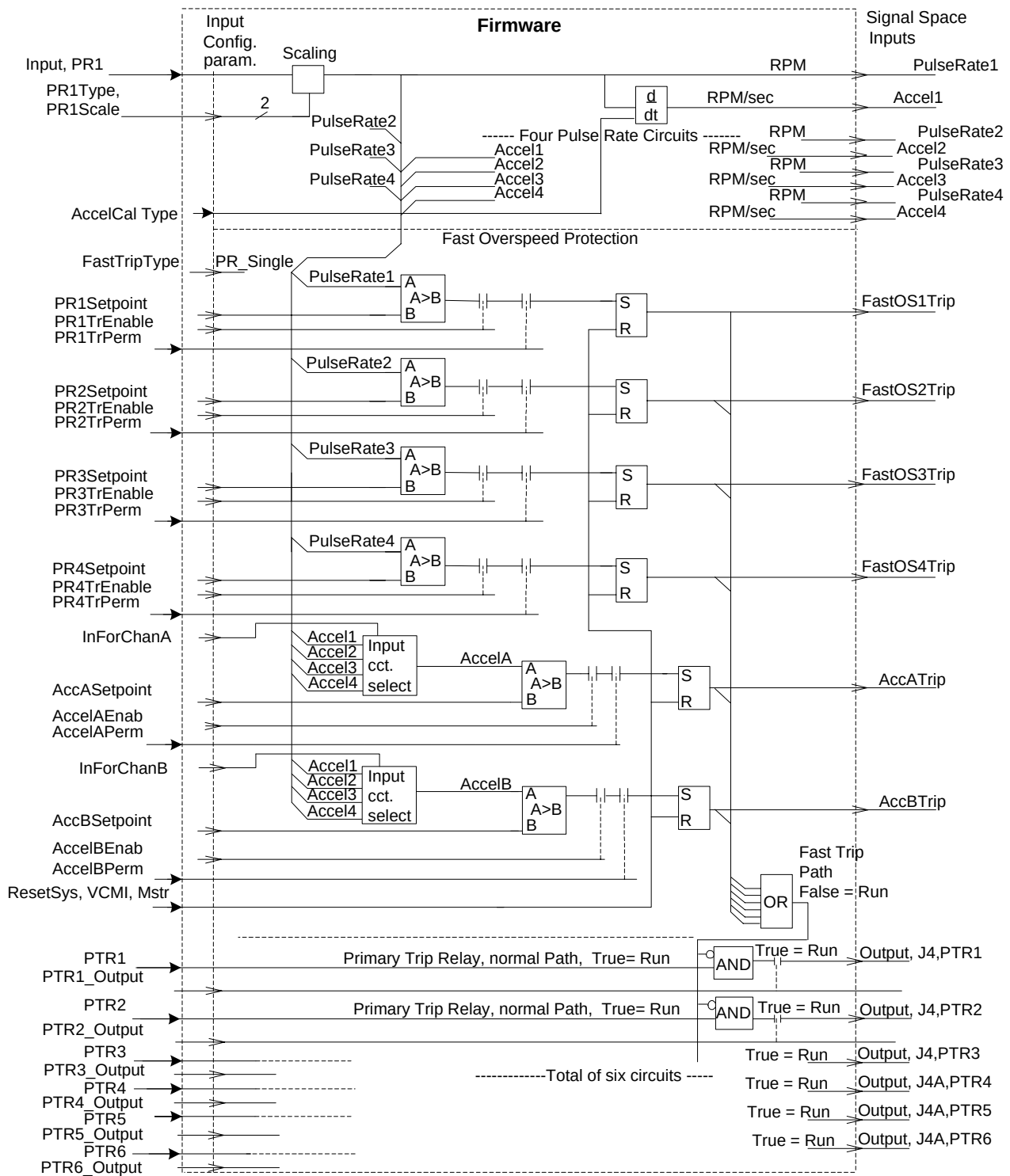
Return the slip frequency to 0.1 to 0.2 Hz, and verify that K25 and K25A are pulsing. Reduce the generator voltage to 40 V ac and verify that K25 and K25A stop pulsing and are open.

### ***Fast Overspeed Trip***

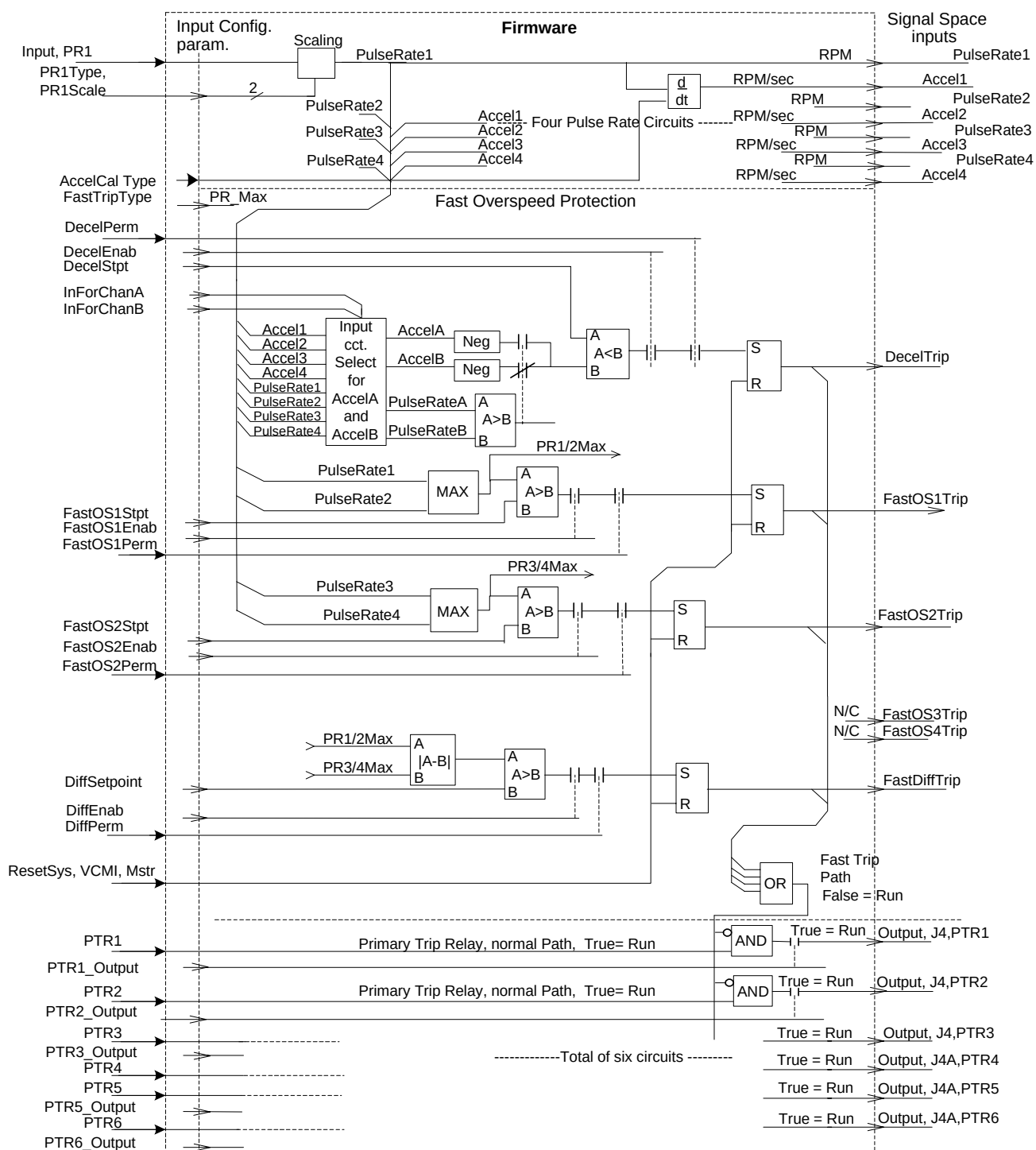
In special cases where a faster overspeed trip system is required, the PTUR Fast Overspeed Trip algorithms can be enabled. The system employs a speed measurement algorithm using a calculation for a predetermined tooth wheel. Two overspeed algorithms are available as follows:

- **PR\_Single** uses two redundant PTURs by splitting up the two redundant PR transducers, one to each board. PR\_Single provides redundancy and is the preferred algorithm for LM gas turbines.
- **PR\_Max** uses one PTUR connected to the two redundant PR transducers. PR\_Max allows broken shaft and deceleration protection without the risk of a nuisance trip if one transducer is lost.

The fast trips are linked to the output trip relays with an OR-gate. PTUR computes the overspeed trip instead of the controller, so the trip is very fast. The time from the overspeed input to the completed relay dropout is 30 ms or less.



Fast Overspeed Algorithm, PR-Single



Fast Overspeed Algorithm, PR-Max

## ***Shaft Voltage and Current Monitor***

Bearings can be damaged by the flow of electrical current from the shaft to the case. This current can occur for several reasons:

- A static voltage can be caused by droplets of water being thrown off the last stage buckets in a steam turbine. This voltage builds up until a discharge occurs through the bearing oil film.
- An ac ripple on the dc generator field can produce an ac voltage on the shaft with respect to ground through the capacitance of the field winding and insulation. Note that both of these sources are weak, so high impedance instrumentation is used to measure these voltages with respect to ground.
- A voltage can be generated between the ends of the generator shaft due to dissymmetries in the generator magnetic circuits. If the insulated bearings on the generator shaft breakdown, the current flows from one end of the shaft through the bearings and frame to the other end. Brushes can be used to discharge damaging voltage buildup, and a shunt should be used to monitor the current flow.

The turbine control continuously monitors the shaft to ground voltage and current, and alarms excessive levels. There is an ac test mode and a dc test mode. The ac test applies an ac voltage to test the integrity of the measuring circuit. The dc test checks the continuity of the external circuit, including the brushes, turbine shaft, and the interconnecting wire.

---

**Note** The dc test is driven from the R controller only. If the R controller is down, this test cannot be run successfully.

---

## ***Flame Detectors***

When used with the TRPG primary trip board, signals from eight Geiger-Mueller<sup>®</sup> flame detectors are monitored. With no flame present the detector charges up to the supply voltage, but presence of the flame causes the detector to charge to a level and then discharge through the TRPG board. As the flame intensity increases, the discharge frequency increases. When the detector discharges, the I/O pack/board and TRPG convert the discharged energy into a voltage pulse. The pulse rate varies from 0 to 1,000 pulses/sec. These voltage pulses are fanned out to all three modules. Voltage pulses above 2.5 volts generate a logic high, and the pulse rate over a 40 ms time period is measured in a counter.

## ***ID Line***

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-62 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## ***Power Management***

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## **Status LEDs**

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## **Connectors**

- A DC-62 pin connector on the underside of the I/O pack connects directly to a discrete output terminal board.
- An RJ45 Ethernet connector named ENET1 on the pack side is the primary system interface.
- A second RJ45 Ethernet connector named ENET2 on the pack side is the redundant or secondary system interface.

---

**Note** The terminal board provides fused power output from a power source that is applied directly to the terminal board, not through this pack connector.

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## ***Specifications***

The following table gives information specific to the PTUR.

| <b>Item</b>                            | <b>PTUR Specification</b>                                                                                                                                                                                                                                                          |
|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs                       | 4 Passive speed pickups<br>1 Shaft voltage and 1 current measurement<br>1 Generator and 1 bus voltage<br>Generator breaker status<br>Eight flame detectors from TRPG                                                                                                               |
| Number of outputs                      | Automatic synchronizing control to main breaker<br>Primary trip solenoid interface, 3 outputs to TRPG                                                                                                                                                                              |
| Speed sensor range                     | MPU pulse rate range 2 Hz to 20 kHz                                                                                                                                                                                                                                                |
| Speed sensor accuracy                  | MPU pulse rate accuracy 0.05% of reading                                                                                                                                                                                                                                           |
| Speed sensor input circuit sensitivity | 27 mV pk (detects 2 rpm speed)                                                                                                                                                                                                                                                     |
| Shaft voltage monitor                  | Voltage signal is $\pm 5$ V dc pulses from 0 to 2,000 Hz                                                                                                                                                                                                                           |
| Shaft voltage dc test                  | Applies a 5 V dc source to test integrity of the circuit. Circuit reads a differential resistance between 0 and 150 $\Omega$ within $\pm 5$ $\Omega$ . Readings above 50 $\Omega$ indicate a fault.<br>Returned signal is filtered to provide 40 dB of noise attenuation at 60 Hz. |
| Shaft voltage ac test                  | Applies a test voltage of 1 kHz to the input of the PTUR shaft voltage circuit (R module only).                                                                                                                                                                                    |
| Shaft current input                    | Measures ac voltage up to 0.1 V pp                                                                                                                                                                                                                                                 |
| Generator and bus voltage sensors      | Two single phase potential transformers, with secondary output supplying a nominal 115 V rms.<br>Each input has less than 3 VA of loading. Allowable voltage range for sync is 75 to 130 V rms.                                                                                    |
| Synchronizing measurements             | Frequency accuracy 0.05% over 45 to 66 Hz range.<br>Zero crossing of the inputs is monitored on the rising slope.<br>Phase difference measurement is better than $\pm 1$ degree.                                                                                                   |
| Contact voltage sensing                | 20 V dc indicates high and 6 V dc indicates low. Each circuit is optically isolated and filtered for 4 ms.                                                                                                                                                                         |
| <b>Physical</b>                        |                                                                                                                                                                                                                                                                                    |
| Size                                   | 8.26 cm High x 4.19 cm Wide x 12.1 cm Deep (3.25 in. x 1.65 in. x 4.78 in.)                                                                                                                                                                                                        |
| Temperature                            | -30 to 65°C (-22 to +149 °F)                                                                                                                                                                                                                                                       |
| Technology                             | Surface mount                                                                                                                                                                                                                                                                      |

## Diagnostics

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware.
- Continuous monitoring of the internal power supplies for correct operation.
- L3BKR\_GXS – the Sync Check Relay on TTUR is Slow.
- L3BKR\_GES – the Auto Sync Relay on TTUR is Slow.
- Breaker #1 Slower than Adjustment Limit Allows.
- Breaker #2 Slower than Adjustment Limit Allows.
- Synchronization Trouble – the K25 Relay on TTUR Locked Up.
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.
- Diagnostic information includes status of the solenoid relay driver, contact, high and low flame detector voltage, and the sync relays. If any one of the signals goes unhealthy a composite diagnostic alarm, L3DIAG\_PTUR occurs.

The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy. Details of the individual diagnostics are available from the toolbox.

## Configuration

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**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

---

| Parameter          | Description                                                                    | Choices                   |
|--------------------|--------------------------------------------------------------------------------|---------------------------|
| PTUR_Mod_Cfg       |                                                                                |                           |
| System Limits      | Enable or disable all system limit checking                                    | Enable, disable           |
| SMredundancy       | Used to determine how shaft monitor testing is controlled if a TMR application | Simplex or TMR            |
| Redundancy         | Used to specify the voting mode for the card                                   | Simplex or TMR            |
| AccelCalType       | Select acceleration calculation time (msec)                                    | 10 ... 100                |
| FastTripType       | Select fast trip algorithm                                                     | Unused, PR_Single, PR_Max |
| DecelStpt          | Deceleration setpoint, RPM/sec                                                 | 0 ... 1500                |
| Fast Trip Type (2) |                                                                                |                           |
| DecelEnab          | Deceleration enable                                                            | Disable, Enable           |
| FastOS1Stpt        | Fast Overspeed trip #1 setpoint, Max (PR1, PR2), RPM                           | 0 .. 20000                |
| FastOS1Enabl       | Fast Overspeed trip #1 enable                                                  | Disable, Enable           |
| FastOS2Stpt        | Fast Overspeed trip #2 setpoint, Max (PR3, PR4), RPM                           | 0 .. 20000                |
| FastOS2Enabl       | Fast Overspeed trip #2 enable                                                  | Disable, Enable           |
| DiffSetpoint       | Difference Speed trip setpoint, RPM                                            | 0 .. 20000                |
| DiffEnable         | Difference Speed trip, enable                                                  | Disable, Enable           |
| PR1Setpoint        | Fast Overspeed trip #1, setpoint, PR1, RPM                                     | 0 .. 20000                |
| PR1TrEnable        | Fast Overspeed trip #1, enable                                                 | Disable, Enable           |
| AccASetpoint       | Acceleration trip setpoint, Change A, RPM/sec                                  | 0 .. 1500                 |

| Parameter        | Description                                                     | Choices                        |
|------------------|-----------------------------------------------------------------|--------------------------------|
| InForChanA       | Input change selection for Accel/Decel trip                     | Accel, Accel2, Accel3, Accel4. |
| DiagSo1PwrA      | When using TRPL/S, Sol Power, Bus A, Diagnostic enable.         | Enable, Disable                |
| PTUR_PR_Cfg      |                                                                 |                                |
| PRType           | Selects the type of pulse rate input, n (for proper resolution) | Unused, Speed, Flow, Speed_LM  |
| PRScale          | Pulses per revolution (outputs RPM)                             | 0 to 1,000                     |
| SysLim1Enabl     | Enable system limit 1 fault check                               | Enable, Disable                |
| SysLim1Latch     | Latch system limit 1 fault                                      | Latch, Not Latch               |
| SysLim1Type      | System limit 1 check type (>= or <=)                            | >= or <=                       |
| SysLimit1        | System limit 1 - RPM                                            | 0 to 20,000                    |
| SysLim2Enabl     | Enable system limit 2 fault check (as above)                    | Enable, Disable                |
| TMRDiffLimit     | Diag Limit, TMR input vote difference, in Eng units             | 0 to 20,000                    |
| PTUR_ShV_Cfg     |                                                                 |                                |
| SysLim1Enabl     | Enable system limit 1                                           | Enable, Disable                |
| SysLim1Latch     | Latch system limit 1 fault                                      | Latch, Not Latch               |
| SysLim1Type      | System limit 1 check type (>= or <=)                            | >= or <=                       |
| SysLimit1        | Select alarm level in frequency Hz                              | 0 to 100                       |
| SysLim2Enabl     | Select system limit 2 (as above)                                | Enable, Disable                |
| TMRDiffLimit     | Diag limit, TMR input vote difference, in Hertz                 | 0 to 100                       |
| PTURShC_Cfg      |                                                                 |                                |
| ShuntOhms        | Shunt ohms                                                      | 0 to 100                       |
| Shunt Limit      | Shunt maximum test ohms                                         | 0 to 100                       |
| Brush Limit      | Shaft (Brush) maximum ohms                                      | 0 to 100                       |
| SysLim1Enable    | Select system limit 1                                           | Enable, Disable                |
| SysLim1Latch     | Select whether alarm will latch                                 | Latch, Not Latch               |
| SysLim1Type      | Select type of alarm initiation                                 | >= or <=                       |
| SysLimit1        | Current Amps, select alarm level in Amps                        | 0 to 100                       |
| SysLim2Enable    | Select system limit 2                                           | Enable, Disable                |
| PTUR_PT_Cfg      |                                                                 |                                |
| PT_Input         | PT primary in Eng units (kv or percent) for PT_Output           | 0 to 1,000                     |
| PT_Output        | PT output in volts rms, for PT_Input - typically 115            | 0 to 150                       |
| SysLim1          | Select alarm level in k volts rms                               | 0 to 1,000                     |
| SysLim2          | Select alarm level in k volts rms                               | 0 to 1,000                     |
| PTUR_CB_Cfg      |                                                                 |                                |
| System Frequency | Select frequency in Hz                                          | 50 or 60                       |
| CB1CloseTime     | Breaker 1 closing time, ms                                      | 0 to 1,000                     |
| CB1 AdaptLimit   | Breaker 1 self adaptive limit, ms                               | 0 to 1,000                     |
| CB1 AdaptEnabl   | Enable breaker 1 self adaptive adjustment                       | Enable, Disable                |
| CB1FreqDiff      | Breaker 1 special window frequency difference, Hz               | 0.15 .. 0.66                   |
| CB1PhaseDiff     | Breaker 1 special window phase Diff, degrees                    | 0 to 20                        |
| CB2CloseTime     | Breaker 2 closing time, ms (as above)                           | 0 to 1,000                     |
| PTUR_Flm_Cfg     |                                                                 |                                |
| FlmDetTime       | Flame detector time interval                                    | 0.160, 0.080, 0.040 sec        |



| Parameter      | Description                                                       | Choices         |
|----------------|-------------------------------------------------------------------|-----------------|
| FlameLimitHI   | Flame threshold LimitHI (HI detection cnts means LOW sensitivity. | 0 ... 160       |
| Flame_Det      | Flame detector used/unused                                        | Used, Unused    |
| PTUR_Rly1_Cfg  |                                                                   |                 |
| PTR_Output     | Primary protection relay used/unused                              | Unused, used    |
| DiagVoteEnab   | Enable voting disagreement diagnostic                             | Enable, Disable |
| PTUR_Estop_Cfg |                                                                   |                 |
| DiagVoteEnab   | Enable voting disagreement diagnostic                             | Enable, Disable |
| IS220PTUR      | Distributed I/O turbine module                                    |                 |

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**Note** When *FlameLimHi* and *FlameLimLo* are set to the default value of 0, flame detection is turned off and the flame present signal *FDn\_Flame* is always true.

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#### *PTUR Auto Sync Signal Space Interface*

##### **PTUR Signal Space Output**

|              |                            |                                                                                                                  |
|--------------|----------------------------|------------------------------------------------------------------------------------------------------------------|
| Sync_Perm_AS | Auto sync permissive       | Traditionally known as L83AS                                                                                     |
| Sync_Perm    | Sync permissive mode, L25P | Traditionally known as L25P; interface to control the K25P relay                                                 |
| Sync_Monitor | Auto Sync monitor mode     | Traditionally known as L83S_MTR; enables the Auto Sync function, except it blocks the K25 relays from picking up |
| Sync_Bypass1 | Auto Sync bypass           | Traditionally known as L25_BYPASS; to pickup L25 for Dead Bus or Manual Sync                                     |
| Sync_Bypass0 | Auto Sync bypass           | Traditionally known as L25_BYPASSZ; to pickup L25 for Dead Bus or Manual Sync                                    |
| CB2 Selected | #2 Breaker is selected     | Traditionally known as L43SAUTO2; to use the breaker close time associated with Breaker #2                       |
| AS_WIN_SEL   | Special Auto Sync window   | New function, used on Synchronous condenser applications to give a more permissive window                        |
| Sync_Reset   | Auto Sync reset            | Traditionally known as L86MR_TCEA; to reset the Sync Lockout function                                            |

##### **PTUR Signal Space Inputs**

|             |                                                                               |                                                                                                                                                                                                                              |
|-------------|-------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ckt_BKR     | Breaker State (feedback)                                                      | Traditionally known as L52B_SEL                                                                                                                                                                                              |
| CB_Volts_OK | Breaker Closing Coil Voltage is present                                       | Used in diagnostics                                                                                                                                                                                                          |
| CB_K25P_PU  | Breaker Closing Coil Voltage is present downstream of the K25P relay contacts | Used in diagnostics                                                                                                                                                                                                          |
| CB_K25_PU   | Breaker Closing Coil Voltage is present downstream of the K25 relay contacts  | Used in diagnostics                                                                                                                                                                                                          |
| CB_K25A_PU  | Breaker Closing Coil Voltage is present downstream of the K25A relay contacts | Used in diagnostics                                                                                                                                                                                                          |
| Gen_Sync_LO | Sync Lock out                                                                 | Traditionally known as L30AS1 or L30AS2; it is a latched signal requiring a reset to clear (Sync_Reset). It detects a K25 relay problem (picked up when it should be dropped out) or a slow Sync Check (relay K25A) function |
| L25_Comand  | Breaker Close Command to the K25 relay                                        | Traditionally known as L25                                                                                                                                                                                                   |
| GenFreq     | Generator frequency                                                           | Hz                                                                                                                                                                                                                           |
| BusFreq     | Bus frequency                                                                 | Hz                                                                                                                                                                                                                           |

## PTUR Signal Space Inputs

|                 |                                                        |                                  |
|-----------------|--------------------------------------------------------|----------------------------------|
| GenVoltsDiff    | Difference Voltage between the Generator and the Bus   | Engineering units, kV or percent |
| GenFreqDiff     | Difference Frequency between the Generator and the Bus | Hz                               |
| GenPhaseDiff    | Difference Phase between the Generator and the Bus     | Degree                           |
| CB1CloseTime    | Breaker #1 measured close time                         | ms                               |
| CB2CloseTime    | Breaker #2 measured close time                         | ms                               |
| GenPT_Kvolts    | Generator Voltage                                      | Engineering units, kV or percent |
| BusPT_Kvolts    | Bus Voltage                                            | Engineering units, kV or percent |
| J4:IS200TRPGH1A | TRPG terminal board, 8 flame detectors                 | Connected, not connected         |

| Board Points Signals | Description - Point Edit                         | Direction | Type  |
|----------------------|--------------------------------------------------|-----------|-------|
| L3DIAG_PTUR          | I/O Diagnostic Indication                        | Input     | BIT   |
| LINK_OK_PTUR         | I/O Link Okay Indication                         | Input     | BIT   |
| ATTN_PTUR            | I/O Attention Indication                         | Input     | BIT   |
| ShShntTst_OK         | Shaft voltage monitor shunt test OK              | Input     | BIT   |
| ShBrshTst_OK         | Shaft voltage brush test OK                      | Input     | BIT   |
| CB_Volts_OK          | L3BKR_VLT circuit breaker coil voltage available | Input     | BIT   |
| CB_K25P_PU           | L3BKR_PERM sync permissive relay picked up       | Input     | BIT   |
| CB_K25_PU            | L3KBR_GES auto sync relay picked up              | Input     | BIT   |
| CB_K25A_PU           | L3KBR_GEX sync check relay picked up             | Input     | BIT   |
| Gen_Sync_LO          | Generator sync trouble (lockout)                 | Input     | BIT   |
| L25_Command          | -----                                            | Input     | BIT   |
| Kq1_Status           | -----                                            | Input     | BIT   |
| :                    | :                                                | Input     | BIT   |
| Kq6_Status           | -----                                            | Input     | BIT   |
| FD1_Flame            | -----                                            | Input     | BIT   |
| :                    | :                                                | Input     | BIT   |
| FD16_Flame           | -----                                            | Input     | BIT   |
| SysLim1PR1           | -----                                            | Input     | BIT   |
| :                    | :                                                | Input     | BIT   |
| SysLim1PR4           | -----                                            | Input     | BIT   |
| SysLim1SHV           | Ac shaft voltage frequency high L30TSVH          | Input     | BIT   |
| SysLim1SHC           | Ac shaft current high L30TSCH                    | Input     | BIT   |
| SysLim1GEN           | -----                                            | Input     | BIT   |
| SysLim1BUS           | -----                                            | Input     | BIT   |
| SysLim2PR1           | (same set as for Limit1 above)                   | Input     | BIT   |
| GenFreq              | Hz frequency                                     | Input     | FLOAT |
| BusFreq              | Hz frequency                                     | Input     | FLOAT |
| GenVoltsDiff         | KiloVolts rms-Gen Low is negative                | Input     | FLOAT |
| Gen Freq Diff        | Slip Hz-Gen Slow is negative                     | Input     | FLOAT |
| Gen Phase Diff       | Phase Degrees-Gen Lag is negative                | Input     | FLOAT |
| CB1CloseTime         | Breaker #1 close time in milliseconds            | Input     | FLOAT |
| CB2CloseTime         | Breaker #2 close time in milliseconds            | Input     | FLOAT |
| Accel1               | RPM/SEC                                          | Input     | FLOAT |
| :                    | :                                                | Input     | FLOAT |

| Board Points | Signals | Description - Point Edit            | Direction | Type  |
|--------------|---------|-------------------------------------|-----------|-------|
| Accel4       |         | RPM/SEC                             | Input     | FLOAT |
| FImDetPwr1   |         | 335 V dc                            | Input     | FLOAT |
| ShTestAC     |         | L97SHAFT_AC SVM_AC_TEST             | Output    | BIT   |
| ShTestDC     |         | L97SHAFT_DC SVM_DC_TEST             | Output    | BIT   |
| FD1_Level    |         | 1 = high detection counts level     | Output    | BIT   |
| :            | :       |                                     | Output    | BIT   |
| FD16_Level   |         | 1 = high detection counts level     | Output    | BIT   |
| Sync_Perm_AS |         | L83AS - auto sync permissive        | Output    | BIT   |
| Sync_Perm    |         | L25P - sequencing sync permissive   | Output    | BIT   |
| Sync_Monitor |         | L83S_MTR - monitor mode             | Output    | BIT   |
| Sync_Bypass1 |         | L25_BYP-1 = auto aync bypass        | Output    | BIT   |
| Sync_Bypass0 |         | L25_BYPZ-0 = auto sync permissive   | Output    | BIT   |
| CB2_Selected |         | L43SAUT2 - 2nd breaker selected     | Output    | BIT   |
| AS_Win_Sel   |         | L43AS_WIN - special window selected | Output    | BIT   |
| Sync_Reset   |         | L86MR_SYNC - sync trouble reset     | Output    | BIT   |
| Kq1          |         | L20PTR1 - primary trip relay        | Output    | BIT   |
| :            | :       |                                     | Output    | BIT   |
| Kq6          |         | L20PTR6 - primary trip relay        | Output    | BIT   |

## Alarms

### PTUR Specific Alarms

The following alarms are specific to the PTUR I/O pack.

| Alarm ID | Alarm Description                            | Possible Cause                                                                                                                                                                                                           | Solution                                                                                                                             |
|----------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 32-37    | Solenoid [ ] Relay driver Feedback Incorrect | I/O pack monitors the relay command for correct state and termination into the expected trip card impedance. The I/O pack internal feedback of relay command output does not match the desired state.                    | Check mounting of I/O pack on terminal board. Check cable from TTUR to trip card if used. Replace I/O pack.                          |
| 38-43    | Solenoid [ ] Contact Feedback Incorrect      | The contact state feedback from the trip board does not match the commanded state.                                                                                                                                       | Check mounting of I/O pack on terminal board. Check cable from TTUR to TRPG. Check operation of relay.                               |
| 44-45    | TRPG 1 Solenoid Power Absent                 | I/O pack has detected the absence of Solenoid power as indicated by the connected TRPG board.                                                                                                                            | Power may not be coming into TRPX on the J1 connector, or the monitoring circuit on TRPX is bad, or the cabling to TRPX is at fault. |
| 46,48    | TRPG 1 Flame Detect Volts Low at [ ] Volts   | Nominal 335v DC power comes into TRPG via J3, J4, and J5. If the voltage is less than 314.9 V dc this fault is declared.                                                                                                 | Check the voltage on TRPG. If the voltage is above 314.9V, the monitoring circuitry on TRPG or the cabling to TRPG is suspect.       |
| 47,49    | TRPG 1 Flame Detect Volts High at [ ] Volts  | This power comes into TRPG via J3, J4, and J5. If the voltage is greater than 355.1 V dc this fault is declared. If the voltage is below this value, the monitoring circuitry on TRPG or the cabling to TRPG is suspect. | Check the voltage on TRPG. If the voltage is below 355V the monitoring circuitry on TRPG or the cabling to TRPG is suspect.          |
| 50       | L3BKRGXS – Sync Check Relay Is Slow          | The Sync check relay I3BKRGXS, known as K25A, on TTUR is suspect.                                                                                                                                                        |                                                                                                                                      |
| 51       | L3BKRGES – Auto Sync Relay Is Slow           | The Auto Sync relay I3BKRGES, also known as K25, on TTUR is suspect.                                                                                                                                                     |                                                                                                                                      |

| Alarm ID | Alarm Description                                      | Possible Cause                                                                                                                                                                                      | Solution                                                                                                                                                                                                |
|----------|--------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 52-53    | Breaker Slower Than Adjustment Limit Allows            | The breaker is experiencing a problem, or the operator should consider changing the configuration (both nominal close time and self-adaptive limit in ms can be configured).                        | Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack.                                                                     |
| 54       | Synchronization Trouble K25 Relay Locked Up            | K25 on TTUR is most likely stuck closed, or the contacts are welded.                                                                                                                                |                                                                                                                                                                                                         |
| 55       | Card and Configuration File Incompatibility            | An incompatibility has been detected between the pack firmware and the configuration information.                                                                                                   |                                                                                                                                                                                                         |
| 56       | Term Board On J5x not supported (deprecated)           | Check your configuration.                                                                                                                                                                           |                                                                                                                                                                                                         |
| 57       | Term Board and ToolboxST Incompatibility               | An incompatibility has been detected between I/O pack and the terminal board it is mounted on.                                                                                                      | Review hardware compatibility information and correct if necessary. Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack. |
| 58       | Aux Term Brd and ToolboxST Incompatibility             | An incompatibility has been detected between I/O pack and the trip terminal board that is cable connected to I/O pack.                                                                              | Review hardware compatibility information and correct if necessary. Confirm correct installation of ToolboxST. Rebuild application and download firmware and application code to the affected I/O pack. |
| 59       | Term Board on J4a not supported (deprecated)           | Check your configuration.                                                                                                                                                                           | The TTUR or I/O pack must be changed to a compatible combination.                                                                                                                                       |
| 60       | Term Board TTUR and card I/O pack Incompatibility      | There is a compatibility problem between I/O pack and TTUR.                                                                                                                                         |                                                                                                                                                                                                         |
| 61       | TRPL/S, Solenoid Power, Bus A, Absent                  | Cabling problem or solenoid power source                                                                                                                                                            |                                                                                                                                                                                                         |
| 62       | TRPL/S, Solenoid Power, Bus B, Absent                  | Cabling problem or solenoid power source                                                                                                                                                            |                                                                                                                                                                                                         |
| 63       | TRPL/S, Solenoid Power, Bus C, Absent                  | Cabling problem or solenoid power source                                                                                                                                                            |                                                                                                                                                                                                         |
| 64-66    | TRPL/S, Solenoid [ ] Voltage Mismatch                  | PTR or ETR relays, or defective feedback circuitry                                                                                                                                                  |                                                                                                                                                                                                         |
| 67       | Overspeed Trip Generated                               | I/O pack has observed a speed input that exceeds the settings for overspeed.                                                                                                                        | Determine the cause of the overspeed condition- Input signal, configuration, noise, etc..                                                                                                               |
| 70       | Reference Voltage out of limits                        | Every scan the I/O pack uses the internal analog/digital converter to read a precision voltage reference. This reference input exceeded the converter specified limits indicating a hardware fault. | The precision reference voltage, signal multiplexing, or A/D converter in the I/O pack has failed.                                                                                                      |
| 71       | Null Voltage out of limits                             | Every scan the I/O pack uses the internal analog/digital converter to read a zero voltage reference. This reference input exceeded the converter specified limits indicating a hardware fault.      | The signal multiplexing or A/D converter on the I/O pack has failed.                                                                                                                                    |
| 128-223  | Logic Signal [ ] Voting Mismatch                       | Voter disagreement detected between R,S & T controller                                                                                                                                              |                                                                                                                                                                                                         |
| 224-252  | Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ] | Voter disagreement detected between R,S & T controller                                                                                                                                              |                                                                                                                                                                                                         |

## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                             |
|-------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                                |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                           |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                                |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                                |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                                |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                         |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                              |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A .tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                             |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                               |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                 |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                 |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                             |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                      |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                  |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                 |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                 |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                   |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                            |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                      |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                   |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                           |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                              |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                               |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                       |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                               |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                   |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                   |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                              |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                                |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                   |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                              |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                                |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                            |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

## ***TTURH1C Primary Turbine Protection Input***

### ***Functional Description***

The Primary Turbine Protection Input (TTURH1C) terminal board works with the PTUR turbine I/O packs as part of the Mark\* VIe system. The inputs and outputs are as follows:

- 12 pulse rate devices sensing a toothed wheel to measure the turbine speed
- Generator voltage and bus voltage signals taken from potential transformers
- 125 V dc output to the main breaker coil for automatic generator synchronizing
- Inputs from shaft voltage and current sensors to measure induced shaft voltage and current
- Three overspeed trip signals to the trip board
- Additional I/O signals from the trip board

TTUR has three relays, K25, K25P, and K25A, that all have to close to provide 125 V dc power to close the main breaker 52G.

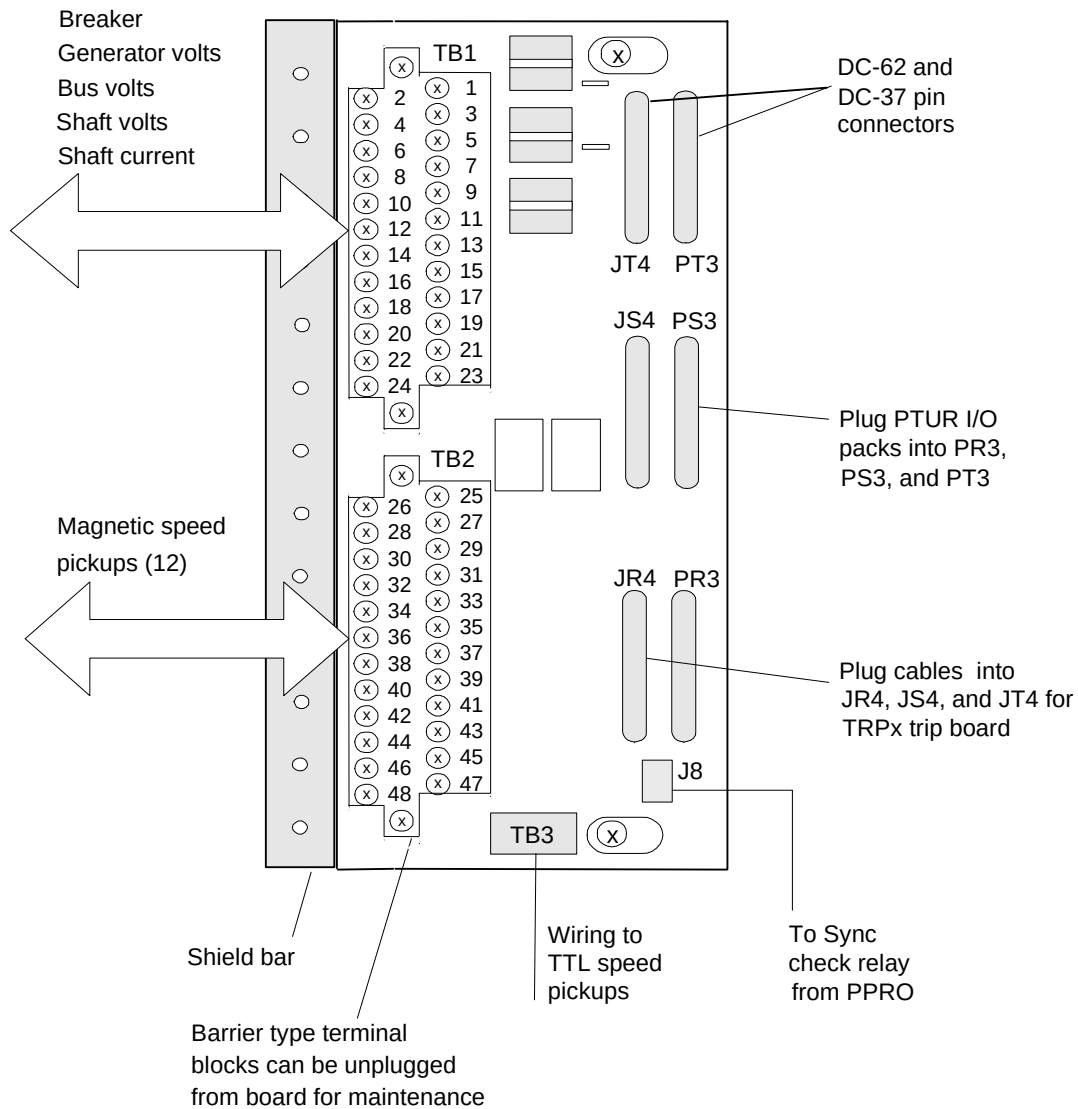
The signals to PTUR use the PR3 and JR4 connector for simplex systems. For TMR systems, signals fan out to the PR3, PS3, PT3, JR4, JS4, and JT4 connectors.

### ***Mark VI Systems***

TTURH1C cannot be used with the Mark VI system. For Mark VI, use the TTURH1B terminal board.

## Mark VIe Systems

TTURH1C supports connection of TRPG, TRPS, TRPA boards and accommodates PTUR I/O pack.

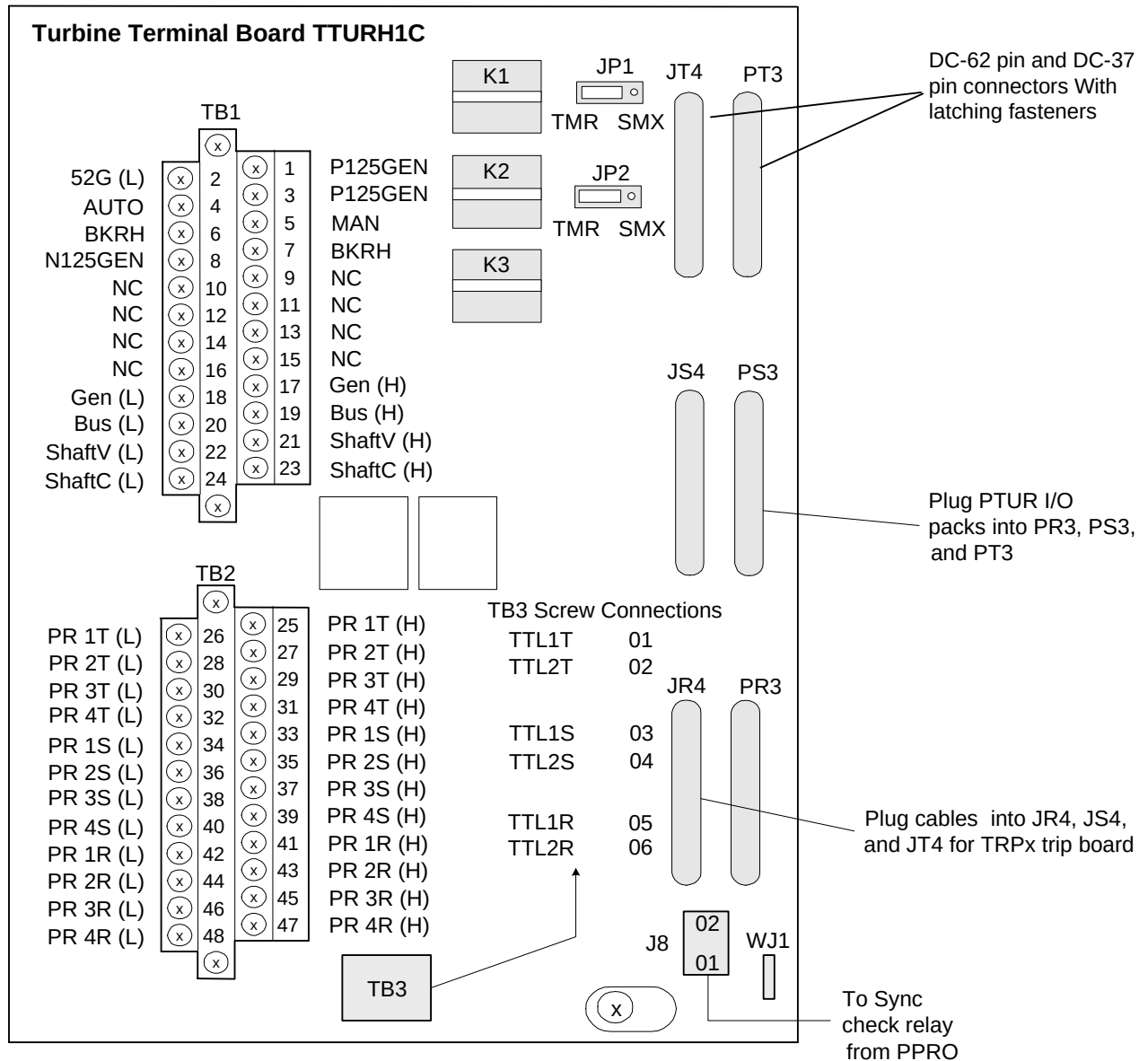


TTURH1C Turbine Terminal Board

## Installation

Pulse rate pick ups, shaft pick ups, potential transformers, and the breaker relay are wired to the two terminal blocks TB1 and TB2. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

Jumpers JP1 and JP2 select either simplex or TMR for relay drivers K25 and K25P. Removing wire jumper WJ1 isolates the K25A control line to the TRPX board. TB3 is for optional TTL connections to active speed pickups; these devices require an external power supply. Simplex systems use cable connectors PR3 and JR4. TMR systems use all six cable connectors.

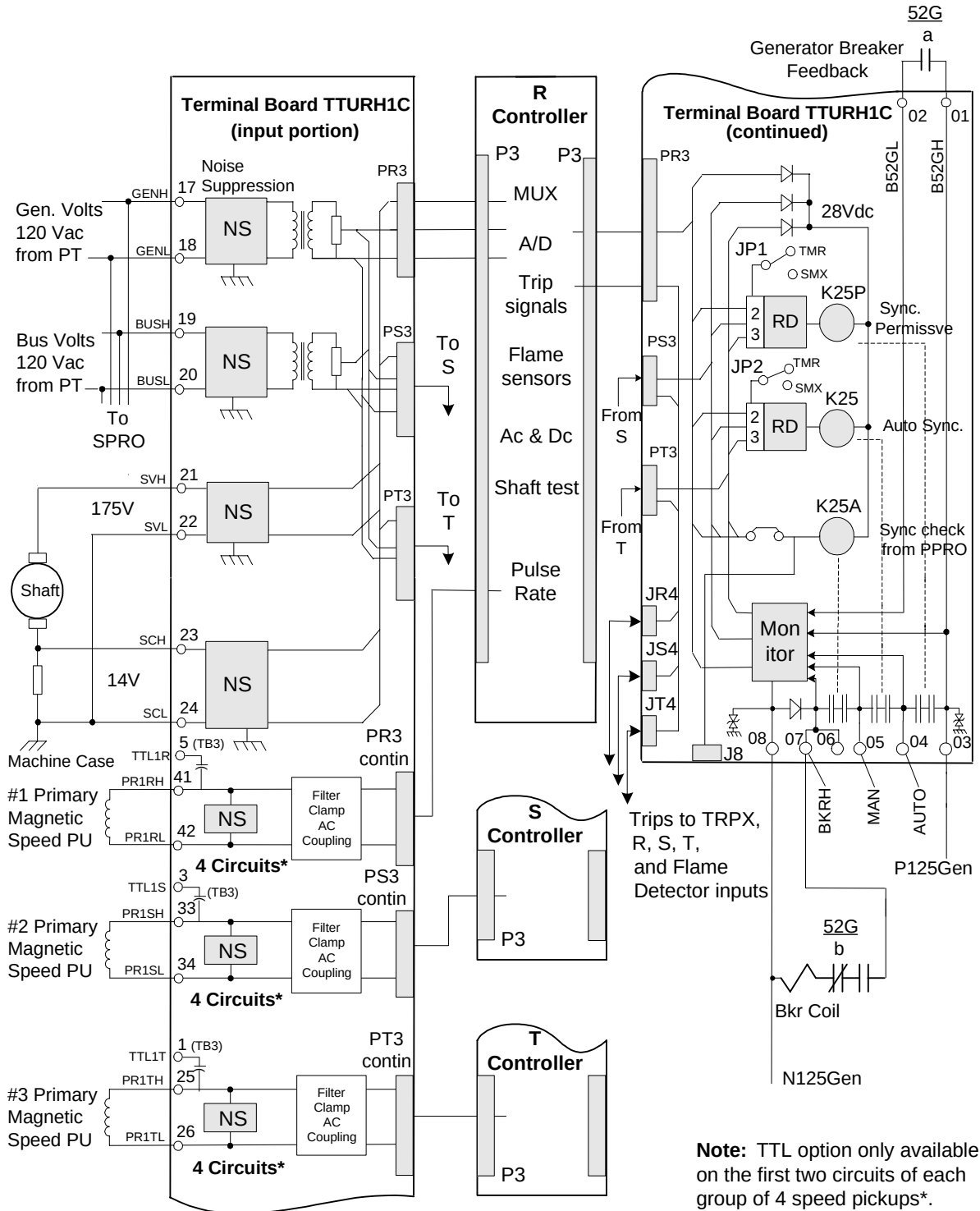


TTUR Terminal Board Wiring



## Operation

PTUR turbine control packs plug into TTURH1C as shown in the figure. Either one or three can be used. The TRPX trip board connects to the J4 connectors.



TTUR and Controller, TMR system

**Note** Passive or active Pulse rate devices can be used.

In the simplex application, up to four pulse rate signals may be used to measure turbine speed. Generator and bus voltages are brought into TTUR for automatic synchronizing in conjunction with PTUR, the turbine controller, and excitation system. TTUR has permissive generator synchronizing relays and controls the main breaker relay coil 52G.

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**Note** All three relays have two normally open contacts in series with the breaker close coil.

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In TMR applications, all inputs, except speed, fan to the three PTUR packs. Control signals coming into TTUR from R, S, and T are voted before they actuate permissive relays K25 and K25P. Relay K25A is controlled by the PPRO and TREG boards through J8.

## ***Specifications***

| <b>Item</b>                                | <b>Specification</b>                                                                                                                                                                                                                                                          |
|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs                           | 12 passive speed pickups<br>1 shaft voltage and 1 shaft current measurement<br>1 generator and 1 bus voltage. Generator breaker status contact.<br>Signal to K25A relay from PPRO                                                                                             |
| Number of outputs                          | Generator breaker coil, 5 A at 125 V dc                                                                                                                                                                                                                                       |
| Power supply voltage                       | Nominal 125 V dc to breaker coil                                                                                                                                                                                                                                              |
| MPU pulse rate range                       | 2 Hz to 20 kHz                                                                                                                                                                                                                                                                |
| MPU pulse rate accuracy                    | 0.05% of reading                                                                                                                                                                                                                                                              |
| MPU input circuit sensitivity              | 27 mV pk (detects 2 rpm speed)                                                                                                                                                                                                                                                |
| Shaft voltage monitor                      | Signal is frequency of $\pm 5$ V dc (0 – 1 MHz) pulses from 0 to 2,000 Hz                                                                                                                                                                                                     |
| Shaft voltage wiring                       | Up to 300 m (984 ft), with maximum two-way cable resistance of 15 $\Omega$                                                                                                                                                                                                    |
| Shaft voltage dc test                      | Applies a 5 V dc source to test integrity of the external turbine circuit and measures dc current flow.                                                                                                                                                                       |
| Shaft voltage ac test                      | Applies a test voltage of 1 kHz to the input of the PTUR shaft voltage circuit (R module only).                                                                                                                                                                               |
| Shaft current input                        | Measures shaft current in amps ac (shunt voltage up to 0.1 V pp)                                                                                                                                                                                                              |
| Generator and bus voltage sensors          | Two single phase potential transformers, with secondary output supplying a nominal 115 V rms<br><br>Each input has less than 3 VA of loading.<br>Each PT input is magnetically isolated with a 1,500 V rms barrier.<br>Cable length can be up to 1,000 ft. of 18 AWG wiring.  |
| Generator breaker circuits (synchronizing) | External circuits should have a voltage range within 20 to 140 V dc. The external circuit must include a NC breaker auxiliary contact to interrupt the current. Circuits are rated for NEMA class E creepage and clearance. 250 V dc applications require interposing relays. |
| Contact voltage sensing                    | 20 V dc indicates high and 6 V dc indicates low. Each circuit is optically isolated and filtered for 4 ms.                                                                                                                                                                    |
| <b>Physical</b>                            |                                                                                                                                                                                                                                                                               |
| Size                                       | 33.0 cm high x 17.8 cm wide (13 in x 7 in)                                                                                                                                                                                                                                    |
| Technology                                 | Surface mount                                                                                                                                                                                                                                                                 |
| Temperature                                | -30 to 65°C (-22 to +149 °F)                                                                                                                                                                                                                                                  |

## ***Diagnostics***

Diagnostic tests are made on the terminal board as follows:

- Feedback from the solenoid relay drivers is checked; if there is a problem with the control signal a fault is created.
- Feedback from the relay contacts; if there is a problem with the control signal a fault is created.
- Loss of solenoid power creates a fault.
- Slow sync check relay, slow auto sync relay, slow breaker, and locked up K25 relay; all of these create a fault.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG\_PTUR occurs. The diagnostic signals can be individually latched and then reset with the RESET\_DIA signal if they go healthy.
- Terminal board connectors have their own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by PTUR and a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

Jumpers JP1 and JP2 select either simplex (SMX) or TMR for relay drivers K25 and K25P. Wire jumper WJ1 is installed; removing this will isolate the K25A control line to the TRPX board. There are no switches on the board.

---

# ***TRPG Turbine Primary Trip***

## ***Functional Description***

The Gas Turbine Primary Trip (TRPG) terminal board is controlled by the Primary Turbine Protection controller (VTUR or PTUR). TRPG contains nine magnetic relays in three voting circuits to interface with three trip solenoids (ETDs). The TRPG works in conjunction with the TREG to form the primary and emergency sides of the interface to the ETDs. TRPG also accommodates inputs from eight Geiger-Mueller<sup>®</sup> flame detectors for gas turbine applications. There are two board types as follows:

- The H1A and H1B version for TMR applications has three voting relays per trip solenoid.
- The H2A and H2B version for simplex applications has one relay per trip solenoid.

### **Mark VI System**

In the Mark\* VI system, the TRPG works with the VTUR board and supports simplex and TMR applications. Cables with molded plugs connect TRPG to the VME rack where the VTUR board is located.

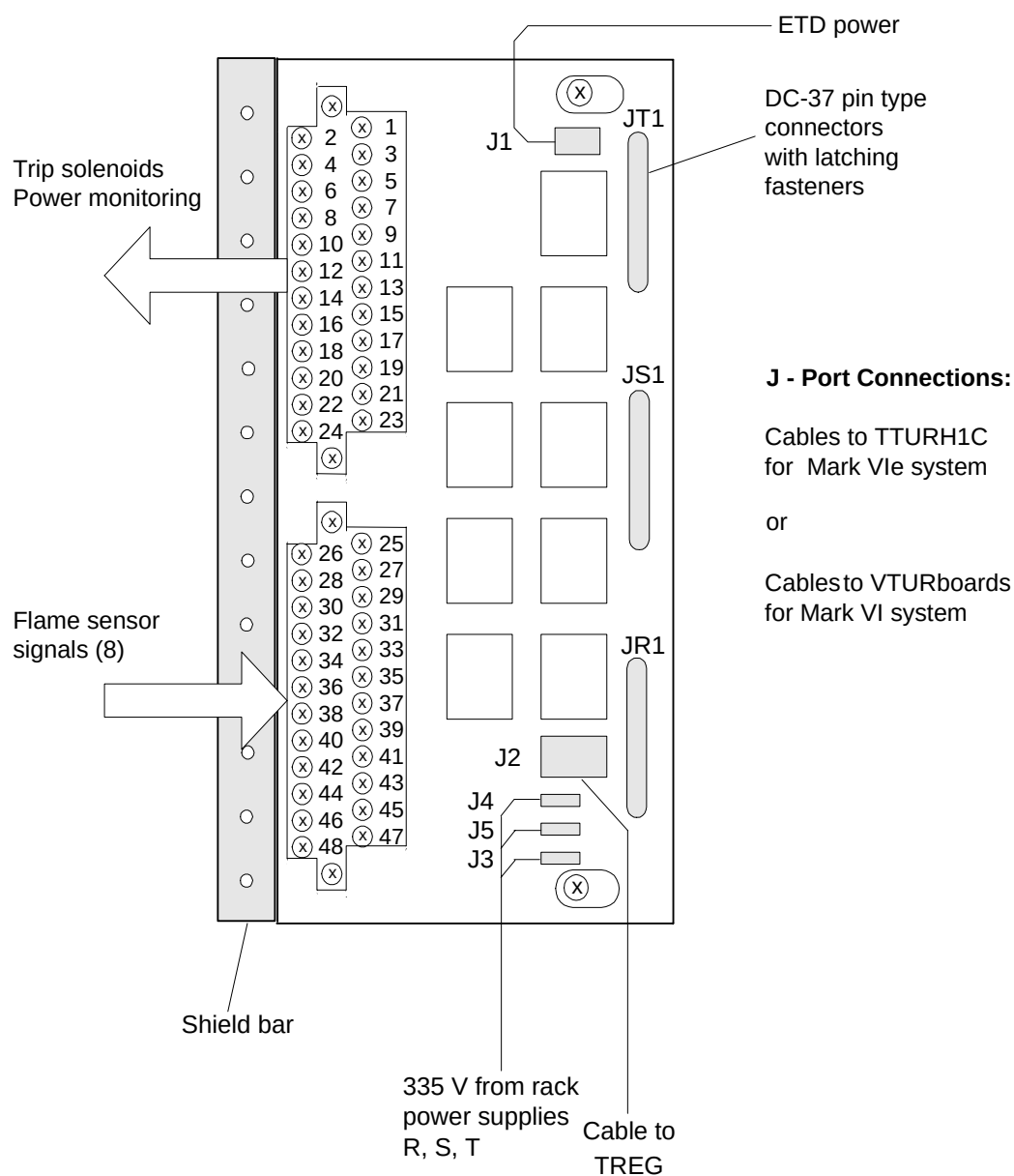
### **Mark VIe System**

In the Mark VIe system, the TRPG is controlled by the PTUR packs on TTURH1C and supports simplex and TMR applications. The I/O packs plug into the D-type connectors on TTURH1C, which is cabled to TRPG.

## Version Difference

| Board    | TMR | Simplex | Output contact,<br>125 V dc, 1 A | Output contact,<br>24 V dc, 3 A | 28 V Power<br>use |
|----------|-----|---------|----------------------------------|---------------------------------|-------------------|
| TRPGH1A* | Yes | No      | Yes                              | No                              | Normal            |
| TRPGH2A* | No  | Yes     | Yes                              | No                              | Normal            |
| TRPGH1B  | Yes | No      | Yes                              | Yes                             | Normal            |
| TRPGH2B  | No  | Yes     | Yes                              | Yes                             | Normal            |
| TRPGH3B  | Yes | No      | Yes                              | Yes                             | Special           |

\* H1A and H2A are not used for new applications. TRPGH3B features special handling of 28 V control power and is otherwise identical to a TRPGH1B. Consult factory for additional details.

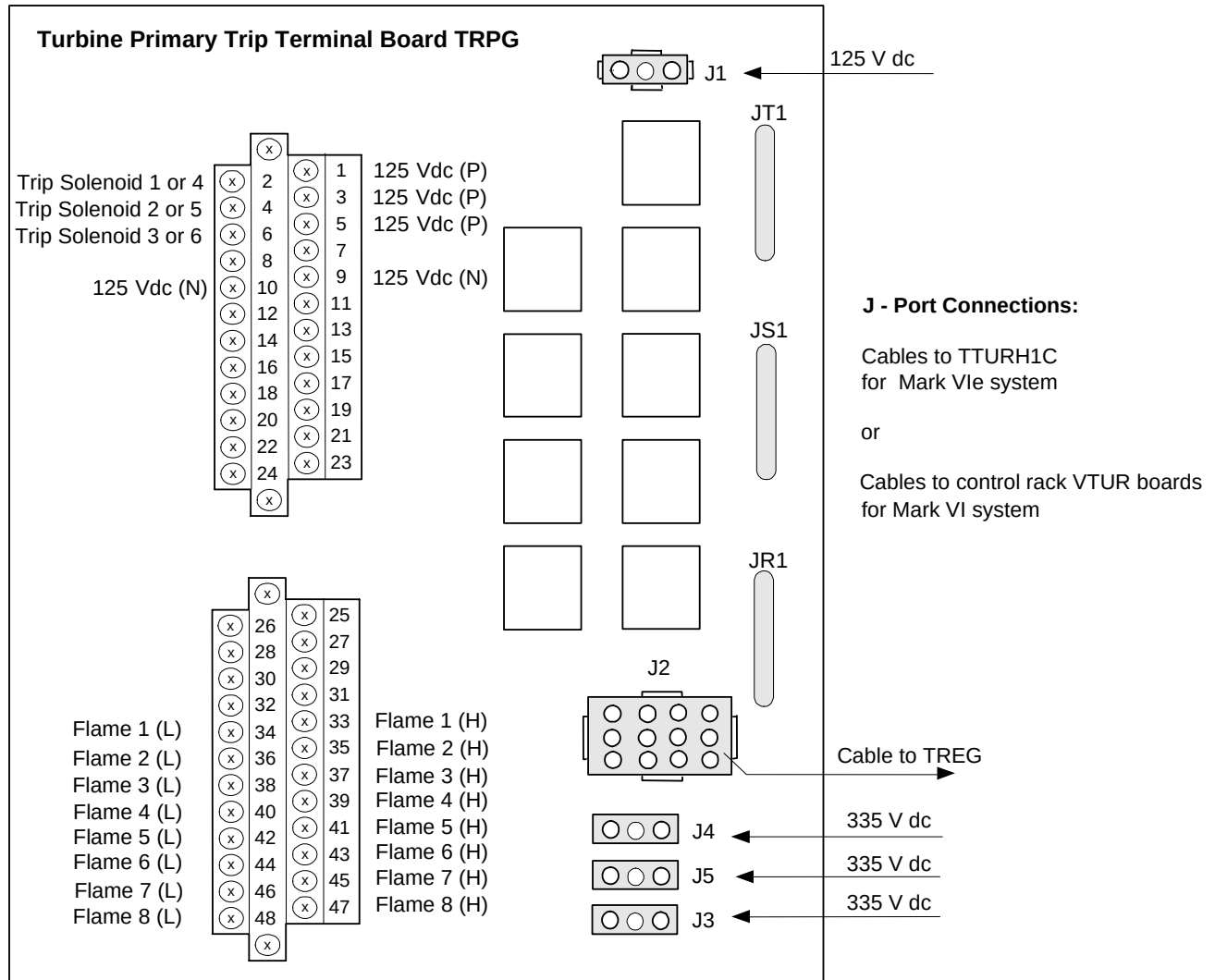


TRPG Terminal Board and Cabling

## Installation

Connect the wires for the three trip solenoids directly to the first I/O terminal block. Connect the wires for the flame detectors (if used) to the second terminal block. Connect the power for the flame detectors to the J3, J4, and J5 plug.

Connect the 125 V dc power for the trip solenoids to the J1 plug. Transfer power to the TREG board using the J2 plug.



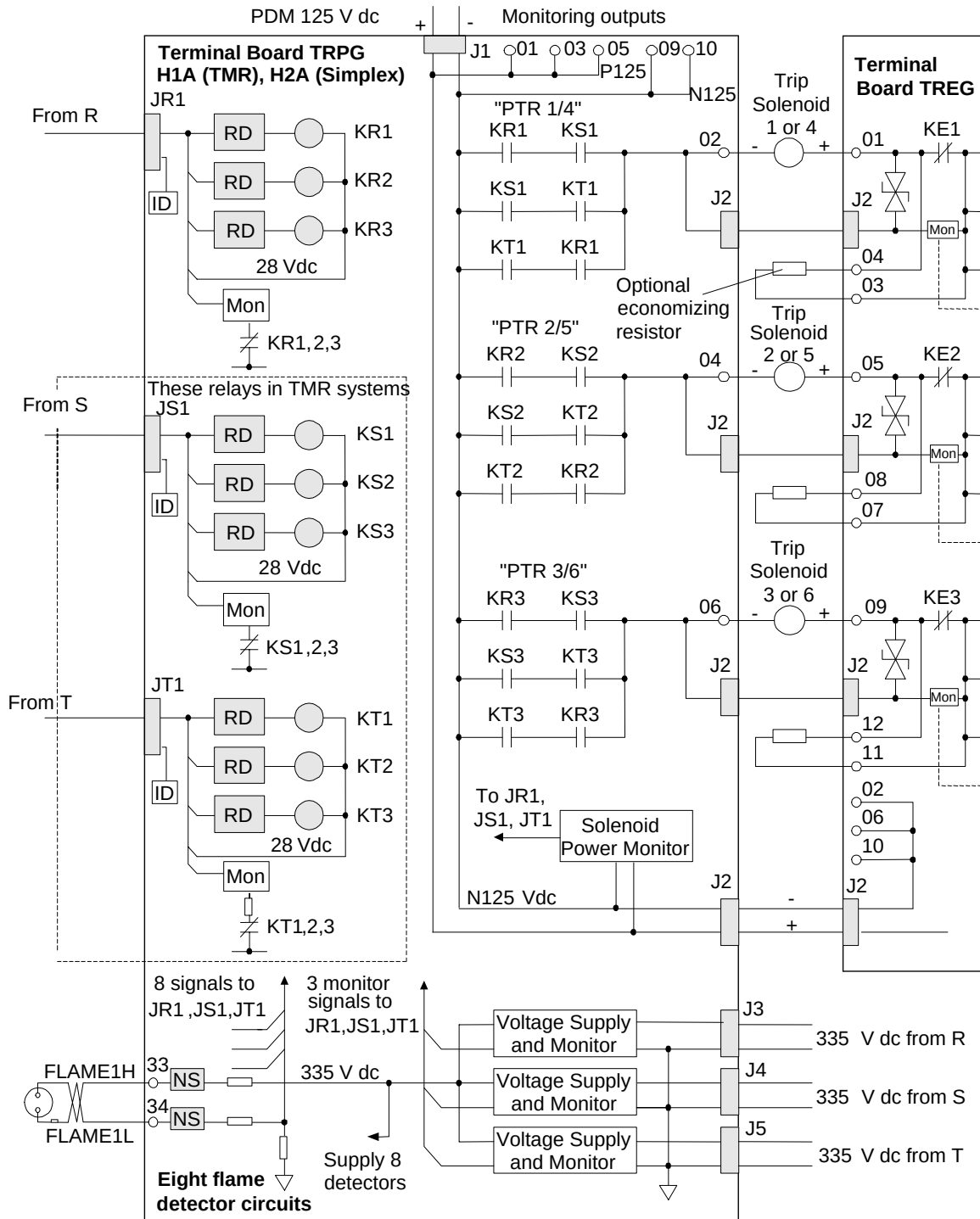
Up to two #12 AWG wires per point with 300 V insulation

Terminal blocks can be unplugged from terminal board for maintenance

*TRPG Terminal Board Wiring*

## Operation

The I/O pack/board provides the primary trip function by controlling the relays on TRPG, which trip the main protection solenoids. In TMR applications, the three inputs are voted in hardware using a relay ladder logic two-out-of-three voting circuit. The I/O pack/board monitors the current flow in its relay driver control line to determine its energize or de-energize vote/status of the relay coil contact status. Supply voltages are monitored for diagnostic purposes. A normally closed contact from each relay on TRPG is monitored by the diagnostics to determine its proper operation.



TRPG and Connections to Controller and Trip Solenoids

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**Note** A metal oxide varister (MOV) and a current limiting resistor are used in each ETD circuit

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The primary overspeed trip comes from the controller and is passed to the I/O pack/board, and then to TRPG. TRPG works in conjunction with the TREG board, which is controlled by the emergency overspeed system. This TRPG/TREG combination can drive three ETDs.

### ***Flame Detectors***

The primary protection system monitors signals from eight Geiger-Mueller<sup>®</sup> flame detectors. With no flame present, the detector charges up to the supply voltage. The presence of flame causes the detector to charge to a level and then discharge through TRPG. As the flame intensity increases, the discharge frequency increases. When the detector discharges, the I/O pack/board and TRPG convert the discharged energy into a voltage pulse. The pulse rate varies from 0 to 1,000 pulses/sec. These voltage pulses are fanned out to all three modules. Voltage pulses above 2.5 volts generate a logic high, and the pulse rate over a 40 ms time period is measured in a counter.

### ***Specifications***

| <b>Item</b>                           | <b>Specification</b>                                                                              |
|---------------------------------------|---------------------------------------------------------------------------------------------------|
| Trip solenoids                        | 3 solenoids per TRPG                                                                              |
| Solenoid rated voltage/current        | 125 V dc standard with up to 1 A draw<br>24 V dc is alternate with up to 1 A draw (H1B, H2B, H3B) |
| Solenoid response time                | L/R time constant is 0.1 sec                                                                      |
| Current suppression                   | MOV on TREG                                                                                       |
| Current economizer                    | Terminals for optional 10 $\Omega$ , 70 W economizing resistor on TREG                            |
| Control relay coil voltage supply     | Relays are supplied with 28 V dc from JR1, JS1, and JT1                                           |
| Flame detectors                       | 8 detectors per TRPG                                                                              |
| Flame detector supply voltage/current | 335 V dc with 0.5 mA per detector                                                                 |

### ***Diagnostics***

The I/O board runs the TRPG diagnostics. These include feedback from the trip solenoid relay driver and contact, solenoid power bus, and the flame detector excitation voltage too low or too high. A diagnostic alarm is created if any one of the signals go unhealthy (beyond limits). Connectors JR1, JS1, and JT1 on the terminal board have their own ID device, which is interrogated by the I/O board, and if a mismatch is encountered, a hardware incompatibility fault is created. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

### ***Configuration***

There are no jumpers or hardware settings on the board.

---

# ***TRPA Turbine Primary Trip***

## ***Functional Description***

The Aeroderivative Turbine Primary Trip (TRPAH1A) terminal board works with the PTUR turbine I/O packs or with the TTUR terminal board as part of the Mark\* VIe system. The inputs and outputs are as follows:

- Twelve passive pulse rate devices (four per R/S/T section) sensing a toothed wheel to measure the turbine speed. Or, six active pulse rate inputs (two per TMR section)
- Two 24 V dc (H1) or 125 V dc (H2) TMR voted output contacts to the main breaker coil for trip coil.
- Four 24-125 V dc voltage detection circuits for monitoring trip string.
- One 24-125 V dc 'Fail-safe' ESTOP input for removing power from trip relays.

For TMR systems, signals fan out to the PR3, PS3, PT3, JR4, JS4, and JT4 connectors.

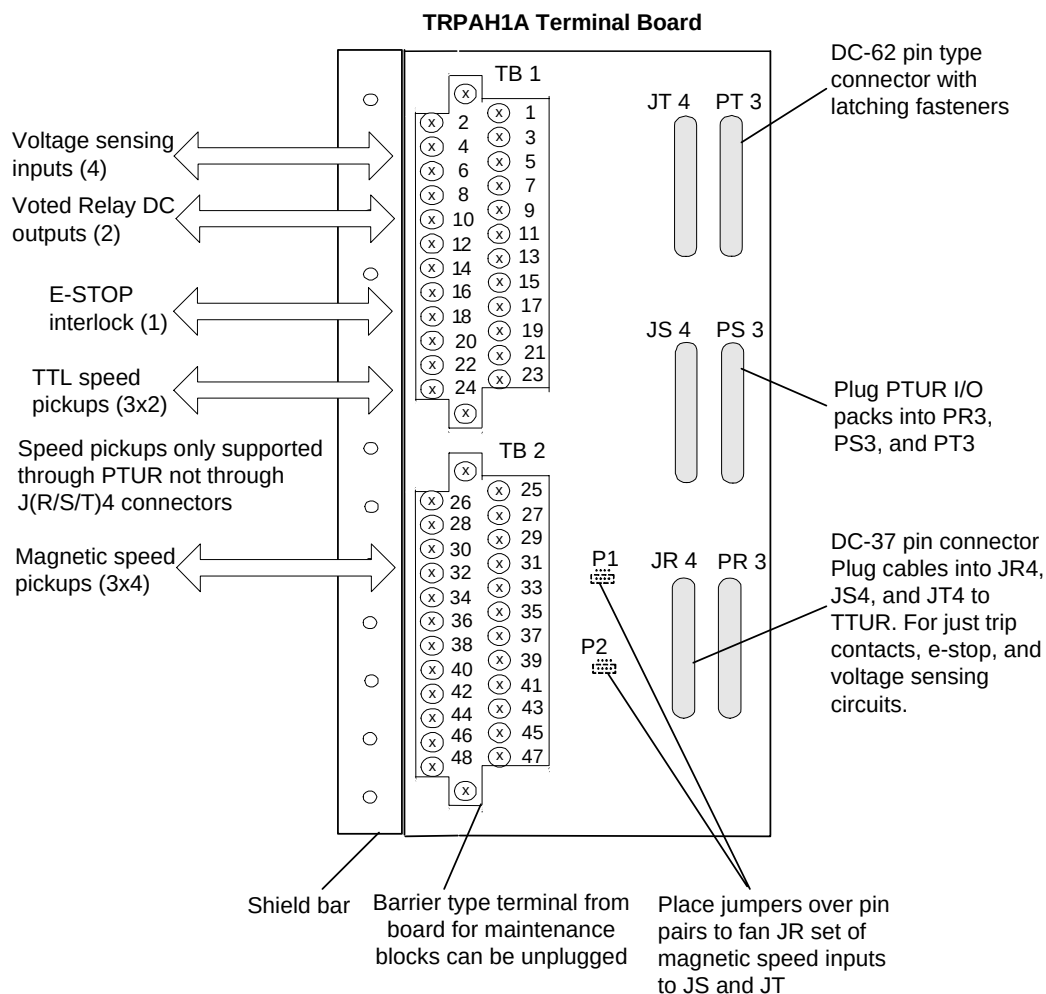
## ***Mark VI Systems***

TRPAH1A cannot be used with the Mark VI system.

## ***Mark VIe Systems***

TRPAH1A supports the Mark VIe system and accommodates PTUR I/O packs.





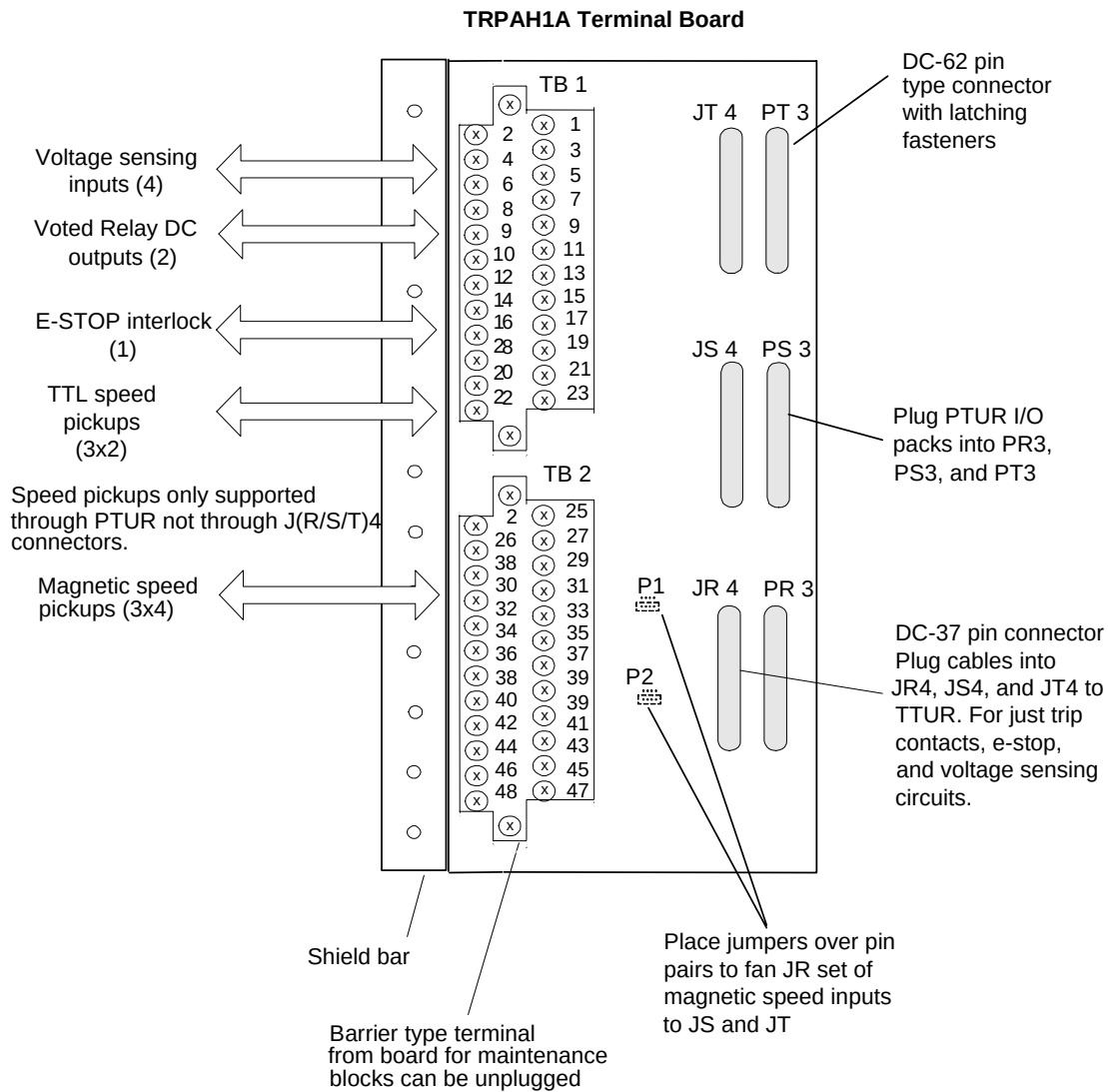
*TRPAH1A Turbine Terminal Board*

## Installation

TTL pulse rate pick ups, voltage detection, E-STOP, and the breaker relay are wired to the I/O terminal blocks TB1. Passive pulse rate pick-ups are wired to TB2. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left of each terminal block.

The TRPA must be configured for the desired speed input connections using the following table. Jumpers JP1 and JP2 select fanning of the R section pulse rate pickups to the S and T PTURs.

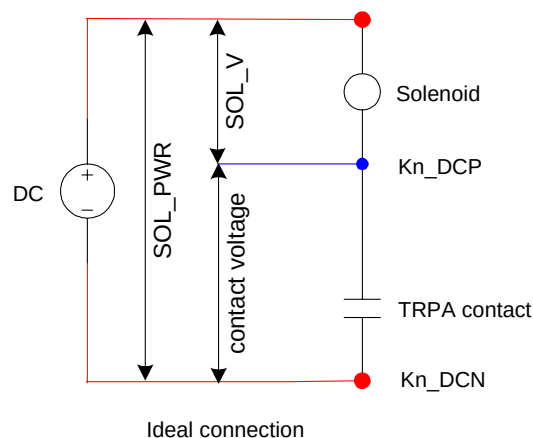
| Speed Input Connections                                                                              | Function                                                              | Jumper                                        |
|------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------|
| Wire to all 12 pulse inputs:<br>PR1_R – PR4_T                                                        | Each set of (4) pulse inputs goes to its own dedicated PTUR I/O pack. | Cannot use jumper:<br>Place in STORE position |
| Wire to TTL pulse inputs:<br>TTL1_R – TTL2_T                                                         | Each set of (2) pulse inputs goes to its own dedicated PTUR I/O pack. | Cannot use jumper:<br>Place in STORE position |
| Wire to bottom 4 pulse inputs only:<br>PR1_R – PR4_R<br>NO wiring to TTL1_R-TTL2_T or<br>PR1_S-PR4_T | The same set of signals are fanned to all the PTUR I/O packs.         | Use jumper:<br>Place over pin pairs           |
| Wire to bottom 2 pulse inputs:<br>TTL1_R – TTL2-R                                                    | Cannot fan the TTL signals. Only the R PTUR will receive data.        | Cannot use jumper:<br>Place in STORE position |



*TRPA Terminal Board Wiring*

### **Contact outputs**

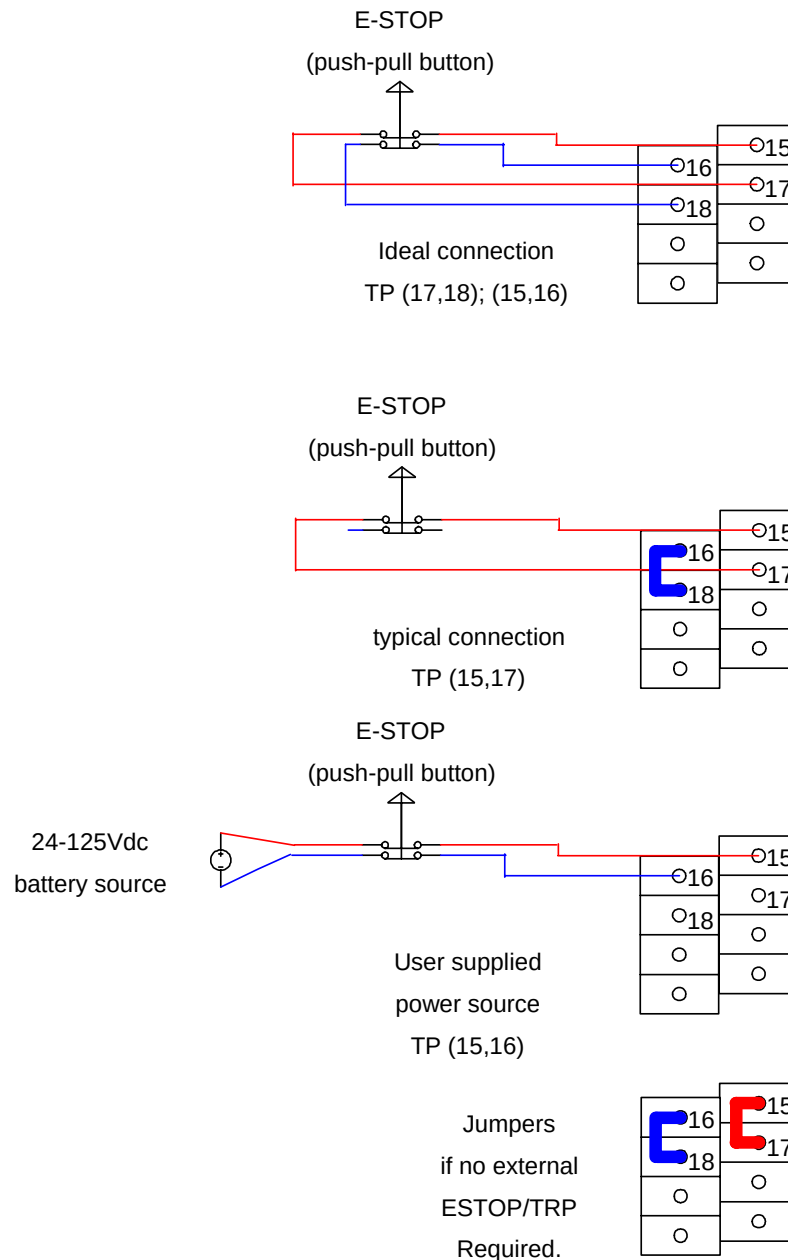
- The contact outputs are polarity sensitive. Wire the circuit carefully to avoid damaging the relays.
- There is no contact or solenoid suppression, user must add external solenoid suppression to avoid damaging the relays and their contacts.



*Connection to TRPA contact output*

## E-STOP/TRP input

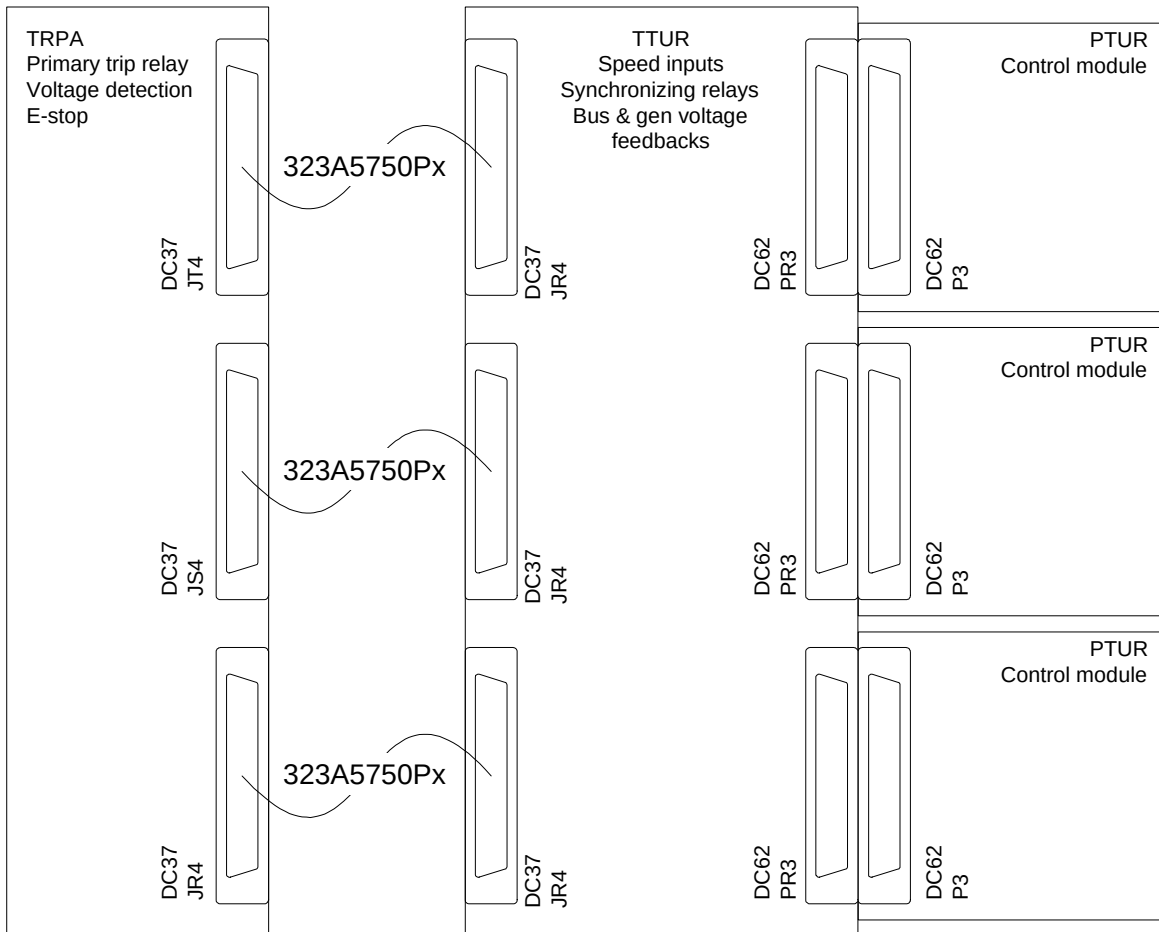
- The TRP inputs must be powered for the relays to operate. If the user does not need or use an E-STOP, then jumper the local TRP power source (P24O/R) to the respective TRP inputs at the terminal board.
- The E-STOP must be connected to a CLEAN dc source – battery or filtered (< 5% ripple) rectified ac.
- There must be a minimum of 18 V dc at the TRP inputs for proper operation. The current required was kept low to minimize drop on long cable runs.
- As the TRP is very fast < 5 ms and the output relay contacts are also fast (< 15 ms), best wiring practices should be utilized to avoid misoperation. Use twisted-pair cable when possible and avoid running with ac wiring and so on.



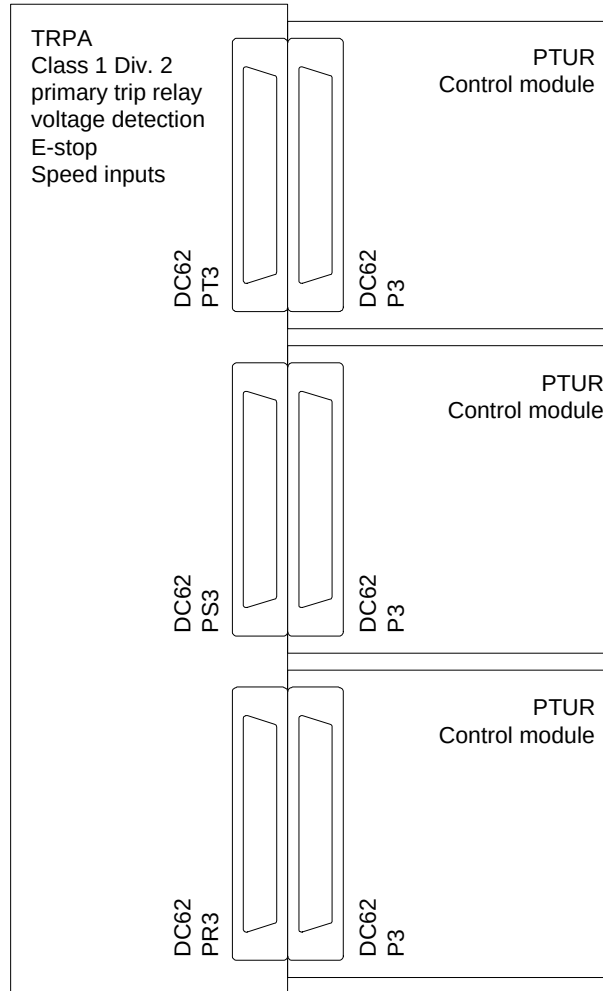
Typical E-STOP connection options

## Operation

**System Design:** The TRPA board is designed for application in two different ways. When a TTUR terminal board is used to hold three PTUR I/O packs the TRPA terminal board may be connected using three cables with DC-37 pin connectors on each end. In this mode of operation the TRPA provides two contact voted trip relay outputs, ESTOP, and four voltage sensors. TTUR provides the normal set of features described for that board. The TRPA speed inputs are not active and should not be connected with this board arrangement.



The TRPA board may also be used with three PTUR I/O packs mounted directly on TRPA. In this mode of operation the speed inputs to TRPA become active paths into the PTUR allowing for a single terminal board primary trip solution.



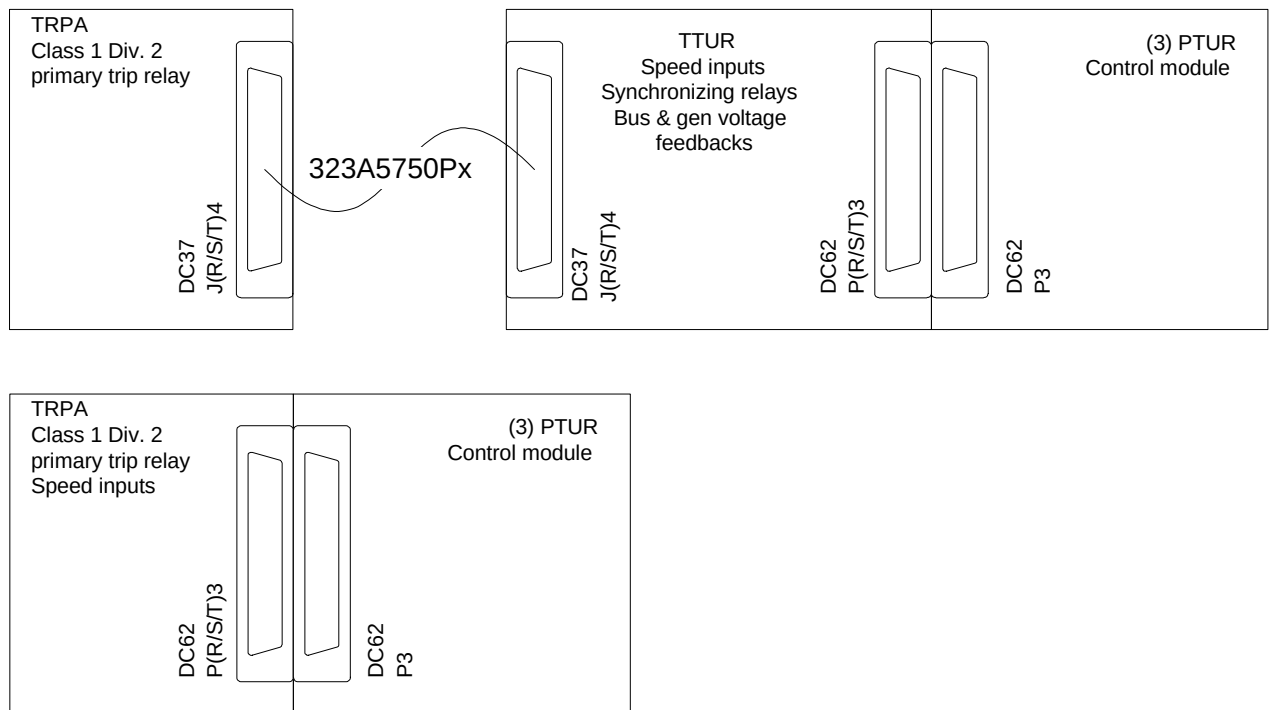
TRPAH1A and TRPAH2A will only function correctly with three PTUR I/O packs, simplex operation is not possible.

**Speed Inputs:** When used with PTUR I/O packs mounted directly on the TRPA the speed inputs provide two options. Each PTUR I/O pack may receive a dedicated set of four speed inputs from their respective TRPA terminal points as is done on TTUR. As an option, jumpers P1 and P2 may be placed on the TRPA to take the first four speed inputs (those for the R pack) and fan them to the S and T packs. When this is selected the terminal board points for S and T speed input become no-connects and should not be used.

**EStop:** The TRPA includes an EStop function. This consists of an optically isolated input circuit designed for a dc input in the range of 24 V to 125 V nominal. When energized the circuit enables coil drive power in the R, S, and T relay circuits through independent hardware paths. The response time of this circuit of less than five milliseconds plus the response time of the trip relays of less than one millisecond yields very fast EStop response. EStop is monitored by PTUR, but the action to remove trip relay coil power is entirely in the hardware of TRPA.

**Voltage Monitors:** The trip relays on TRPA may be freely located anywhere in a trip string. Because the trip string circuit is not fixed, there are four general-purpose isolated voltage sensor inputs on TRPA. These may be used to monitor any points in the trip system and drive the voltage status into the system controller where action may be taken. Typical use of these inputs may be to sense the power supply voltage for the two trip strings and to sense the solenoid voltage of the device being driven by the relays. This set of applications is used in the wording of the board symbol, but the sensors may be freely applied to best serve the application.

**Trip Relays:** The trip relays are made using sets of six individual form A devices arranged in a voting pattern. Any two controllers that vote to close will establish a conduction path through the set. Because detection of a shorted relay is important to preserve tripping reliability there is a sensing circuit applied to each of the sets of relays. When the relays are commanded to open and voltage is present across the relays the circuit will detect if one or more relays are shorted. This signal goes to the PTUR I/O pack to create an alarm. The TRPA sensing circuit uses the relay commands from all three packs to avoid a false indication in the event that one PTUR I/O pack votes to close the relay while the other two PTUR I/O packs vote to open.



TRPA and PTUR I/O Pack, TMR System

### TRPA - Primary Tip Board

**TRPAH\_A**

**Pulse Rate Inputs**

Four of above circuits to T, except for TTL, see Table.

Four of above circuits to S, except for TTL, see Table.

Four of above circuits to R, except for TTL, see Table.

Relay V Monitor

Relay V Monitor

Monitors go to TTUR and PTUR RST connectors

**Termination Board Speed Input Screw Assignments:**

| Circuit | MnnH | TB1/2 | MnnL | TB1/2 | TTL    | TB3   |
|---------|------|-------|------|-------|--------|-------|
| 1 T     | M1TH | 25    | M1TL | 26    | TTL1_T | 01    |
| 2 T     | M2TH | 27    | M2TL | 28    | TTL2_T | 02    |
| 3 T     | M3TH | 29    | M3TL | 30    | -----  | ----- |
| 4 T     | M4TH | 31    | M4TL | 32    | -----  | ----- |
| 1 S     | M1SH | 33    | M1SL | 34    | TTL1_S | 03    |
| 2 S     | M2SH | 35    | M2SL | 36    | TTL2_S | 04    |
| 3 S     | M3SH | 37    | M3SL | 38    | -----  | ----- |
| 4 S     | M4SH | 39    | M4SL | 40    | -----  | ----- |
| 1 R     | M1RH | 41    | M1RL | 42    | TTL1_R | 05    |
| 2 R     | M2RH | 43    | M2RL | 44    | TTL2_R | 06    |
| 3 R     | M3RH | 45    | M3RL | 46    | -----  | ----- |
| 4 R     | M4RH | 47    | M4RL | 48    | -----  | ----- |

**Note** The above figure is simplified with many circuit paths omitted for clarity.

## ***Specifications***

| <b>Item</b>                   | <b>Specification</b>                                                                                                                                                                                                                             |
|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs              | 3x4 passive (magnetic) speed pickups or 3x2 active (TTL) speed pickups.<br>4 voltage detection circuits<br>1 ESTOP/TRP input                                                                                                                     |
| Number of outputs             | 2 trip contacts:<br>1 ESTOP/TRP power source.                                                                                                                                                                                                    |
| Contact ratings               | NEMA class F. Minimum operations: 100,000                                                                                                                                                                                                        |
| IS200TRPAH1A                  | Voltage: 28 V dc max<br>Max. Current 10 A dc @40°C (140 °F) maximum<br>de-rate current linearly to 7 A dc @ 65°C (149 °F) maximum<br>Leakage: 2.21 mA max                                                                                        |
| IS200TRPAH1A                  | Voltage: 145 V dc max<br>Max. Current : 3 A dc@40°C (140 °F) maximum<br>de-rate current linearly to 2 A dc @65°C (149 °F) maximum<br>Leakage: 3.31 mA max                                                                                        |
| Voltage detection inputs      | Min/max input voltage rating: 16/150 V dc max pk<br>Current Loading (Max leakage): 3 mA<br>Detection delay (max): 60 ms<br>Voltage isolation: Optically isolated.: 2500 V rms isolation, for one min<br>Surge/Spike rating: 1000 V pk for 8.3 ms |
| ESTOP/TRP voltage source      | 24 V dc no-load, 0.3 to 1K source impedance                                                                                                                                                                                                      |
| ESTOP/TRP detection           | Input Voltage: 24-125 V dc ±10% (18/150 V pk Min/Max)<br>Loading (max): 12 mA (5 typical)<br>Delay (max): 5 ms (<1 typical)                                                                                                                      |
| MPU pulse rate range          | 2 Hz to 20 kHz                                                                                                                                                                                                                                   |
| MPU pulse rate accuracy       | 0.05% of reading                                                                                                                                                                                                                                 |
| MPU input circuit sensitivity | 27 mV pk (detects 2 rpm speed)                                                                                                                                                                                                                   |
| Physical                      |                                                                                                                                                                                                                                                  |
| Size                          | 33.0 cm high x 17.8 cm , wide (13 in x 7 in)                                                                                                                                                                                                     |
| Technology                    | Surface mount                                                                                                                                                                                                                                    |
| Temperature                   | -30 to 65°C (-22 °F to 149 °F)                                                                                                                                                                                                                   |



## ***Diagnostics***

Diagnostic tests are made on the terminal board:

- Feedback from the shorted contact detector checked; if there is a problem with the control signal an alarm should be created.
- Feedback from the ESTOP/TRP input is checked; if there is a problem with the signal a fault should be created.
- Feedback from speed pickup fanning jumpers is checked; if there is a mismatch between intention and actual position, an alarm should be created.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm DIAG\_PTUR occurs. The diagnostic signals can be individually latched and then reset with the RESET\_DIA signal if they go healthy.
- Terminal board connectors have their own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by PTUR and a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

Jumpers JP1 and JP2 select the fanning of the 4 R section passive speed pickups to the S and T section PTURs. Place the jumper over the pin pairs to fan the 4 R speed input to the other two TMR sections.

---

# ***TRPL Turbine Primary Trip***

## ***Functional Description***

The Large Steam Turbine Primary Trip (TRPL) terminal board is used for the primary overspeed protection of large steam turbines. TRPL is controlled by the turbine Primary Turbine Protection controller (VTUR or PTUR), and contains nine magnetic relays in three voting circuits to interface with three trip solenoids (ETDs). TRPL works in conjunction with the TREL terminal board to form the primary and emergency sides of the interface to the ETDs. These two terminal boards are used in a similar way as TRPG and TREG are used on gas turbine applications.

Up to three trip solenoids can be connected between the TREL and TRPL terminal boards. TREL provides the positive side of the 125 V dc to the solenoids and TRPL provides the negative side. In addition, two manual emergency stop functions can be connected.

### **Mark VI Systems**

In the Mark\* VI system, the TRPL works with the VTUR board and only supports TMR systems applications. Cables with molded plugs connect TRPL to the VME rack where the VTUR board is located.

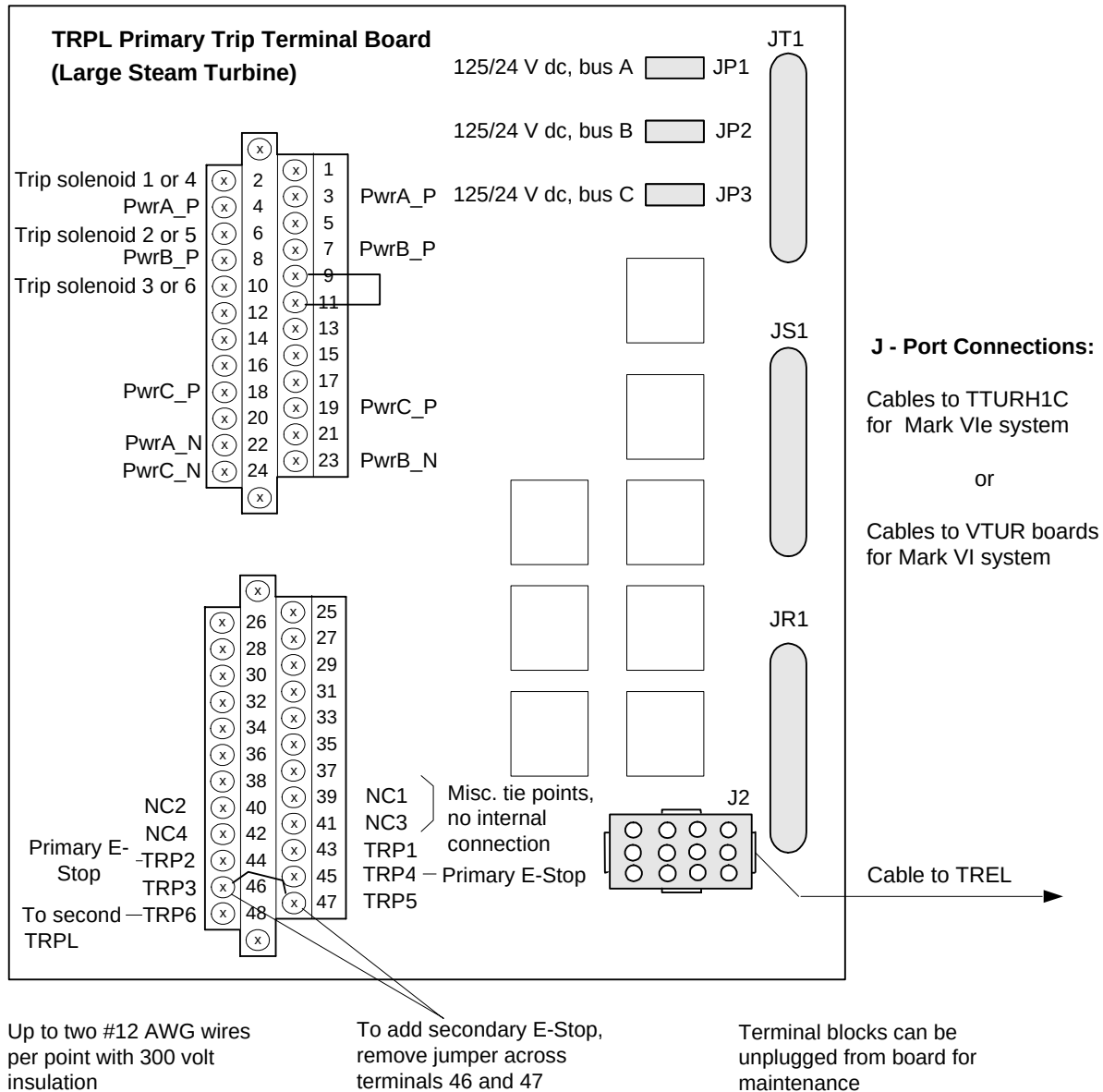
### **Mark VIe Systems**

In the Mark VIe system, the TRPL is controlled by the PTUR I/O packs on TTURH1C and only supports TMR applications. The I/O packs plug into the D-type connectors on TTURH1C, which is cabled to TRPL.

## Installation

Connect the wires for the three trip solenoids directly to the first I/O terminal block. Connect the wires for the primary emergency stop and optional secondary emergency stop to the second terminal block. Connect the trip solenoid power to plugs JP1, JP2, and JP3. The wiring connections are shown in the following figure.

Install a jumper across terminals 9 and 11 for the PTR3 trip. If a second emergency stop is required, remove the jumper from terminals 46 and 47 and connect the wires here.



TRPL Terminal Board Wiring

## Operation

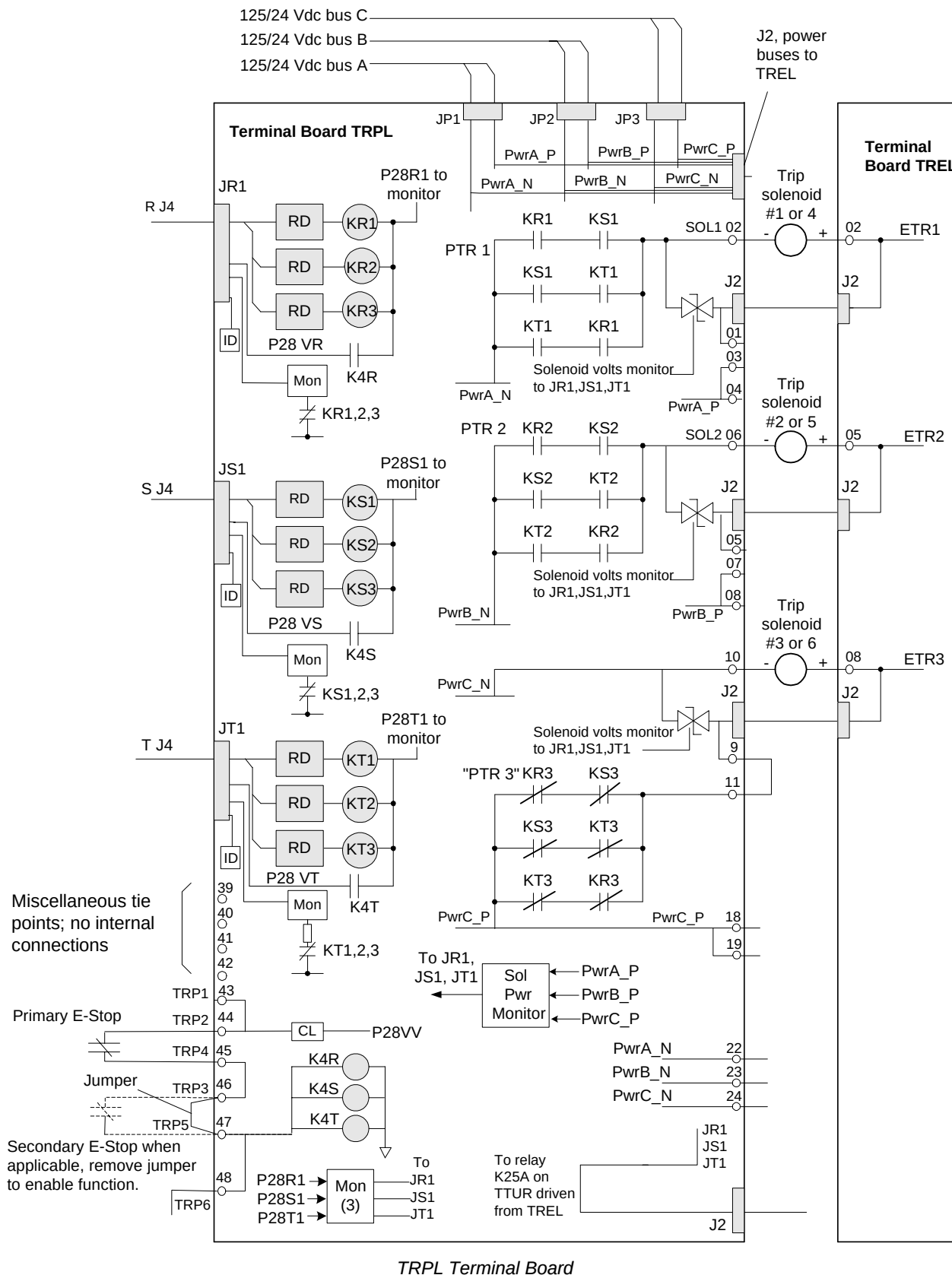
TRPL is used for TMR applications only. Three separate power buses, PwrA, PwrB, and PwrC for solenoid power, are brought in through connectors JP1, JP2, and JP3, and then distributed to TREL through connector J2.

The power buses have a nominal voltage of 125 V dc (70 to 145 V dc) or 24 V dc (18 to 32 V dc). The board includes power bus monitoring (three buses). The maximum current per bus is 3 A.

Each of the three trip solenoids is controlled by three relays using 2/3 contact voting. The relay output rating (for 100,000 operations) is as follows:

- At 24 V dc, 3 A, L/R = 100 ms, with suppression
- At 125 V dc, 1.0 A, L/R = 100 ms, with suppression

The trip circuits include solenoid suppression, associated solenoid voltage monitoring, and trip relay contact monitoring. In the TRPL, the hardwired trip (E-STOP) and associated monitoring provides approximately 6.6 V dc to the I/O board when the K4 relays are picked up.



## Specifications

| Item                              | Specification                                                                     |
|-----------------------------------|-----------------------------------------------------------------------------------|
| Trip solenoids                    | 3 solenoids per TRPx                                                              |
| Solenoid rated voltage/current    | 125 V dc standard with up to 1 A draw<br>24 V dc is alternate with up to 3 A draw |
| Solenoid response time            | L/R time constant is 0.1 sec with suppression                                     |
| Current suppression               | MOVs                                                                              |
| Control relay coil voltage supply | Relays are supplied with 28 V dc from JR1, JS1, and JT1                           |
| Primary Emergency Stop, manual    | One with optional secondary E-stop                                                |

## Diagnostics

**Note** The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

The I/O controller runs the TRPx diagnostics. These include feedback from the trip solenoid relay driver and contact, solenoid voltage, and solenoid power bus. A diagnostic alarm is created if any one of the signals goes unhealthy (beyond limits).

The Jx1 connectors on the terminal board have their own ID device, which is interrogated by the I/O board, and if a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

There are no switches or hardware settings on the terminal board. Terminals 9 and 11 must use a jumper to include the PTR 3 trip. Terminals 46 and 47 must use a jumper if only one manual emergency stop is required.

---

# **TRPS Turbine Primary Trip**

## **Functional Description**

The Small Steam Turbine Primary Trip (TRPS) terminal board is used for the primary overspeed protection of small and medium size steam turbines. TRPS is controlled by the Primary Turbine Protection controller (VTUR or PTUR), and contains three magnetic relays to interface with three trip solenoids (ETDs). TRPS works in conjunction with the TRES terminal board to form the primary and emergency sides of the interface to the ETDs. These two terminal boards are used in a similar way as TRPG and TREG are used on gas turbine applications, except with the following differences:

- Two-out-of-three voting is done in the relay drivers and not using relay contacts as with TRPG and TRPL.
- In a simplex application, the voting is bypassed and the relay drivers are controlled by a single signal from JA1.
- There are no economizing relays.
- There are no flame detector inputs.

Up to three trip solenoids can be connected between the TRES and TRPS terminal boards. TRES provides the positive side of the 125 V dc to the solenoids and TRPS provides the negative side. In addition, two manual emergency stop functions can be connected.

## **Mark VI Systems**

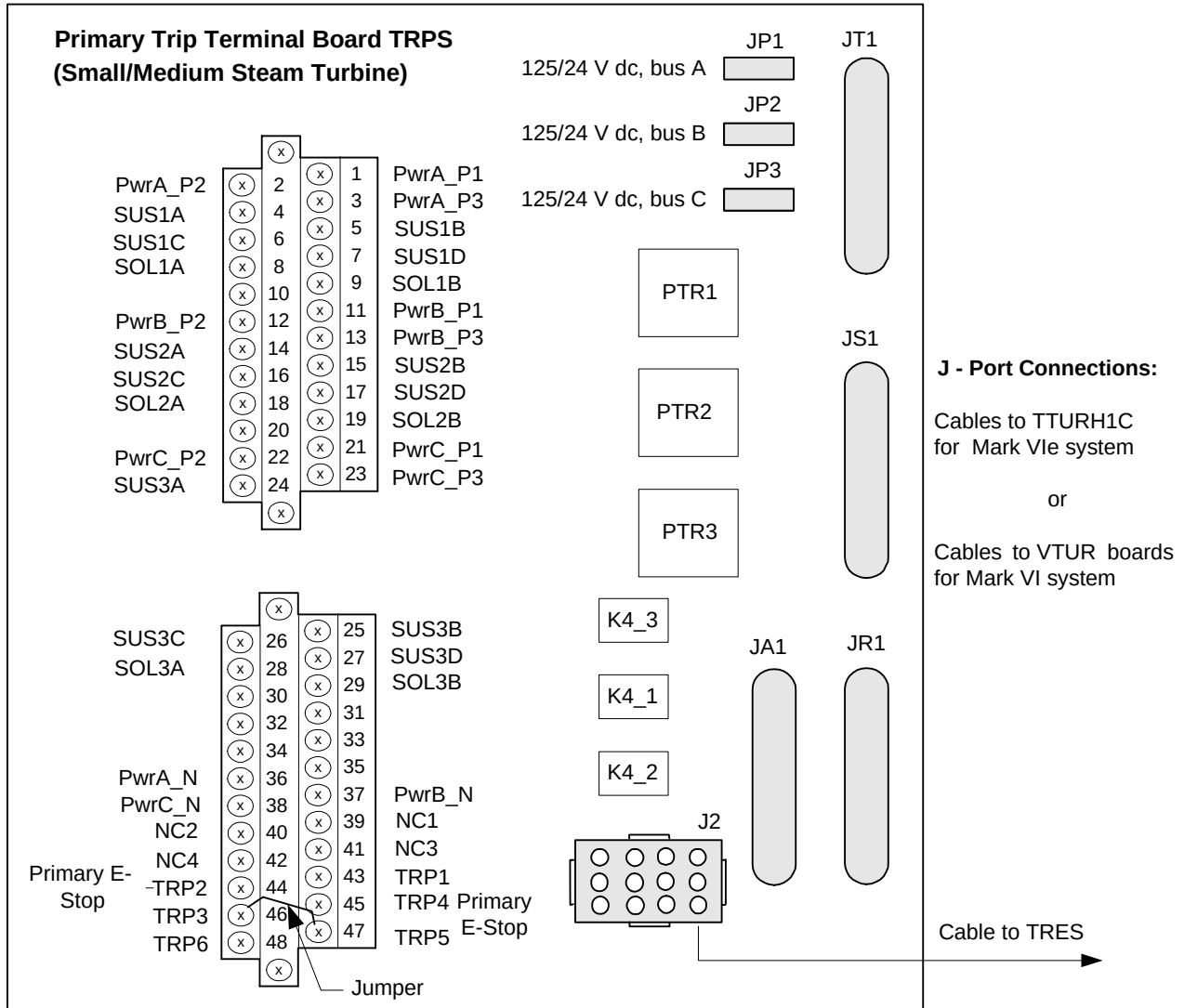
In the Mark\* VI system, the TRPS works with the VTUR board and supports simplex and TMR applications. Cables with molded plugs connect TRPS to the VME rack where the VTUR board is located.

## **Mark VIe Systems**

In the Mark VIe system, TRPS is controlled by the PTUR I/O packs on TTURH1C and supports simplex and TMR applications. The I/O packs plug into the D-type connectors on TTURH1C, which is cabled to TRPS.

## Installation

Connect the wires for the three trip solenoids to the first I/O terminal block. Connect the wires for the primary emergency stop and optional secondary emergency stop to the second terminal block. Connect the trip solenoid power to plugs JP1, JP2, and JP3. If a second emergency stop is required, remove the jumper from terminals 46 and 47, and connect the wires here. The wiring connections are shown in the following figure.



TRPS Terminal Board Wiring

## Operation

TRPS is used for TMR and simplex applications. Three separate power buses, PwrA, PwrB, and PwrC for solenoid power, are brought in through connectors JP1, JP2, and JP3, and then distributed to TRES through connector J2.

The power buses have a nominal voltage of 125 V dc (70 to 145 V dc) or 24 V dc (18 to 32 V dc). The board includes power bus monitoring (three buses). The maximum current per bus is 3 A.

Each of the three trip solenoids is controlled by a relay driver. The relay output rating (for 100,000 operations) is as follows:

- At 24 V dc, 3 A, L/R = 100 ms, with suppression
- At 125 V dc, 1.0 A, L/R = 100 ms, with suppression

The trip circuits include solenoid suppression, associated solenoid voltage monitoring, and trip relay contact monitoring. In the TRPS, the hardwired trip (E-Stop) and associated monitoring provides approximately 6.6 V dc to the I/O board when the K4 relays are picked up.





## Specifications

| Item                              | Specification                                                                     |
|-----------------------------------|-----------------------------------------------------------------------------------|
| Trip solenoids                    | 3 solenoids per TRPx                                                              |
| Solenoid rated voltage/current    | 125 V dc standard with up to 1 A draw<br>24 V dc is alternate with up to 3 A draw |
| Solenoid response time            | L/R time constant is 0.1 sec with suppression                                     |
| Current suppression               | MOVs                                                                              |
| Control relay coil voltage supply | Relays are supplied with 28 V dc from JR1, JS1, and JT1                           |
| Primary Emergency Stop, manual    | One with optional secondary E-stop                                                |

## Diagnostics

**Note** The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

The I/O controller runs the TRPx diagnostics. These include feedback from the trip solenoid relay driver and contact, solenoid voltage, and solenoid power bus. A diagnostic alarm is created if any one of the signals goes unhealthy (beyond limits).

The Jx1 connectors on the terminal board have their own ID device, which is interrogated by the I/O board, and if a mismatch is encountered, a hardware incompatibility fault is created.

## Configuration

There are no switches or hardware settings on the terminal board. Terminals 46 and 47 must use a jumper if only one manual emergency stop is required; remove jumper if secondary E-Stop is used.

---

# ***STUR Simplex Primary Turbine Protection Input***

## ***Functional Description***

The Simplex Primary Turbine Protection Input (STUR) terminal board is a simplex S-type terminal board version of the turbine terminal board (TTUR). It provides a connection for the turbine specific primary trip (PTUR), speed and synchronizing inputs, and trip relay outputs or a cable to drive a primary trip board.

STUR is used for the following:

- Mechanical drives requiring overspeed protection but no synchronizing function.
- Generator drive systems requiring overspeed and primary synchronization.
- Other applications requiring the four pulse input circuits of PTUR.

This terminal board has the same physical size, customer terminal locations, and I/O pack mounting as other S-type terminal boards. There will be no components higher than an attached PTUR I/O pack permitting double stacking of terminal boards.

There are four groups:

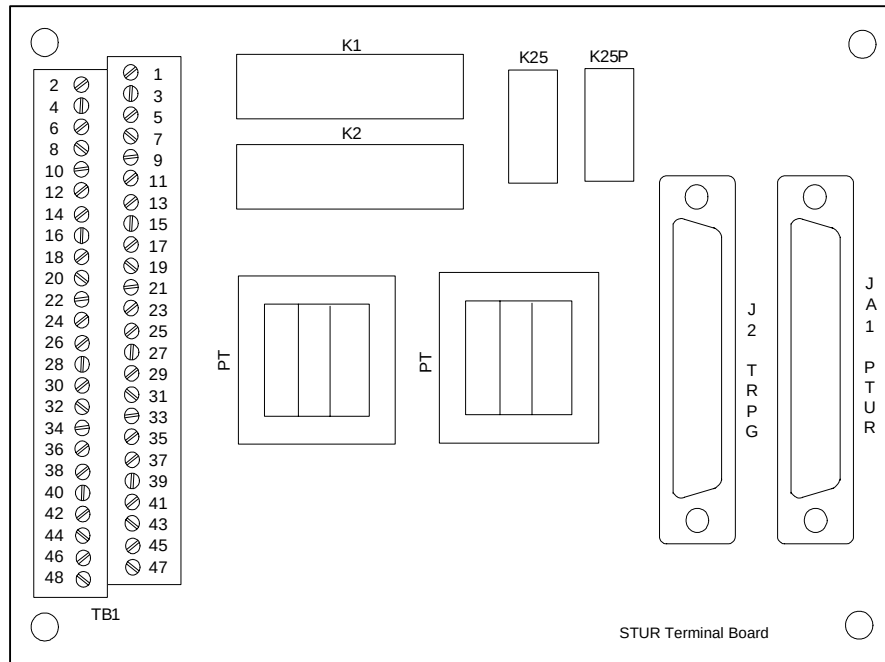
- IS200STURH1 omits synchronizing hardware and includes trip relays.
- IS200STURH2 includes synchronizing hardware and trip relays.
- IS200STURH3 omits synchronizing hardware and includes a DC-37 pin connector for a cable leading to a trip terminal board.
- IS200STURH4 includes synchronizing hardware and includes a DC-37 pin connector for a cable leading to a trip terminal board.

STUR provides the following major functions:

- Provides a DC-62 pin connector for mounting a single PTUR I/O pack.
- Accepts up to four speed input signals.
- A 48 terminal Euro-style box connector for customer connection points is supplied on the board.
- Provides two trip solenoid outputs, K1 and K2, with each composed of a safety relay (H1, H2).
- Provides a DC-37 pin connector for connecting a TPRG, TPRL, TPRS, or TPRA primary trip relay (H3, H4).
- Accepts two PT inputs supporting primary synchronization (H2, H4). They accept generator voltage and bus voltage signals taken from potential transformers.
- Provides two relay outputs supporting primary synchronization (H2, H4). Two relays, K25 and K25P, have to close to provide 125 V dc power needed to close the main breaker 52G.

## Installation

STUR and a plastic insulator mount on a sheet metal carrier. The carrier is then mounted to a cabinet by screws.



STUR Terminal Board Layout

### Customer Terminal Assignments

| Terminal | Signal Name  |              | Description |                                        |
|----------|--------------|--------------|-------------|----------------------------------------|
|          | STURH1A      | STURH2A      | STURH3A     | STURH4A                                |
| 1        | K1_NO1_In    | K1_NO1_In    |             | Parallel connection to terminal 2.     |
| 2        | K1_NO1_In    | K1_NO1_In    |             | Relay K1 Normally Open contact #1      |
| 3        | K1_Centertap | K1_Centertap |             | Relay K1 Common                        |
| 4        | K1_NC_Out    | K1_NC_Out    |             | Relay K1 Normally Closed               |
| 5        | K1_NO2_In    | K1_NO2_In    |             | Relay K1 Normally Open Contact #2 in   |
| 6        | K1_NO2_Out   | K1_NO2_Out   |             | Relay K1 Normally Open Contact #2 ret. |
| 7        | K1_NO2_Out   | K1_NO2_Out   |             | Parallel connection to terminal 6      |
| 8        | K2_NO1_In    | K2_NO1_In    |             | Parallel connection to terminal 9      |
| 9        | K2_NO1_In    | K2_NO1_In    |             | Relay K2 Normally Open contact #1      |
| 10       | K2_Centertap | K2_Centertap |             | Relay K2 Common                        |
| 11       | K2_NC_Out    | K2_NC_Out    |             | Relay K2 Normally Closed               |
| 12       | K2_NO2_In    | K2_NO2_In    |             | Relay K2 Normally Open Contact #2 in   |
| 13       | K2_NO2_Out   | K2_NO2_Out   |             | Relay K2 Normally Open Contact #2 ret. |
| 14       | K2_NO2_Out   | K2_NO2_Out   |             | Parallel connection to terminal 13     |
| 15       | SOL1_In      | SOL1_In      |             | Solenoid 1 voltage sensor + input      |
| 16       | SOL1_Ret     | SOL1_Ret     |             | Solenoid 1 voltage sensor - input      |
| 17       | SOL2_In      | SOL2_In      |             | Solenoid 2 voltage sensor + input      |
| 18       | SOL2_Ret     | SOL2_Ret     |             | Solenoid 2 voltage sensor - input      |
| 19       |              |              |             | no connect                             |
| 20       |              |              |             | no connect                             |
| 21       |              | GENH         | GENH        | Generator PT input high                |

| Terminal | Signal Name |       |       | Description                                |
|----------|-------------|-------|-------|--------------------------------------------|
| 22       |             | GENL  | GENL  | Generator PT input low                     |
| 23       |             | BUSH  | BUSH  | Bus PT input high                          |
| 24       |             | BUSL  | BUSL  | Bus PT input low                           |
| 25       |             | B52GH | B52GH | Output (PGEN) to B52G feedback contact     |
| 26       |             | B52GL | B52GL | Return side of B52G feedback contact       |
| 27       |             | PGEN  | PGEN  | Positive breaker coil power input          |
| 28       |             | AUTO  | AUTO  | Output of K25P contact closure             |
| 29       |             | MAN   | MAN   | Output of K25 contact closure              |
| 30       |             | BKRH  | BKRH  | 52G Breaker Coil positive output.          |
| 31       |             | BKRH  | BKRH  | Parallel connection to terminal 30         |
| 32       |             | NGEN  | NGEN  | Negative breaker coil power connection     |
| 33       |             |       |       | no connect                                 |
| 34       |             |       |       | no connect                                 |
| 35       |             |       |       | no connect                                 |
| 36       |             |       |       | no connect                                 |
| 37       | TTL1        | TTL1  | TTL1  | Active speed pickup input 1                |
| 38       | PR1_H       | PR1_H | PR1_H | Passive speed pickup input 1               |
| 39       | PR1_L       | PR1_L | PR1_L | Speed pickup 1 return (active and passive) |
| 40       | TTL2        | TTL2  | TTL2  | Active speed pickup input 2                |
| 41       | PR2_H       | PR2_H | PR2_H | Passive speed pickup input 2               |
| 42       | PR2_L       | PR2_L | PR2_L | Speed pickup 2 return (active and passive) |
| 43       | TTL3        | TTL3  | TTL3  | Active speed pickup input 3                |
| 44       | PR3_H       | PR3_H | PR3_H | Passive speed pickup input 3               |
| 45       | PR3_L       | PR3_L | PR3_L | Speed pickup 3 return (active and passive) |
| 46       | TTL4        | TTL4  | TTL4  | Active speed pickup input 4                |
| 47       | PR4_H       | PR4_H | PR4_H | Passive speed pickup input 4               |
| 48       | PR4_L       | PR4_L | PR4_L | Speed pickup 4 return (active and passive) |

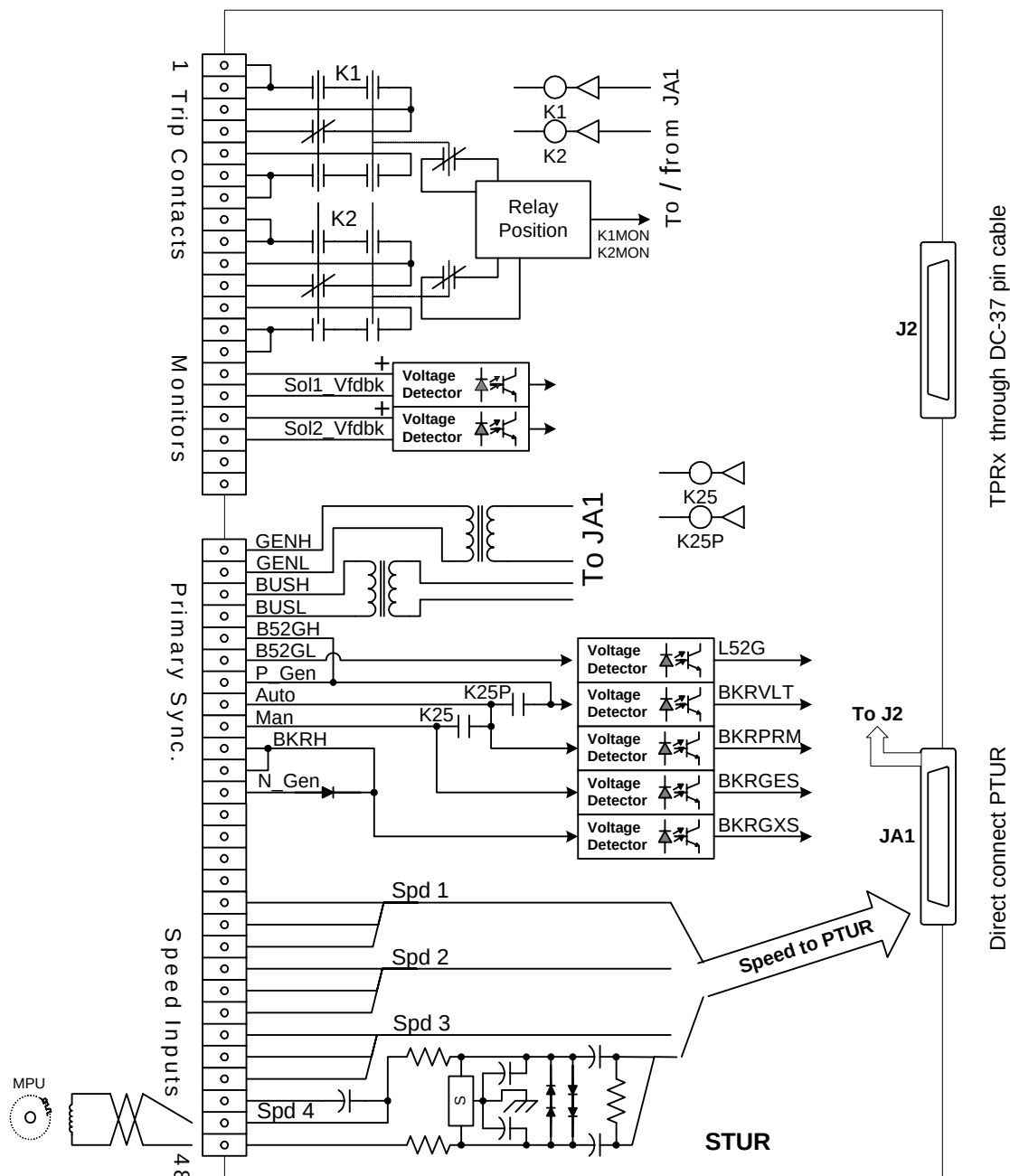
## Operation

### Board Groups

STUR is available in four distinct configurations. STUR is not available with fixed box terminals. It uses pluggable type terminals. Two groups offer on-board trip relays and two groups offer DC-37 pin connectors for using an external trip board. Components supporting generator applications will be omitted from two groups used for mechanical applications and added for groups used for generator applications.

#### STUR Board Variations

| Board Version | Generator Application | Trip Connections    | Application                                                                                       |
|---------------|-----------------------|---------------------|---------------------------------------------------------------------------------------------------|
| STURH1A       | No                    | Trip relays         | Mechanical drive turbines                                                                         |
| STURH2A       | Yes                   | Trip relays         | Generator drive turbines                                                                          |
| STURH3A       | No                    | DC-37 pin connector | Pulse inputs only, mechanical drive requiring features provided by a separate primary trip board. |
| STURH4A       | Yes                   | DC-37 pin connector | Generator drive turbines requiring features provided by a separate primary trip board.            |



STUR Schematic

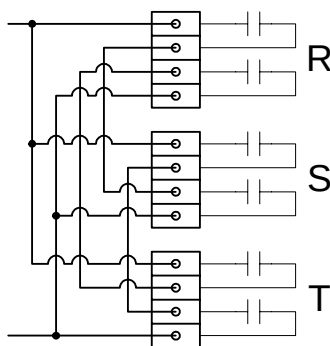
### Speed Input

STUR provides four speed input circuits that accept passive speed sensors or active speed sensors. When passive sensors are used the signal is applied between terminals PR#\_H and PR#\_L where # is 1 through 4. Sensitivity of the passive sensor input is such that the PTUR I/O pack is able to sense speeds as low as 2RPM. When active speed sensors are used the signal is applied between terminals TTL# and PR#\_L.

### Trip Relays

STUR version H1 and H2 provides two trip solenoid outputs, K1 and K2, with each composed of a safety relay that uses forcibly guided contacts. Relay position feedback is provided to PTUR using one of the contact pairs in the relay. Extra customer terminals are provided to allow connecting two or three STUR boards in a redundant tripping configuration.

If three STUR boards are to have their trip relays connected as a TMR voting set two sets of normally open contacts are required of each board. Two out of three voting is then provided when the following connection pattern is followed:



The above diagram displays four locations that require two wires on a single terminal as indicated by the wire junctions used. The STUR terminal board has been designed to provide dual terminals on these circuits to permit TMR wiring with no more than one wire on each terminal point. The four redundant terminals are listed in the connection chart in the *Installation* section.

### **Primary Synchronizing**

STURH2 and STURH4 used with PTUR provides support for synchronized closure of a 52G primary breaker. Two PT inputs are provided for Bus and Generator voltage on terminals 21 through 24. Breaker positive power at 24, 48, or 125 V dc is applied to terminal 27 (PGEN) and the return is applied to terminal 32 (NGEN). The presence of this voltage is indicated by the BKRVLTL signal. Positive power passes through a permissive relay K25P to terminal 28 (AUTO) with power indicated by the BKRPRM signal. Power then passes through the synchronizing pilot relay K25 to terminal 29 (MAN) as indicated by the BKRGES signal.

If a backup sync-check relay is used it is to be wired between terminals 29 and 30 (BKRH) with closure indicated by signal BKRGXSL. If a backup sync-check is not used a jumper between terminals 29 and 30 is used to complete the circuit and BKRGXSL and BKRGES both indicate that power is applied to the breaker coil. The breaker coil or a pilot relay is to be wired between terminals 31(BKRH) and 32 (NGEN).

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**Note** All voltage based feedback of synchronizing relay status is based on a voltage return path through terminal 32.

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Please refer to *GEI-100575* PTUR documentation for a detailed description of the synchronizing process.

## Feedback Signals

Feedback signals are dependent on the group of STUR. Possible signals include the following:

- Relay position feedback from STUR K1 and K2 trip relays.
- Solenoid voltage feedback associated with K1 and K2.
- Five voltage feedbacks associated with the sync function. The following signals are formed by testing the voltage between the desired signal and the return side of the power bus or N125GEN.
  - BKRVLTL – Voltage status of the power bus used to close the breaker.
  - L52G – Voltage feedback from an auxiliary contact on the 52G breaker. A separate set of customer screw terminals provides input.
  - BKRPRM – Voltage status of the breaker close permissive relay contact, K25P.
  - BKRGES – Voltage status of the combination of the K25P contacts wired in series with the K25 contacts.
  - BKRGSX – Voltage status of the series combination of K25P, K25, and an auxiliary backup sync check relay (K25A) which equals the voltage applied to the breaker coil or a pilot relay.
- Two sync relay coil drive feedback signals.
- Feedback signals provided by a trip card wired to J2

The relationship between feedback and STUR group is as follows

|        | Relay<br>Position | Solenoid<br>Volts | Sync Circuit<br>Volts | Sync Relay<br>Coils | Trip Card<br>Feedback |
|--------|-------------------|-------------------|-----------------------|---------------------|-----------------------|
| STURH1 | Yes               | Yes               |                       |                     |                       |
| STURH2 | Yes               | Yes               | Yes                   | Yes                 |                       |
| STURH3 |                   |                   |                       |                     | Yes                   |
| STURH4 |                   |                   | Yes                   | Yes                 | Yes                   |

## Emergency Stop Circuit

STUR contains no provisions for an emergency stop circuit.

## Failure Detection

An external test signal is required for speed input testing. Normal running speed signal failure detection is achieved through redundant signals applied to STUR. PT inputs require external test signals for proper feedback. Trip relays, depending on which STUR version is being tested, use forcibly guided contacts ensuring a feedback contact accurately represents the power contact position. Breaker closure relay contact logic includes voltage based status feedback announcing any unexpected behavior.



## ***Trip Board Comparison***

The following table compares existing primary trip boards to STUR.

*Trip Board Comparison Chart*

| <b>Board</b> | <b>TMR/Simplex</b> | <b>Output<br/>Contacts 125 V</b> | <b>Output<br/>Contacts 24 V</b> | <b>Estop</b> | <b>Sync Support</b> | <b>Trip<br/>Output Count</b> |
|--------------|--------------------|----------------------------------|---------------------------------|--------------|---------------------|------------------------------|
| TRPGH1B      | TMR                | 1A                               | No                              | No           | Yes                 | 3                            |
| TRPGH2B      | Simplex            | 1A                               | 3A                              | No           | Yes                 | 3                            |
| TRPLH1A      | TMR                | 1A                               | 3A                              | Yes          | Yes                 | 3                            |
| TRPSH1A      | TMR/Simplex        | 1A                               | 3A                              | Yes          | Yes                 | 3                            |
| TRPAH1A      | TMR                | No                               | 5A                              | Yes          | No                  | 2                            |
| TRPAH2A      | TMR                | 1A                               | No                              | Yes          | No                  | 2                            |
| STURH1A      | Simplex            | 0.5A                             | 5A                              | No           | No                  | 2                            |
| STURH2A      | Simplex            | 0.5A                             | 5A                              | No           | Yes                 | 2                            |
| STURH3A      | Simplex            | (TRPx)                           | (TRPx)                          | No           | No                  | (TRPx)                       |
| STURH4A      | Simplex            | (TRPx)                           | (TRPx)                          | No           | Yes                 | (TRPx)                       |

### ***Simplex Turbine Applications***

In simplex applications STUR accepts up to four pulse rate signals used to measure turbine speed. The PT signals provide voltage input from both sides of a 52G circuit breaker permitting automatic synchronization to be performed. The on-board trip relays provided by the H1 and H2 groups of STUR create a self-contained overspeed and synchronizing function. It is also possible to use the H3 or H4 group of STUR in a simplex application with a simplex trip terminal board cabled into STUR using the DC-37 pin connection.

### ***TMR Turbine Applications***

Three STUR/PTUR combinations can be used where TMR applications are needed. A typical application would use a TMR trip terminal board with group H3 or H4 of STUR. This provides trip relay outputs that are wired to vote on the terminal board. It is possible to use three H1 or H2 STUR boards in a TMR normally open tripping configuration as each trip relay provides two normally open contacts. When this is desired the STUR provides two parallel customer terminals on select points to allow TMR relay contact voting wiring to be installed without two wires under one terminal.

## ***Specification***

| <b>Item</b>                   | <b>Specification</b>                                                                                                                              |
|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of inputs              | 4 passive or active speed pickups<br>1 generator and 1 bus voltage potential transformer (H2, H4)<br>1 generator breaker status contact. (H2, H4) |
| Number of outputs             | 2 Primary trip relays (H1, H2)<br>2 Synchronizing relays (H2, H4)<br>1 DC-37 connector for primary trip terminal board (H3, H4)                   |
| MPU pulse rate range          | 2 Hz to 20 kHz                                                                                                                                    |
| MPU pulse rate accuracy       | 0.05% of reading                                                                                                                                  |
| MPU input circuit sensitivity | 27 mV pk (detects 2 rpm speed)                                                                                                                    |

| Item                                                  | Specification                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Generator and bus voltage sensors                     | Two single phase 115 V ac rms potential transformer inputs. Each input has less than 3 VA of loading.<br>Each PT input is magnetically isolated with a 1,500 V rms barrier.<br>Cable length can be up to 1,000 ft. of 18 AWG wiring.                                                                                                                                                                                      |
| Generator breaker circuits (synchronizing, K25, K25p) | External circuits should have a voltage range within 20 to 140 V dc. Circuits are rated for NEMA class E225 creepage and clearance. 250 V dc applications require interposing relays.<br>Contact rating 3.15 A @ 24 V dc, 1.2 A @ 48 V dc, 0.4 A @ 125 V dc, resistive.                                                                                                                                                   |
| Contact voltage sensing                               | 20 V dc indicates high and 6 V dc indicates low. Each circuit is optically isolated and filtered for 4 ms. Circuits will accept up to 145 V dc input.                                                                                                                                                                                                                                                                     |
| Trip Relays (K1, K2)                                  | Contact Rating: 4A @ 24 V dc, 4A @ 48 V dc, 2A @ 125 V dc for normally open contacts resistive. 4A @ 24 V dc, 4A @ 48 V dc, 0.3A @ 125 V dc for normally closed contacts resistive.<br>Minimum contact load >50 mW.<br>Maximum Switching Rate: 3 operations/minute at rated load, 60 operations/minute at minimum load<br>Associated printed circuit board designed for minimum of 20 A surge rating for 10 milliseconds. |
| <b>Physical</b>                                       |                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Size                                                  | 15.9 cm high x 17.8 cm, wide (6.25 in x 7 in)                                                                                                                                                                                                                                                                                                                                                                             |
| Technology                                            | Surface mount                                                                                                                                                                                                                                                                                                                                                                                                             |
| Temperature                                           | -30 to +65°C (-22 to + 149 °F)                                                                                                                                                                                                                                                                                                                                                                                            |
| Humidity                                              | 5% to 90% non-condensing                                                                                                                                                                                                                                                                                                                                                                                                  |
| Cooling                                               | Free air convection                                                                                                                                                                                                                                                                                                                                                                                                       |

## ***Diagnostics***

Diagnostic tests are made on the STUR as follows:

- Feedback from the solenoid relay drivers is checked; if there is a problem with the control signal a fault is created.
- Feedback from the relay contact position is checked; if there is a problem with the control signal a fault is created.
- Loss of solenoid power creates a fault.
- Slow synch check relay, slow auto synch relay, slow breaker, and locked up K25 relay; all of these create a fault.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG\_PTUR occurs. The diagnostic signals can be individually latched and then reset with the RESET\_DIA signal if they go healthy.
- Terminal board connectors have their own ID device that is interrogated by the I/O pack. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by PTUR and a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

There are no jumpers or hardware settings on the board.

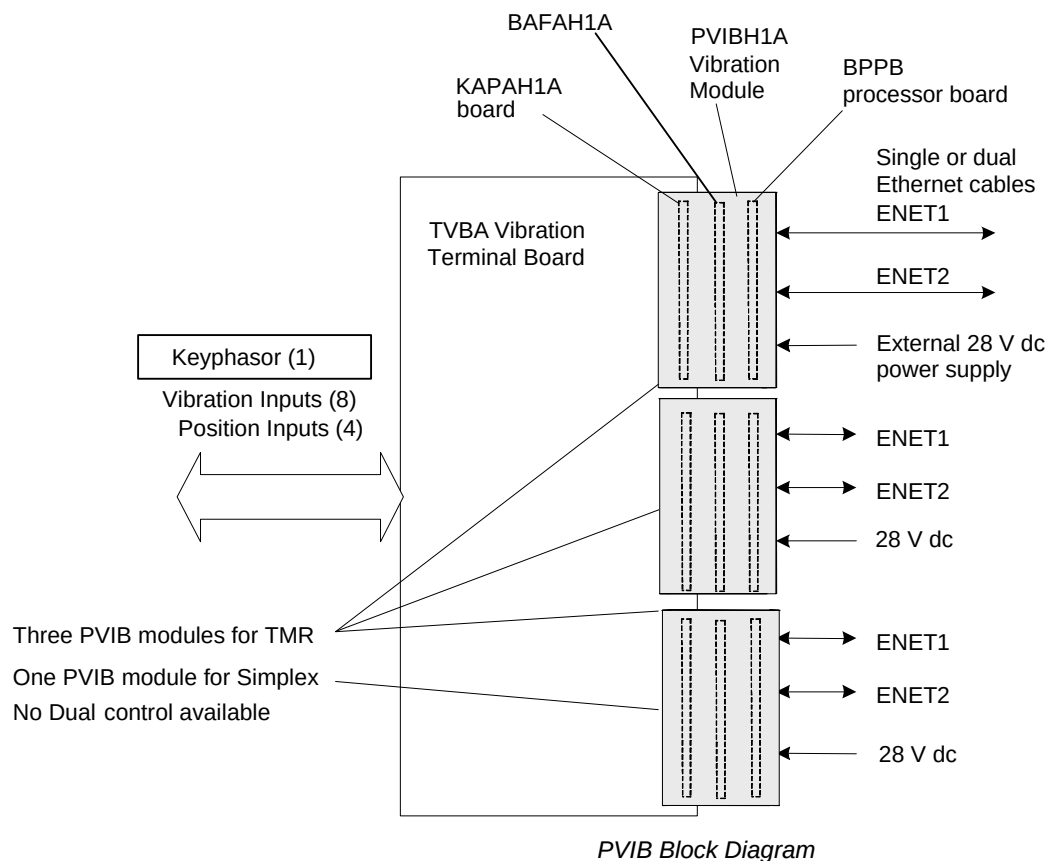
# PVIB Vibration Monitor Board

## PVIB Vibration Monitor

### Functional Description

The Vibration Monitor (PVIB) pack provides the electrical interface between one or two I/O Ethernet networks and the TVBA vibration terminal board. The pack contains a processor board common to all Mark\* VIE distributed I/O packs, an acquisition board and a daughterboard. The pack uses channels 1 through 8 to read vibration or proximity information from the following sensor types: Proximitors<sup>®</sup>, accelerometers with an integrated output (Channels 1-3 only), Velomitor<sup>®</sup>, or seismics. Channels 9 through 12 only support proximitors and channel 13 can input either a Keyphasor<sup>®</sup> signal-type or a proximity-type signal.

Input to the pack is through dual RJ45 Ethernet connectors and a 3-pin power input. The PVIB supports dual Ethernet networks for frame rates slower than 100 Hz. It supports single Ethernet network for frame rates of 3.125, 6.25, 12.5, 25, 50, and 100 Hz. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs, and local diagnostic serial communications are possible through an infrared port.



## Compatibility

PVIBH1A is compatible with the Vibration Terminal Board (TVBA), but not compatible with the TVIB. The following table gives details of the compatibility:

| Terminal Board | TVBA        | TVIB    |
|----------------|-------------|---------|
| Control mode   | Simplex-yes | TMR-yes |
|                |             | No      |

Control mode refers to the number of I/O packs used in a signal path:

- Simplex uses one I/O pack with one or two network connections.
- TMR uses three I/O packs with one network connection on each.

## Installation

### ➤ To install the PVIB pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PVIB I/O pack for simplex or three PVIB I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.
- 7 Verify that the TVBA's N28 power supply daughterboard is seated properly in the TVBA connector.

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**Note** The PVIB mounts directly to a Mark VIe terminal board. TMR-capable terminal boards have three DC-37 pin connectors and can also be used in simplex mode if only one PVIB is installed. The PVIB directly supports all of these connections.

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# **Operation**

## **Processor**

The processor board in the pack is common to all Mark VIe Ethernet I/O packs. It contains the following:

- High-speed processor with RAM and flash memory
- Two fully independent 10/100 Ethernet ports with connectors
- Hardware watchdog timer and reset circuit
- Internal I/O pack temperature sensor
- Infrared serial communications port
- Status-indication LEDs
- Electronic ID and the ability to read IDs on other boards
- Substantial programmable logic supporting the acquisition board
- Input power connector with soft start/current limiter
- Local power supplies, including sequencing and monitoring

The processor board connects to an acquisition board specific to the I/O pack function. Upon application of input power, the soft-start circuit ramps up the voltage available on the processor board. The local power supplies are sequenced on, and the processor reset is removed. The processor completes self-test routines and then loads application code specific to the I/O pack type from flash memory. The application code reads board ID information to ensure the correct matching of application code, acquisition board, and terminal board. With a good match, the processor attempts to establish Ethernet communications, starting with request of a network address. The address request uses the industry standard dynamic host configuration protocol (DHCP) and the unique identification read from the terminal board. After Ethernet initialization, the processor programs the on-board logic, runs the application, and enables the acquisition board to begin operation.

The processor application code contains all the logic necessary to allow the pack to operate from one or two Ethernet inputs. When operated from two Ethernet inputs, both network paths are active all the time. A failure of either network will not result in any disturbance to the I/O pack operation, and the failure will be indicated through the working network connection. This arrangement is more tolerant of faults than a classic hot-backup system where the second port is only used after a primary port failure is detected. The Ethernet ports on the processor auto-negotiate between 10 MB/s and 100 MB/s speed, and between half-duplex and full-duplex operation.

An industry-standard infrared serial communications port is provided on the processor board. Accessible through the pack front, this port provides diagnostic information on the pack status and an ability to program the pack when both Ethernet connections fail. It is possible to communicate with this port using most notebook computers and most hand-held Personal Digital Assistants (PDA).

## ***Vibration Monitoring Hardware***

The PVIB application-specific hardware consists of the analog filter acquisition board (BAFA), and the analog processing daughterboard (KAPA). The analog filter acquisition board provides the signal conditioning to center and amplify signal to improve analog-to-digital resolution. The first eight channels can be used for vibration and position signal information. Channels 9 through 12 support position information only. Channel 13 contains circuitry to support pedestal or slot-type Keyphasor.

Each of the 13 differential amplifier inputs has a digital analog converter (DAC) bias adjustment to null the dc content of the signal to better center the signal for the analog-to-digital (A/D) input range. The DAC bias command is stored in the microprocessor to be used in the gap calculation for the Proximity sensors. The input channel's gain stage allows the vibration signal to be amplified. Channels 1 through 8 and 13 have gain adjustments of 1x, 2x, 4x, or 8x, and channels 9 through 12 have gain adjustments of 1x and 4x for the vibration signal. Channels 1 through 8 and 13 use a multi-pole anti-aliasing filter with a band-pass frequency range of 7 kHz. Channels 9 through 12 use a multi-pole anti-aliasing filter with a cutoff-frequency of 2.2 kHz. The BAFA also provides voltage monitoring of the precision reference and the different supply voltages.

The analog processing board, KAPA, has the A/D conversion, the digital-to-analog (D/A) conversion, and the digital pre-processing for the PVIB. The A/D block has 16 channels, sampling at a frequency of 80 kHz with 14-bit A/Ds. The digital pre-processing is handled by a field-programmable gate-array (FPGA). The FPGA reads the A/Ds, digitally filters the sampled signals and the information is passed on to micro processor memory. The FPGA also runs the high-frequency section of the tracking filter and the 1x and 2x functions. The tracking filter is used to determine the vibration content of a turbine caused by a given rotation speed. The 1x vibration is the peak-to-peak magnitude of the radial movement in sync with the turbine shaft speed. The 1x calculation also provides the phase relationship of the vibration phasor relative to the Keyphasor. The 2x calculation provides the radial vibration component that is at twice the speed of the shaft.

## **Vibration Monitoring Application Firmware**

The vibration monitoring on the PVIB is as follows:

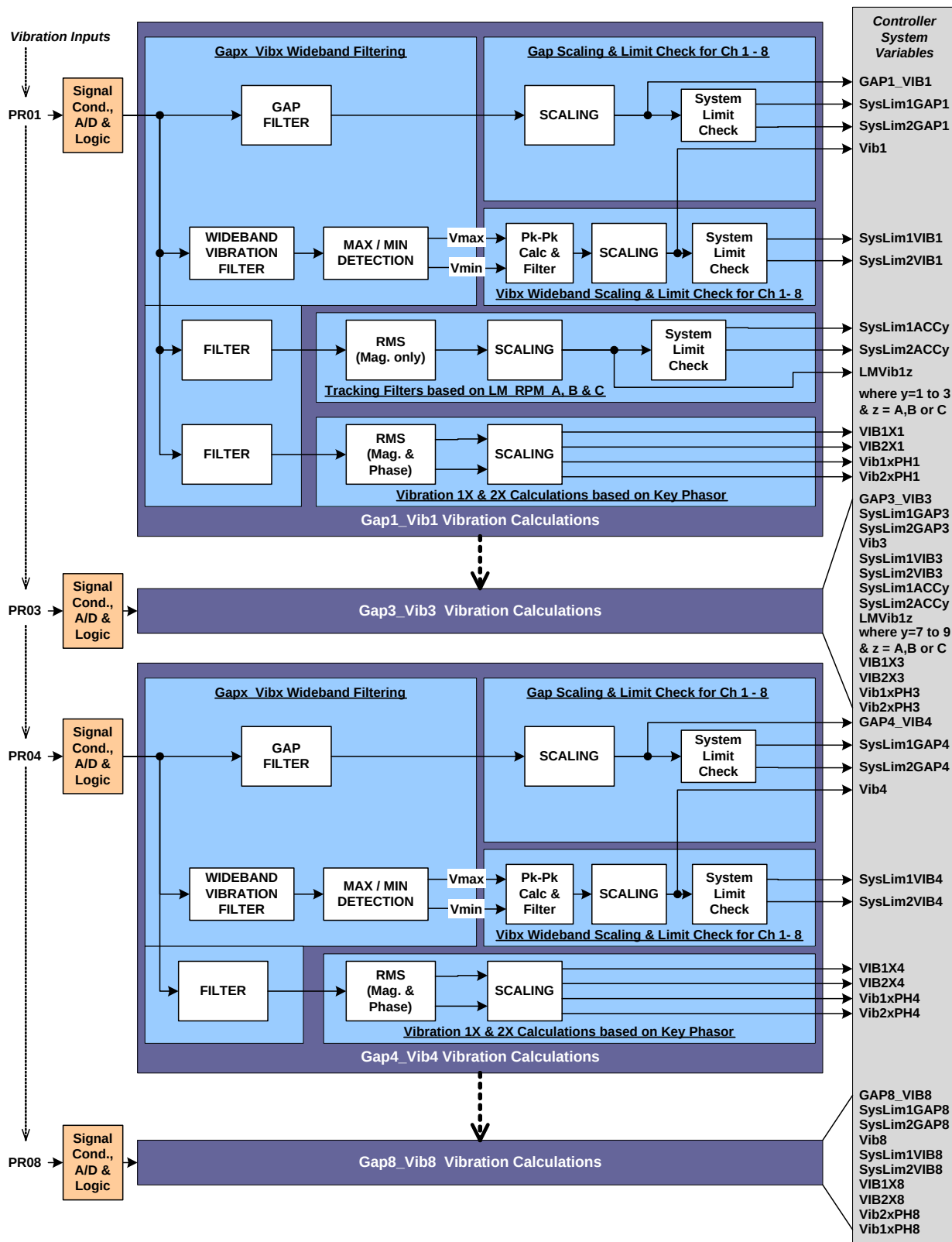
**Channels 1 through 3** can be used for position information from Proximitys, wideband vibration information from Proximitys, accelerometers with integrated outputs, Velomitors, and Seismics. 1x and 2x information can be derived from Proximitys viewing axial vibration information when a Keyphasor is used. Tracking filters are normally used in Mark V LM control applications.

Gapx\_Vibx\_Wideband\_Filtering runs every 10 ms activating the low-pass filter for the gap calculation, the wideband vibration filter, and the maximum/minimum detect for the peak-to-peak calculation. The Gap Scaling and Limit Check runs at the frame rate. This function converts the gap value from counts to the desired engineering units (EU). The system limit check provides the user with two detection limits and Boolean outputs for the status. The Vibx Wideband Scaling and Limit Check block runs every frame. The peak-to-peak calculation is based on the Vmax and Vmin values of the Gapx\_Vibx Wideband Filtering. The wideband peak-to-peak signal is filtered and then scaled to EU. The re-scaled wideband peak-to-peak signal is then run through a limit check. The limit check provides the Booleans, SysLim1VIBx and SysLim2VIBx for the limit check status.

Three tracking filters calculate the peak vibration for the LM applications when accelerometers are used. The tracking filters provide the vibration that occurs at the rotor speeds defined by the system outputs, LM\_RPM\_A, LM\_RPM\_B, and/or LM\_RPM\_C. LMVib1A is the vibration detected on channel 1 based on the rotor speed, LM\_RPM\_A. LMVib1B is the vibration detected on channel 1 based on rotor speed, LM\_RPM\_B and LMVib1C is based on LM\_RPM\_C.

The 1x and 2x filters provide the peak-to-peak vibration vector relative to the Keyphasor input from channel 13. VIB1X1 is the peak-to-peak magnitude of the vibration from channel 1 relative to the rpm based on the Keyphasor. Vib1xPH1 is the phase angle in degrees of the vibration vector from channel 1 relative to the Keyphasor. VIB2X1 is the peak-to-peak magnitude of the vibration from channel 1 relative to twice the Keyphasor rpm. VIB2XPH1 is the phase angle in degrees of the 2x vibration vector from channel 1.

**Channels 4 through 8** can be used for position information from Proximitys, wideband vibration information from Proximitys, Velomitors, and Seismics. 1x and 2x information can be derived from Proximitys viewing axial vibration information when a Keyphasor is used. Channels 4 through 8 are identical to channels 1 through 3 with the exception of the tracking filters. Channels 4 – 8 do not include the tracking filters.



Gapx\_Vibx\_Wideband\_Filtering Diagram



**Channels 9-12** are used for position information only. The Gapx\_Pos\_Filtering runs every 10 ms and filters the position information. Gapx\_Pos Scaling and Limit Check runs every frame. This function rescales the gap value from counts representing volts to EU based on the PVIB configuration. The System Limit Check can be used to set a Boolean at minimum or maximum limit values configured by the user.

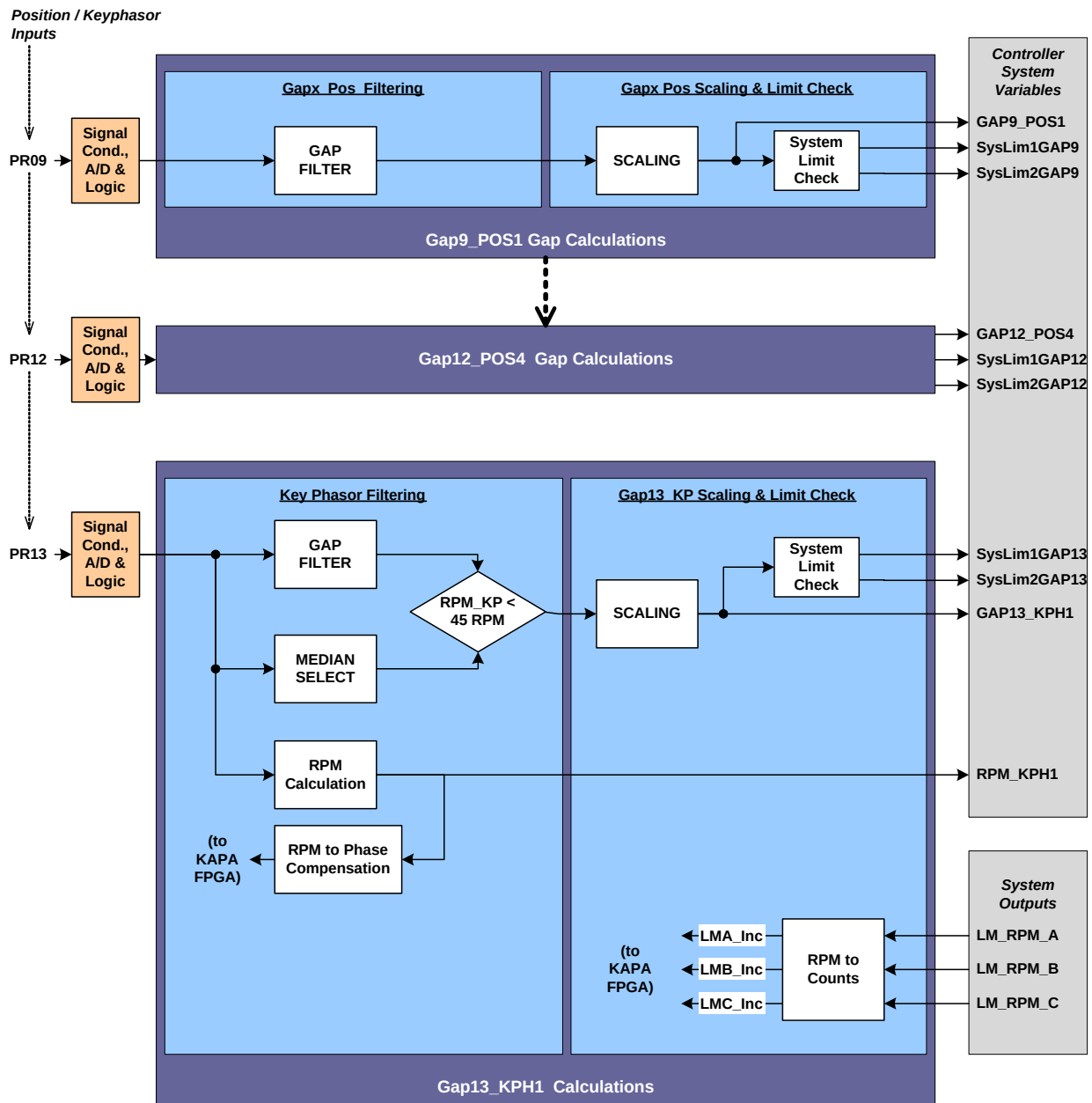
**Channel 13** supports position feedback and Keyphasor feedback. The Key\_Phase Filtering runs every 10 ms. A low-pass filter is used for the Gap filter calculation when the rotor speed is greater than or equal to 100 rpm. Below 100 rpm, the filter converts to a median select of the present and last two values. At very low speeds, the hardware Keyphasor comparator is not usable and the runtime application code determines speed by counting pulses detected through the system input, GAP13\_KPH1. The Keyphasor Filtering function also calculates the speed of the rotor.

The Gap13 KP Scaling and Limit check runs every frame. The Gap Scaling Limit Check performs the same way it does for channels 1 through 12. This function also inputs the three rotor speeds, LM\_RPM\_A, LM\_RPM\_B, and LM\_RPM\_C that are calculated externally to the PVIB.

*Signal Space Inputs for Sensor Types*

| Signal Space Input | Gapn_Vibn    | Gapy_Posn<br>(y = 1-4) | Gap13_Kph<br>1 | Vib1xn<br>Vib1xPhn<br>Vib2xn<br>Vib2xn | LMVibnA<br>LMVibnB<br>LMVibnC | Vibn         |
|--------------------|--------------|------------------------|----------------|----------------------------------------|-------------------------------|--------------|
| Sensor Type        |              |                        |                |                                        |                               |              |
| PosProx            | Channels 1-8 | Channels 9-12          | Channel 13     |                                        |                               | Channels 1-8 |
| VibProx-KPH        | Channels 1-8 |                        |                | Channels 1-8                           |                               | Channels 1-8 |
| VibLMAccel         | Channels 1-8 |                        |                |                                        | Channels 1-3                  | Channels 1-8 |
| VibSeismic         | Channels 1-8 |                        |                |                                        |                               | Channels 1-8 |
| VibVelomitor       | Channels 1-8 |                        |                |                                        |                               | Channels 1-8 |
| KeyPhasor          |              |                        | Channel 13     |                                        |                               |              |
| VibProx            | Channels 1-8 |                        |                |                                        |                               | Channels 1-8 |

n=channel



*Gapx\_Pos\_Filtering Diagram*

## ***Gapx\_Vibx\_Wideband\_Filtering Function***

The Gapx\_Vibx\_Wideband\_Filtering function executes at 100 Hz rate. The gap or position filter is a 2-pole, low-pass filter with a fixed cutoff frequency of 8 Hz. The output of the gap filter, LP\_Gap is expressed in counts and passes through a rolling-average filter to account for the slower activation rate Gap Scaling and Limit Check function.

The wideband vibration information can be shaped or conditioned based on the configuration parameter and FilterType. FilterType equal to Low-pass, Band-pass, or High-pass are used for the Seismic and Velomitor sensor types. FilterType equals to None is used by all the other sensor types. The Low-Pass filter can be configured for 2, 4, 6, or 8 pole behavior through the parameter Filtrlpattn. The 3 db frequency cutoff frequency, Filtrlpcutoff, is also adjustable. The High-pass filter can also be configured for 2, 4, 6 and 8 pole to sharpen the attenuation characteristics of the filter through the parameter, Filtrhpattn. The cutoff frequency, Filtrhpcutoff, is adjustable in configuration.

The wideband filtered vibration output, Vfout, goes through a minimum or maximum peak detect function. The detect function is based on the Keyphasor detected speed in rpm. If the rotor speed is less than 60 or greater than 2250 rpm, the capture window is 160 ms wide. If the speed range is between 60 and 480 rpm, the capture window is 2000 ms wide. If the speed range is between 480 and 2250 rpm, the capture window is 250 ms. The objective is to capture at least two cycles of vibration information to get an accurate peak-to-peak calculation.

## ***Vibx Wideband Scaling and Limit Check***

The Vibx Wideband Scaling and Limit Check operates on channels 1 through 8 of the PVIB. The calculation rate for the function is 0.5, 4 or 6.25 Hz. The calculation rate is based on the peak-to-peak scan times. For example, a scan time of 160 ms requires a calculation rate of 6.25 Hz.

The Vibx Wideband Scaling and Limit Check inputs are:

Vfmax

Vfmin

The Vibx Wideband Scaling and Limit Check outputs are:

VIBx, the wideband vibration in EU

SysLim1VIBx, the System Limit #1 Boolean; (Boolean is True if VIBx exceeds system limit 1)

SysLim2VIBx, the System Limit #2 Boolean. (Boolean is True if VIBx exceeds system limit 2)

The system output uses the System Limit Reset Boolean. If Reset is True, a latched System Limit Boolean is cleared.

The filtered peak-to-peak wideband vibration signal, FVMpp equals to Vfmax – Vfmin. FVMpp passes through a single-pole low-pass filter with an adjustable cutoff frequency, VIB\_PP\_Fltn.

The Vibx Wideband Scaling and Limit Check scaling block converts the filtered wideband peak-to-peak vibration from counts to EU peak or EU peak-peak, depending on the configuration parameter VibType. The scaling values are determined by the following configuration parameters:

**VibType** – determines the type of sensor being used.

**Scale** – gain factor expressed in volts/EU

**GnBiasOverride** – Gain Bias Override allows the user to override the default sensor gain value and use the configuration parameter, Gain. See table *Probe Nominal Settings* for sensor default values.

**Gain** – used only when GnBiasOverride = Enables and modifies the resolution of the incoming signal. Use of settings other than 1x DO NOT increase the net gain of the Vibx system input. The gain is applied to the input in the hardware, but is divided out in firmware for a net gain of 1. This provides amplification to small signals before being digitized to improve signal to noise ratio. The maximum signal amplitude (peak in volts) times the selected gain factor should not exceed 10 volts to avoid saturation.

The Vibx Wideband Scaling and Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

**SysLimxEnabl** – the System Limit (x=1 or 2) Enable is set to Enable to select the use of the block.

**SysLimxType** – the System Limit (x=1 or 2) Type selects whether the limit check does a >= check or a <= check.

**SysLimitx** – System Limit (x=1 or 2) is the limit value used in the >= or <= check.

**SysLimxLatch** – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched, the flag will remain True, even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxVIBy where x is the System Limit block number (1 or 2) and y is the PVIB channel input number (1–8).

### **Gap Wideband Scaling and Limit Check**

The Gap Wideband Scaling and Limit Check operates on channels 1 through 8 of the PVIB. The calculation rate for the function is based on the frame rate selected for IONet. The Gap Wideband Scaling and Limit Check input, Avg\_LP\_Gap is from the Gapx\_Vibx Wideband Filtering block. The system inputs or Gap Wideband Scaling and Limit Check outputs are:

Gapx\_VIBx, the position or gap value in engineering units (EU) for Proximitors, voltage in V dc for accelerometers with integrated outputs, seismics and Velomiters.

SysLim1GAPx, the System Limit #1 Boolean; (Boolean is True if GAPx\_VIBx exceeds system limit 1)

SysLim2GAPx, the System Limit #2 Boolean. (Boolean is True if GAP\_VIBx exceeds system limit 2)

The system output used is the System Limit Reset Boolean. If Reset is True, a latched System Limit Boolean is cleared.

The Gap Wideband Scaling and Limit Check scaling block converts the average-filtered gap signal, Avg\_LP\_Gap from counts to engineering units or Volts (dc) depending on the configuration parameter VibType. The scaling values are determined by the following configuration parameters:

**VibType** – determines the type of sensor being used.

**Scale** – gain factor expressed in volts/EU

**ScaleOff** – offset value in EU (used for position proximitors only)

**Snsr\_Offset** – the sensor offset or bias voltage (V dc) is used to remove most of the dc bias of the input signal and move it within the A/D input range. Used only when GnBiasOvrde = Enable

**GnBiasOvrde** – Gain Bias Override allows the user to override the sensor-specific default values for dc bias and Gain and use the configuration parameters, Gain and Snsr\_Offset. See table *Probe Nominal Settings* for sensor default values.

**Gain** – used only when GnBiasOvrde = Enable and modifies the resolution of the incoming signal. Use of settings other than 1x DO NOT increase the net gain of the Gapx system input. The gain is applied to the input in the hardware, but is divided out in firmware for a net gain of 1. This provides amplification to small signals before being digitized to improve signal to noise ratio. The maximum signal amplitude (peak in volts) times the gain factor chosen should not exceed 10 volts to avoid saturation.

The Gap Wideband Scaling and Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

**SysLimxEnabl** – the System Limit (x=1 or 2) Enable is set to Enable to select the use of the block.

**SysLimxType** – the System Limit (x=1 or 2) Type selects whether the limit check does a >= check or a <= check.

**SysLimitx** – System Limit (x=1 or 2) is the limit value used in the >= or <= check.

**SysLimxLatch** – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched, the flag will remain True, even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxGAPy where x is the System Limit block number (1 or 2) and y is the PVIB channel input number (1-8).

### ***Gapx\_POSy Gap Calculations***

The Gapx\_POSy Gap Calculations consists of the Gapx\_Pos Filtering and the Gapx\_Pos Scaling and Limit Check where x is the PVIB channel number 9 thru 12 and y is the position number 1 - 4. The Gapx\_POSy Gap Calculation's outputs are:

Gapx\_POSy, the position or gap value in engineering units (EU) for Proximitors

SysLim1GAPx, the System Limit #1 Boolean; (Boolean is True if GAPx\_POSy exceeds system limit 1)

SysLim2GAPx, the System Limit #2 Boolean. (Boolean is True if GAP\_POSy exceeds system limit 2)

The system output used is the System Limit Reset Boolean. If Reset is True, a latched System Limit Boolean is cleared.

The Gapx\_Pos Filtering is executed at a 100 Hz rate. The vibration input for this function comes from an array with 5 kHz sampled data. The gap or position filter is a 2-pole low-pass filter with a fixed cutoff frequency of 8 Hz. The output of the gap filter is expressed in counts and passes through a rolling-average filter to account for the slower execution rate Gapx\_Pos Scaling and Limit Check function.

The Gapx\_Pos Scaling and Limit Check scaling block converts the average-filtered gap signal, Avg\_LP\_Gap from counts to EU. The conversion is based upon the scaling variables gain factor SCALE, and the offset value Scale\_Off. The scaling values and scaling block topology are determined by the following configuration parameters:

**VibType** – determines the type of sensor being used.

**Scale** – gain factor expressed in volts/EU

**ScaleOffset** – offset value in EU

**Snsr\_Offset** – the sensor offset or bias voltage (V dc) is used to remove most of the dc bias of the input signal and move it within the A/D input range. Used only when GnBiasOvrde = Enable

**GnBiasOvrde** – Gain Bias Override allows the user to override the sensor-specific default values for DC bias and Gain and use the configuration parameters, Gain and Snsr\_Offset. See table *Probe Nominal Settings* for sensor default values.

**Gain** – used only when GnBiasOvrde = Enable and modifies the resolution of the incoming signal. Use of settings other than 1x DO NOT increase the net gain of the Gapx system input. The gain is applied to the input in the hardware, but is divided out in firmware for a net gain of 1. This provides amplification to small signals before being digitized to improve signal to noise ratio. The maximum signal amplitude (peak in volts) times the gain factor chosen should not exceed 10 volts to avoid saturation.

The Gapx\_Pos Scaling and Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

**SysLimxEnabl** – the System Limit (x=1 or 2) Enable is set to Enable to select the use of the block.

**SysLimxType** – the System Limit (x=1 or 2) Type selects whether the limit check does a >= check or a <= check.

**SysLimitx** – System Limit (x=1 or 2) is the limit value used in the >= or <= check.

**SysLimxLatch** – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched, the flag will remain True, even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxGAPy where x is the System Limit block number (1 or 2) and y is the PVIB channel input number (9 - 12).

## Gap13\_KPH1 Calculations

The Gap13\_KPH1 Calculations consists of the Keyphasor Filtering and the Gap13\_KP Scaling and Limit Check. The Gap13\_KPH1 Calculation's outputs are:

GAP13\_KPH1, the position or gap value in EU for the Keyphasor Proximitors

SysLim1GAP13, the System Limit #1 Boolean; (Boolean is True if GAP13\_KPH1 exceeds limit 1)

SysLim2GAP13, the System Limit #2 Boolean. (Boolean is True if GAP13\_KPH1 exceeds limit 2)

The Gap13\_KPH1 system outputs are:

SysLimReset, the System Limit Reset Boolean, (If Reset is True, a latched System Limit Boolean is cleared)

LM\_RPMx, rotor shaft speed in rpm from different stages of the turbine. (x = A, B or C)

The Keyphasor Filtering is executed at a 100 Hz rate. The input for this function comes from an array with 5 kHz sampled data. The Keyphasor Filtering uses the low-pass filter when the rotor speed based on the Keyphasor is greater than or equal to 100 rpm and uses a median select function if the speed is below 100 rpm. The gap or position filter is a 2-pole low-pass filter with a fixed cutoff frequency of 8 Hz. The median select filter uses the present value (n), the previous (n-1) and the value 2 samples back (n-2) to perform a median select on. The output of either filter is expressed in counts and passes through a rolling-average filter to account for the slower execution rate Gap13\_KP Scaling and Limit Check.

The Keyphasor Filtering also uses the input to pass through a single-pole low-pass filter with a cutoff fixed at 2.3 Hz. The output of this filter is added to the configuration parameter KPH\_Thrshld whose sign is based on the parameter, KPH\_Type. The output is written to the KAPA FPGA DAC.

The Keyphasor Filtering function reads the time registers from the KAPA FPGA and calculates the signal space output, RPM\_KPH1 in units of rpm.

The Gap13\_KP Scaling and Limit Check scaling block converts the average-filtered gap signal, Avg\_LP\_Gap from counts to EU. The Gap13\_KP calculation runs at the frame rate. The scaling values are determined by the following configuration parameters:

**VibType** – determines the type of sensor being used.

**Scale** – gain factor expressed in volts/EU

**Snsr\_Offset** – the sensor offset or bias voltage (Vdc) is used to remove most of the dc bias of the input signal and move it within the A/D input range. Used only when GnBiasOverride = Enable

**GnBiasOverride** – Gain Bias Override allows the user to override the sensor-specific default values for DC bias and Gain and use the configuration parameters, Gain and Snsr\_Offset. See table *Probe Nominal Settings* for sensor default values.

**Gain** – used only when GnBiasOvrde = Enable and modifies the resolution of the incoming signal. Use of settings other than 1x DO NOT increase the net gain of the Gapx system input. The gain is applied to the input in the hardware, but is divided out in firmware for a net gain of 1. This provides amplification to small signals before being digitized to improve signal to noise ratio. The maximum signal amplitude (peak in volts) times the gain factor chosen should not exceed 10 volts to avoid saturation.

The Gap13\_KP Scaling and Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

**SysLimxEnabl** – the System Limit (x=1 or 2) Enable is set to Enable to select the use of the block.

**SysLimxType** – the System Limit (x=1 or 2) Type selects whether the limit check does a >= check or a <= check.

**SysLimitx** – System Limit (x=1 or 2) is the limit value used in the >= or <= check.

**SysLimxLatch** – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched, the flag will remain True, even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxGAP13 where x is the System Limit block number (1 or 2).

### ***1X and 2X Calculations Based on Keyphasor***

The 1x and 2x calculations based on Keyphasor provides the peak-to-peak vibration component (harmonic magnitude and phase) at both the Keyphasor frequency and twice the frequency. The calculations consist of two sections:

- Low-Pass filter
- Magnitude and Phase Calculation
- The system inputs from the 1x and 2x calculations are:
  - Vib1Xy, the peak-to-peak magnitude of the vibration phasor that is rotating at the Keyphasor frequency
  - Vib1xPHy, the phase angle between the Keyphasor and the ViB1Xy vibration phasor
  - Vib2Xy, the peak-to-peak magnitude of the vibration phasor that is rotating at the twice the Keyphasor frequency
  - Vib1xPHy, the phase angle between the Keyphasor and the Vib2Xy vibration phasor

where y is the PVIB channel number from 1 to 8.

The Vibration 2x function is the same as the 1x function except the results are a peak-to-peak magnitude of the 2x vibration phasor, Vib2Xy rotating at twice the Keyphasor frequency and a phase of Vib2xPHy.

The scaling block converts the input units to Engineering units (EU). The scaling values are determined by the following configuration parameters:

**VibType** – determines the type of sensor being used.

**Scale** – gain factor expressed in volts/EU



## **Tracking Filters Based on LM\_RPM\_A, B, and C**

The tracking filters based on LM\_RPM\_A, B, and C provide the peak vibration component (harmonic magnitude only) at the speeds: LM\_RPM\_A, LM\_RPM\_B, and LM\_RPM\_C. The Tracking filters require both filter stages executing at 100 Hz and the magnitude calculation executing at the frame rate.

The system inputs from the tracking filters are:

- LMVibxA, the peak magnitude of the vibration component rotating at LM\_RPM\_A (RPM) speed
- LMVibxB, the peak magnitude of the vibration component rotating at LM\_RPM\_B (RPM) speed
- LMVibxC, the peak magnitude of the vibration component rotating at LM\_RPM\_C (RPM) speed
- SysLim1ACCx, the System Limit Boolean status of Limit1 where x = 1-9
- SysLim2ACCx, the System Limit Boolean status of Limit2 where x = 1-9

The scaling block converts the phasor magnitude to EU. The scaling values are determined by the following configuration parameters:

**VibType** – determines the type of sensor being used.

**Scale** – gain factor expressed in volts/EU

The Tracking Filter provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

**SysLimxEnabl** – the System Limit (x=1 or 2) Enable is set to Enable to select the use of the block.

**SysLimxType** – the System Limit (x=1 or 2) Type selects whether the limit check does a >= check or a <= check.

**SysLimitx** – System Limit (x=1 or 2) is the limit value used in the >= or <= check.

**SysLimxLatch** – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched, the flag will remain True, even if the limit value is no longer exceeded.

## **ID Line**

The processor board and acquisition board within the I/O pack contain electronic ID parts that are read during power initialization. A similar part located with each terminal board DC-37 pin connector allows the processor to confirm correct matching of I/O pack to terminal board and report board revision status to the system level control.

## **Power Management**

The I/O pack includes power management in the 28 V input circuit. The management function provides soft start to control current inrush during power application. After applying power, the circuit provides a fast current limit function to prevent a pack or terminal board failure from propagating back onto the 28 V power system. When power is present and working properly, the green PWR indicator will light. If the current limit function operates, the indicator will be out until the problem is cleared.

## Status LEDs

A green LED labeled PWR shows the presence of control power.

A red LED labeled ATTN shows pack status. This LED indicates five different conditions as follows:

- LED out - no detectable problems with the pack
- LED solid on - a critical fault is present that prevents the pack from operating critical faults include detected hardware failures on the processor or acquisition boards, or there is no application code loaded.
- LED flashing quickly ( $\frac{1}{4}$  cycle) - an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code
- LED flashing at medium speed ( $\frac{3}{4}$  cycle) - the pack is not online
- LED flashing slowly (2 cycle) - the pack has received a request to flash the LED to draw attention to the pack this is used during factory test or as an aid to confirm physical location against ToolboxST\* application settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

A yellow LED labeled TxRx is provided for each Ethernet port to indicate when the pack is transmitting or receiving data over the port.

## Specifications

| Item                            | Specification                                                                                                                                          |                        |                   |                                         |               |
|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-------------------|-----------------------------------------|---------------|
| Number of Channels              | TVBA: 13 probes<br>Eight Vibration (First three channels only support accelerometer inputs), four Position, one Keyphasor<br>PVIB: 13 probes supported |                        |                   |                                         |               |
| Vibration Inputs                | Measurement                                                                                                                                            | Range                  |                   | Accuracy                                | Frequency     |
|                                 |                                                                                                                                                        | (V dc + V ac)          | (V ac portion)    |                                         |               |
| Proximity<br>(channels 1-8)     | Displacement                                                                                                                                           | +1 to -20 V peak       | 0 to 4.5 V pp     | $\pm 0.030$ V pp*<br>(1% @ 3 V pp*)     | 5 to 200 Hz   |
|                                 |                                                                                                                                                        |                        |                   | $\pm 0.150$ V pp*<br>(5% @ 3 V pp*)     | 200 to 700 Hz |
| Seismic<br>(channels 1-8)       | Velocity                                                                                                                                               | +1 to -1 V peak        | 0 to 1.00 V peak  | Max [2% reading,<br>$\pm 0.008$ V peak] | 5 to 200 Hz   |
|                                 |                                                                                                                                                        |                        |                   | Max [5% reading,<br>$\pm 0.008$ V peak] | 200 to 700 Hz |
| Velomitor<br>(channels 1-8)     | Velocity                                                                                                                                               | -8.75 to 15.625 V peak | 0 to 3.625 V peak | Max [2% reading,<br>$\pm 0.008$ V peak] | 5 to 200 Hz   |
|                                 |                                                                                                                                                        |                        |                   | Max [5% reading,<br>$\pm 0.008$ V peak] | 200 to 700 Hz |
| Accelerometer<br>(channels 1-3) | Velocity<br>(tracking filter)                                                                                                                          | -8.75 to -11.5 V peak  | 0 to 1.5 V peak   | $\pm 0.015$ V peak                      | 10 to 350 Hz  |
| <b>Position Inputs</b>          |                                                                                                                                                        |                        |                   |                                         |               |
| Position<br>(channels 1-13)     | Displacement<br>(Gap)                                                                                                                                  | -0.5 to -20 V dc       | N/A               | $\pm 0.2$ V dc<br>(1% of full scale)    | N/A           |
| Keyphasor<br>(channel 13 only)  | Displacement<br>(Gap)                                                                                                                                  | -0.5 to -20 V dc       | N/A               | $\pm 0.2$ V dc<br>(1% of full scale)    | N/A           |

| Item                    | Specification                                                                                                                                                                                                   |     |     |                                                                                                                      |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|----------------------------------------------------------------------------------------------------------------------|
|                         | Speed                                                                                                                                                                                                           | N/A | N/A | ±0.1 % of full scale 2 to 20,000 rpm speed                                                                           |
|                         | Phase                                                                                                                                                                                                           | N/A | N/A | ±1 degree for 1x Up to 333 Hz<br>±2 degrees for 2x Up to 667 Hz<br>(1x vibration component with respect to key slot) |
| Buffered Outputs        | Amplitude accuracy is 0.1 % for signal to Bently Nevada <sup>*</sup> 3500 system.<br>A -11 V dc ±5% bias is added to output when a seismic probe used.<br>Sinks a minimum of 3 mA when interfacing a velomitor. |     |     |                                                                                                                      |
| Probe Power             | -24 V dc from the -28 V dc bus, each probe supply is current limited. 12 mA load per transducer                                                                                                                 |     |     |                                                                                                                      |
| Probe Signal Resolution | Minimum of 14-bit resolution for full scale ranges defined                                                                                                                                                      |     |     |                                                                                                                      |
| Open Circuit Detection  | Open ckt. Defined as a gap voltage more positive than -1.0 V dc for Proximity, Accelerometer and Velomitor inputs and a bias current >1 mA for Seismic.                                                         |     |     |                                                                                                                      |
| Common Mode Voltage     | Minimum of 5 V dc                                                                                                                                                                                               |     |     |                                                                                                                      |
| CMRR @ 50/60 Hz         | -50 dB                                                                                                                                                                                                          |     |     |                                                                                                                      |
| Size                    | 8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in. x 1.65 in. x 4.78 in.)                                                                                                                                     |     |     |                                                                                                                      |
| Technology              | Surface-mount                                                                                                                                                                                                   |     |     |                                                                                                                      |

\* V pp - V peak-peak

#### *Probe Nominal Settings*

| Probe Type    | Gain | Snsr_Offset (Vdc) | Scale(typical value) |
|---------------|------|-------------------|----------------------|
| Proximity     | 1x   | 10                | 200 mv/mil           |
| Seismic       | 8x   | 0                 | 150 mv/ips           |
| Velomitor     | 2x   | 12                | 100 mv/ips           |
| Accelerometer | 4x   | 10                | 150 mv/ips           |
| Position      | 1x   | 10                | 200 mv/mil           |
| Keyphasor     | 1x   | 10                | 200 mv/mil           |

**Note** These are the default settings used if GnBiasOvrde=Disable.

## ***Diagnostics***

The pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each vibration input has hardware limit checking based on preset (configurable) high and low levels near the end of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. The logic signal, L3DIAG\_PVIB, refers to the entire board.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, to enable/disable, and as latching/non-latching. RESET\_SYS resets the out of limits.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

**Note** The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

| Parameter     | Description                                              | Choices         |
|---------------|----------------------------------------------------------|-----------------|
| System Limits | Enable system limits                                     | Enable, Disable |
| Vib_PP_Fltr   | First order filter time constant (sec)                   | 0.01 to 2       |
| MaxVolt_Prox  | Maximum Input Volts (negative), healthy Input, Prox      | -4 to 0         |
| MinVolt_Prox  | Minimum Input Volts (negative), healthy Input, Prox      | -24 to -16      |
| MaxVolt_KP    | Maximum Input Volts (negative), healthy Input, Keyphasor | -4 to 0         |
| MinVolt_KP    | Minimum Input Volts (negative), healthy Input, Keyphasor | -24 to -16      |
| MaxVolt_Seis  | Maximum Input Volts (positive), healthy Input, Seismic   | 0 to 1.5        |
| MinVolt_Seis  | Minimum Input Volts (negative), healthy Input, Seismic   | -1.5 to 0       |
| MaxVolt_Acc   | Maximum Input Volts, healthy Input, Accel or Velomitor   | -12 to +1.5     |
| MinVolt_Acc   | Minimum Input Volts, healthy Input, Accel or Velomitor   | -24 to -1       |

All the other I/O configuration parameters are defined under the specific pack or terminal board variables given in the following sections.

### PVIB Variable Definitions

| Name                             | Description                                                                      | Setting                  |
|----------------------------------|----------------------------------------------------------------------------------|--------------------------|
| L3DIAG_PVIB                      | PVIB Diagnostics                                                                 | (Input Boolean)          |
| SysLim1GAPx<br>where x = 1 to 13 | Boolean set TRUE if System Limit 1 exceeded for Gap x input                      | (Input FLOAT)            |
| SysLim2GAPx<br>where x = 1 to 13 | Boolean set TRUE if System Limit 2 exceeded for Gap x input                      | (Input FLOAT)            |
| SysLim1VIBx<br>where x = 1 to 8  | Boolean set TRUE if System Limit 1 exceeded for Vib x input                      | (Input FLOAT)            |
| SysLim2VIBx<br>where x = 1 to 8  | Boolean set TRUE if System Limit 2 exceeded for Vib x input                      | (Input FLOAT)            |
| SysLim1ACCx<br>where x = 1 to 9  | Boolean set TRUE if System Limit 1 exceeded for Accelerometer x input            | (Input FLOAT)            |
| SysLim2ACCx<br>where x = 1 to 9  | Boolean set TRUE if System Limit 2 exceeded for Accelerometer x input            | (Input FLOAT)            |
| LMVibxA<br>where x = 1-3         | Vib, 1X component, for LM_RPM_A, input x - Card Point                            | Point Edit (Input FLOAT) |
| FltrLpcutoff                     | Low Pass 3db point (cutoff in Hz)                                                | 1.5 to 5 Hz              |
| SysLimEnabl                      | Enable System Limit 1 Fault Check                                                | Enable, Disable          |
| SysLim1Latch                     | Latch system Limit 1 Fault                                                       | Latch, Not Latch         |
| SysLim1Type                      | System Limit 1 Check Type                                                        | >= or <=                 |
| SysLimit1                        | System Limit 1 – Vibration in mils (Prox) or inch / sec (Seismic, Accelerometer) | -100 to +100             |
| SysLim2Enabl                     | Enable System Limit 2 (same configuration as for Limit 1)                        | Enable, Disable          |
| SysLim2Latch                     | Latch system Limit 2 Fault                                                       | Latch, Not Latch         |
| SysLim2Type                      | System Limit 2 Check Type                                                        | >= or <=                 |

| Name                           | Description                                                                      | Setting                  |
|--------------------------------|----------------------------------------------------------------------------------|--------------------------|
| SysLimit2                      | System Limit 2 – Vibration in mils (Prox) or inch/sec (Seismic, Accelerometer)   | -100 to +100             |
| TMR_DiffLmt                    | Difference Limit for Voted TMR Inputs in Volts or Mils                           | -100 to +100             |
| LMVibxB<br>where x = 1-3       | Vib, 1X component, for LM_RPM_B, input x - Card Point                            | Point Edit (Input FLOAT) |
| Filtrpcutoff                   | Low Pass 3db point (cutoff in Hz)                                                | 1.5 to 5 Hz              |
| SysLimEnabl                    | Enable System Limit 1 Fault Check                                                | Enable, Disable          |
| SysLim1Latch                   | Latch system Limit 1 Fault                                                       | Latch, Not Latch         |
| SysLim1Type                    | System Limit 1 Check Type                                                        | >= or <=                 |
| SysLimit1                      | System Limit 1 – Vibration in mils (Prox) or inch / sec (Seismic, Accelerometer) | -100 to +100             |
| SysLim2Enabl                   | Enable System Limit 2 (same configuration as for Limit 1)                        | Enable, Disable          |
| SysLim2Latch                   | Latch system Limit 2 Fault                                                       | Latch, Not Latch         |
| SysLim2Type                    | System Limit 2 Check Type                                                        | >= or <=                 |
| SysLimit2                      | System Limit 2 – Vibration in mils (Prox) or inch / sec (Seismic, Accelerometer) | -100 to +100             |
| TMR_DiffLmt                    | Difference Limit for Voted TMR Inputs in Volts or Mils                           | -100 to +100             |
| LMVibxC<br>where x = 1-3       | Vib, 1X component, for LM_RPM_C, input x - Card Point                            | Point Edit (Input FLOAT) |
| Filtrpcutoff                   | Low Pass 3db point (cutoff in Hz)                                                | 1.5 to 5 Hz              |
| SysLimEnabl                    | Enable System Limit 1 Fault Check                                                | Enable, Disable          |
| SysLim1Latch                   | Latch system Limit 1 Fault                                                       | Latch, Not Latch         |
| SysLim1Type                    | System Limit 1 Check Type                                                        | >= or <=                 |
| SysLimit1                      | System Limit 1 – Vibration in mils (Prox) or inch / sec (Seismic, Accelerometer) | -100 to +100             |
| SysLim2Enabl                   | Enable System Limit 2 (same configuration as for Limit 1)                        | Enable, Disable          |
| SysLim2Latch                   | Latch system Limit 2 Fault                                                       | Latch, Not Latch         |
| SysLim2Type                    | System Limit 2 Check Type                                                        | >= or <=                 |
| SysLimit2                      | System Limit 2 – Vibration in mils (Prox) or inch / sec (Seismic, Accelerometer) | -100 to +100             |
| TMR_DiffLmt                    | Difference Limit for Voted TMR Inputs in Volts or Mils                           | -100 to +100             |
| PM_KPH                         | Speed of Keyphasor in RPM                                                        | (Input FLOAT)            |
| Vib1Xy<br>where y = 1 thru 8   | Vibration, 1X component only, displacement for input y                           | (Input FLOAT)            |
| Vib1xPHy<br>where y = 1 thru 8 | Angle of 1X component to Keyphasor for input y                                   | (Input FLOAT)            |
| Vib2Xy<br>where y = 1 thru 8   | Vibration, 2X component only, displacement for input y                           | (Input FLOAT)            |
| Vib2xPHy<br>where y = 1 thru 8 | Angle of 2X component to Keyphasor for input y                                   | (Input FLOAT)            |
| LM_RPM_A                       | Speed A in RPM                                                                   | (Output FLOAT)           |
| LM_RPM_B                       | Speed B in RPM                                                                   | (Output FLOAT)           |
| LM_RPM_C                       | Speed C in RPM                                                                   | (Output FLOAT)           |

## IS200TVBA Variable Definitions

| Name                                 | Description                                                                                                                  | Choices                                                                     |
|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| GAPx_VIBx<br>where x = 1 through 8   | Average Air Gap (Prox) or V dc (other sensors) - Card Point(s)                                                               | Point Edit (Input FLOAT)                                                    |
| VIB_Type                             | Type of vibration probe                                                                                                      | Unused, PosProx, VibProx, VibProx-KPH1, VibLMAccel, VibVelomitor, Keyphasor |
| VIB_Scale                            | Volts/mil or Volts/ips                                                                                                       | 0 to 2                                                                      |
| ScaleOff                             | Scale offset for Prox position only, in mils                                                                                 | 0 to 90                                                                     |
| GnBias Ovrde                         | Gain Bias Override                                                                                                           | Enable, Disable                                                             |
| Snsr_Offset                          | Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvrde is enabled | ±13.5 V dc                                                                  |
| SysLim1Enabl                         | Enable System Limit 1                                                                                                        | Enable, Disable                                                             |
| SysLim1Latch                         | Latch the alarm                                                                                                              | Latch, Not Latch                                                            |
| SysLimi1Type                         | System Limit 1 Check Type                                                                                                    | >= or <=                                                                    |
| SysLimit1                            | System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox)                                                   | -100 to +100                                                                |
| SysLim2Enabl                         | Enable System Limit 2                                                                                                        | Enable, Disable                                                             |
| SysLim2Latch                         | Latch the alarm                                                                                                              | Latch, Not Latch                                                            |
| SysLimi2Type                         | System Limit 2 Check Type                                                                                                    | >= or <=                                                                    |
| SysLimit2                            | System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox)                                                   | -100 to +100                                                                |
| TMR_DiffLimt                         | Difference Limit for Voted TMR Inputs in Volts or Mils                                                                       | -100 to +100                                                                |
| Vibx where x =1 thru 8               | Vibration, displacement (pk-pk) or velocity (pk) - Card Point                                                                | Point Edit (Input FLOAT)                                                    |
| FilterType                           | Filter used for Velomitor and Seismic only                                                                                   | None, Low Pass, High Pass or Band Pass                                      |
| Fltrhpcutoff                         | High Pass 3db point (cutoff in Hz)                                                                                           | 4 to 30 Hz                                                                  |
| Fltrhpattn                           | Slope or attenuation of filter after cutoff                                                                                  | 2, 4, 6 or 8 pole                                                           |
| Fltrlpcutoff                         | Low Pass 3db point (cutoff in Hz)                                                                                            | 300 to 2300 Hz                                                              |
| Fltrlpattn                           | Slope or attenuation of filter after cutoff                                                                                  | 2, 4, 6 or 8 pole                                                           |
| SysLim2Enabl                         | Enable System Limit 2                                                                                                        | Enable, Disable                                                             |
| SysLim2Latch                         | Latch the alarm                                                                                                              | Latch, Not Latch                                                            |
| SysLimi2Type                         | System Limit 2 Check Type                                                                                                    | >= or <=                                                                    |
| SysLimit2                            | System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox)                                                   | -100 to +100                                                                |
| TMR_DiffLimt                         | Difference Limit for Voted TMR Inputs in Volts or Mils                                                                       | -100 to +100                                                                |
| GAPx+8_POSx<br>where x = 1 through 4 | Position Probe - Card Point                                                                                                  | Point Edit (Input FLOAT)                                                    |
| Type                                 | Type of vibration probe                                                                                                      | Unused or PosProx                                                           |
| Scale                                | Volts/mil                                                                                                                    | 0 to 2                                                                      |
| ScaleOff                             | Scale offset for Prox position only, in mils                                                                                 | 0 to 90                                                                     |
| GnBias Ovrde                         | Gain Bias Override                                                                                                           | Enable, Disable                                                             |
| Snsr_Offset                          | Amount of voltage bias (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvrde is enabled | ±13.5 V dc                                                                  |
| SysLimi1Type                         | System Limit 1 Check Type                                                                                                    | >= or <=                                                                    |
| SysLimit1                            | System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox)                                                   | -100 to +100                                                                |
| SysLim2Enabl                         | Enable System Limit 2                                                                                                        | Enable, Disable                                                             |
| SysLim2Latch                         | Latch the alarm                                                                                                              | Latch, Not Latch                                                            |

| Name         | Description                                                                                                                  | Choices                      |
|--------------|------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| SysLimi2Type | System Limit 2 Check Type                                                                                                    | >= or <=                     |
| SysLimit2    | System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox)                                                   | -100 to +100                 |
| TMR_DiffLimt | Difference Limit for Voted TMR Inputs in Volts or Mils                                                                       | -100 to +100                 |
| GAP13_KPH1   | Keyphasor Probe air gap - Card Point                                                                                         | Point Edit (Input FLOAT)     |
| Type         | Type of vibration probe                                                                                                      | Unused, Keyphasor or PosProx |
| Scale        | Volts/mil                                                                                                                    | 0 to 2                       |
| ScaleOff     | Scale offset for Prox position only, in mils                                                                                 | 0 to 90                      |
| GnBias Ovrde | Gain Bias Override                                                                                                           | Enable, Disable              |
| Snsr_Offset  | Amount of voltage bias (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvrde is enabled | ±13.5 V dc                   |
| SysLim1Enabl | Enable System Limit 1                                                                                                        | Enable, Disable              |
| SysLim1Latch | Latch the alarm                                                                                                              | Latch, Not Latch             |
| SysLimi1Type | System Limit 1 Check Type                                                                                                    | >= or <=                     |
| SysLimit1    | System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox)                                                   | -100 to +100                 |
| SysLim2Enabl | Enable System Limit 2                                                                                                        | Enable, Disable              |
| SysLim2Latch | Latch the alarm                                                                                                              | Latch, Not Latch             |
| SysLimi2Type | System Limit 2 Check Type                                                                                                    | >= or <=                     |
| SysLimit2    | System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox)                                                   | -100 to +100                 |
| TMR_DiffLimt | Difference Limit for Voted TMR Inputs in Volts or Mils                                                                       | -100 to +100                 |

## Alarms

### PVIB Specific Alarms

| Alarm ID | Alarm Description                                                    | Possible Cause                                                                                                                  | Solution |
|----------|----------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|----------|
| 32       | A/D Converter Channel {0:F0} Calibration Outside of Spec             | Board failed to auto-calibrate on power-up. Board failure.                                                                      |          |
| 33-45    | TVBA Analog Input {0:F0} Out of Sensor Limits or Saturated.          | Terminal point voltage outside of limits for sensor type. Bias level, Gain, or sensor limits improperly set for sensor/channel. |          |
| 46       | D/A Converter Channel {0:F0} Calibration Outside of Spec             | Board failed to auto-calibrate on power-up. Board failure                                                                       |          |
|          | Logic Signal \$V Voting Mismatch                                     | A problem with the input. This could be the device, the wire to the terminal board, or the terminal board.                      |          |
|          | Input Signal \$V Voting Mismatch, Local={0:F3}, Voted={1:F3}         | A problem with the input. This could be the device, the wire to the terminal board, or the terminal board.                      |          |
| 47       | KAPA Download/Initialization Error Detected                          | Board failure                                                                                                                   |          |
| 48       | KAPA FIFO Data Corrupted. Expected ID {0:F0} Read ErrCntr/ID {1:F0}. | Board failure or software process conflict that may be cleared by hard reset.                                                   |          |

| Alarm ID | Alarm Description                                              | Possible Cause                                                                    | Solution |
|----------|----------------------------------------------------------------|-----------------------------------------------------------------------------------|----------|
| 49       | KAPA failure. Status {0:F0}.                                   | Board failure                                                                     |          |
| 50       | DC Isolation Test Failure. Channel {0:F0}.                     | Board failed to auto-calibrate on power-up. Board failure.                        |          |
| 51       | BPPB Failure. Status {0:F0}.                                   | Board failure                                                                     |          |
| 52-64    | TVBA Analog Input {0:F0} Open Circuit at {1:F1} Volts.         | An open circuit has been detected on the terminal board based on the sensor type. |          |
| 65       | Negative 28 Volt Power Low at {0:F0} Counts.                   | Terminal board failure                                                            |          |
| 66       | Dual Ethernets not supported with 10 msec frame rate.          | Remove second Ethernet connection.                                                |          |
| 67       | Reference Channel Failed Calibration.                          | Board failed to auto-calibrate on power-up. Board failure                         |          |
| 68       | KAPA board is above temperature limit at {0:F1} deg F          | Board overheated or temperature sensor failure                                    |          |
| 69       | KAPA Channel 1,5,9,13 ADC Failure. Status {0:F0}.              | Board failure                                                                     |          |
| 70       | KAPA Channel 2,6,10 ADC Failure. Status {0:F0}.                | Board failure                                                                     |          |
| 71       | KAPA Channel 3,7,11 ADC Failure. Status {0:F0}.                | Board failure                                                                     |          |
| 72       | KAPA Channel 4,8,12 ADC Failure. Status {0:F0}.                | Board failure                                                                     |          |
| 73       | 1x2x Phase Calibration Level {0:F0} Failure on Channel {1:F0}. | Board failed to auto-calibrate on power-up. Board failure.                        |          |



## I/O Pack Alarms

| Fault | Fault Description                                                           | Possible Cause                                                                                                                                            |
|-------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2     | Flash memory CRC failure                                                    | Board firmware programming error (board will not go online)                                                                                               |
| 3     | CRC failure override is active                                              | Board firmware programming error (board is allowed to go online)                                                                                          |
| 4     | I/O pack in stand alone mode                                                | Invalid command line option                                                                                                                               |
| 5     | I/O pack in remote I/O mode                                                 | Invalid command line option                                                                                                                               |
| 6     | Special user mode active. Now [ ]                                           | Invalid command line option                                                                                                                               |
| 7     | I/O pack – The I/O pack has gone to the offline state                       | Lost communication with controller                                                                                                                        |
| 16    | System limit checking is disabled                                           | System checking was disabled by configuration                                                                                                             |
| 30    | ConfigCompatCode mismatch; Firmware: [ ]                                    | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 31    | IOCompatCode mismatch; Firmware: [ ]                                        | A tre file has been installed that is incompatible with the firmware on the I/O board. Either the .tre file or firmware must change. Contact the factory. |
| 256   | I/O pack [ ] V power supply voltage is low                                  | Supply voltage below 26.5 V dc                                                                                                                            |
| 257   | I/O pack power supply voltage is low                                        | Supply voltage below 18 V dc                                                                                                                              |
| 258   | I/O pack Temperature [ ] °F is out of range [ ] to [ ] °F                   | Temperature went outside -20°C to +85°C (-4 °F to +185 °F)                                                                                                |
| 261   | Unable to read configuration file from flash                                | Need to download configuration to the pack                                                                                                                |
| 262   | Bad configuration file detected                                             | Configuration file not compatible, re-download                                                                                                            |
| 263   | I/O pack configuration – bad name detected                                  | Wrong configuration file for I/O pack                                                                                                                     |
| 264   | I/O pack configuration – bad config compatibility code                      | Wrong configuration revision for I/O pack                                                                                                                 |
| 265   | I/O pack mapper – EGD header size mismatch                                  | Controller EGD revision code not supported                                                                                                                |
| 266   | I/O pack configuration – configuration size mismatch                        | Incorrect configuration file size received                                                                                                                |
| 267   | FPGA – name mismatch detected                                               | Wrong configuration for FPGA in I/O pack                                                                                                                  |
| 268   | FPGA - incompatible revision: Found [ ] Need; [ ]                           | Wrong revision of FPGA firmware                                                                                                                           |
| 269   | I/O pack mapper – initialization failure                                    | Mapper process was not able to start.                                                                                                                     |
| 270   | I/O pack mapper – mapper terminated                                         | Mapper process stopped, no communication                                                                                                                  |
| 271   | I/O pack mapper – unable to Export Exchange [ ]                             | EGD not being sent to Controller                                                                                                                          |
| 272   | I/O pack mapper – Unable to Import Exchange [ ]                             | Not receiving EGD information from Controller                                                                                                             |
| 273   | IONet-EGD message – Illegal version                                         | EGD protocol version incorrect, greater than current version                                                                                              |
| 274   | IONet-EGD – received redundant exchange from unknown address                | Controller received EGD message from unknown address                                                                                                      |
| 275   | Consumer E_Id [ ], P_Id [ ], RcvdID= [ ], LastID= [ ], Out of order         | Message sequence number was out of order, less than required                                                                                              |
| 276   | IONet-EGD – ProdID [ ], ExchID [ ], UNHEALTHY (Bad Configuration Time)      | Message version mismatch                                                                                                                                  |
| 277   | IONet-EGD – Signature mismatch E_Id= [ ] P_Id= [ ], =Expctd= [ ], Rcvd= [ ] | Message version mismatch                                                                                                                                  |
| 278   | BAD LENGTH ProdID [ ], ExchID [ ], expected [ ], got [ ]                    | Exchange message wrong length                                                                                                                             |
| 293   | IONet-EGD – Waiting on IP address from DHCP on subnet [ ] before continuing | Controller problem, or pack not configured, or incorrect ID                                                                                               |
| 301   | I/O pack - XML files are missing                                            | I/O pack I/O configuration files missing                                                                                                                  |
| 314   | Controller pid [ ], exch [ ] timed out, IONet [ ]                           | I/O pack outputs not received from controller                                                                                                             |
| 315   | Controller pid [ ], exch [ ] received too short, IONet [ ]                  | I/O pack outputs exchange received is shorter than expected                                                                                               |
| 316   | Controller pid [ ], exch [ ] major sig mismatch, IONet [ ]                  | I/O pack outputs exchange received with major signature different than expected                                                                           |

| <b>Fault</b> | <b>Fault Description</b>                                        | <b>Possible Cause</b>                                                                   |
|--------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 317          | Controller pid [ ], exch [ ] minor sig mismatch, IONet [ ]      | I/O pack outputs exchange received with minor signature different than expected         |
| 318          | Controller pid [ ], exch [ ] cfg timestamp mismatch, IO-Net [ ] | I/O pack outputs exchange received with configuration timestamp different than expected |
| 335          | Code Segment CRC mismatch                                       | Process Code Segment CRC mismatch                                                       |
| 338          | I/O pack Mapper SSI signals are not being updated               | I/O pack SSI data is not being updated                                                  |
| 339          | I/O pack App SSO signals are not being received                 | I/O pack SSO data is not being updated                                                  |
| 340          | I/O pack Mapper static data structure CRC mismatch              | Mapper static data CRC does not match                                                   |
| 341          | I/O pack Mapper I/O compatibility code mismatch                 | I/O pack mapper I/O Compat does not match firmware                                      |
| 342          | I/O pack App compatibility code mismatch                        | I/O pack App I/O Compat does not match firmware                                         |
| 343          | I/O pack App BOPLIB static data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 344          | I/O pack process code segment CRC mismatch                      | I/O pack process - code seg CRC bad                                                     |
| 345          | I/O pack App static config data CRC mismatch                    | I/O pack application data structure CRC changed                                         |
| 351          | I/O pack App Periodic thread [ ] timing overrun                 | An I/O pack application thread over/under run                                           |
| 353          | Sys Config Shmem CRC mismatch                                   | Config Shmem CRC changed                                                                |

## TVBA Vibration Input

### Functional Description

The Vibration Input (TVBA) terminal board acts as a signal interface board for the Mark\* VIe I/O pack PVIB. In the Mark VI system, the VVIB board works with TVIB.

The TVBA provides a direct interface to seismic (velocity), Proximitors<sup>®</sup>, Velomitors<sup>®</sup>, and accelerometer-type probes. The terminal board provides signal suppression and electromagnetic interface (EMI) protection for each input signal. Signals are also connected to a pull-up bias to allow open circuit detection.

The signals are passed on to the Mark VIe I/O packs through a 37-pin connector. The TVBA can be used for either simplex or TMR applications. TMR applications fan the signal to three I/O packs.

The TVBA contains buffered outputs to additional connectors beyond the standard 37-pin connection. This feature allows, special 9 and 25 pin connectors to feed the Bently Nevada<sup>\*</sup> 3500 monitoring system. A bayonet nut connection (BNC) connection for each channel is also included with this feature, to feed other third party monitoring equipment.

Mark VIe systems do not use the traditional RKPS power supply. Power is obtained from sourced +28 V power supplies and there is no external source for -28 V. The TVBA must maintain the same functionality as the Mark VI TVIB. For this reason, the TVBA has three removable daughterboards to convert +28 to -28. These boards, WNPS (negative power supply) are the source for all negative power used by the TVBA.

### Mark VI Systems

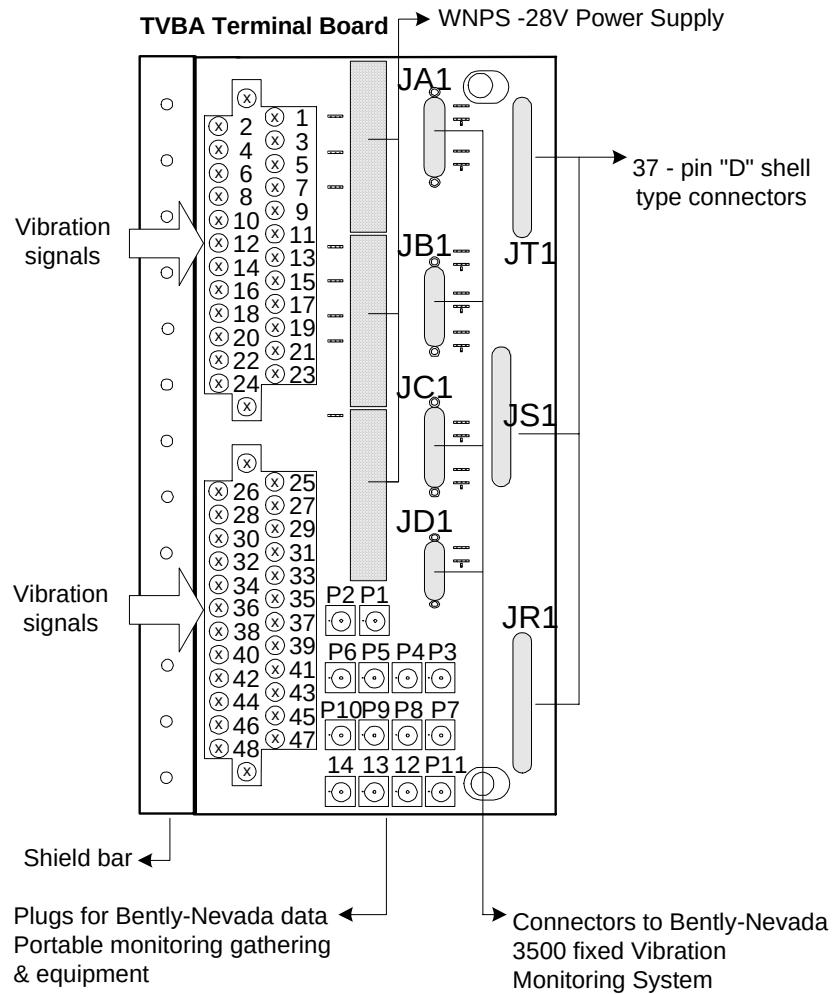
In the Mark VI system, the VVIB board works with TVIB. Simplex and TMR systems are supported. One or two TVIBs can be connected to the VVIB. In TMR systems, TVIB is cabled to three VVIB boards.

Refer to *GEI-100561 VVIB Vibration Monitor Board* for board revision compatibility.

## Mark VIe Systems

In the Mark VIe system, the PVIB I/O pack works with the TVBA. Simplex and TMR systems are supported. In TMR systems, three PVIB packs plug into the TVBA.

Refer to *GEI-100588 PVIB Vibration Monitor Pack* for board revision compatibility.



TVBA Vibration Terminal Board

## ***Installation***

The TVBA accepts 14 sensor inputs that are wired directly to two I/O terminal blocks. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination attachment point is located adjacent to each terminal block.

Input Channels 1 through 8:

- Support Proximity sensors, Seismics, Accelerometers (channel 1, 2, 3 only), and Velometers
- Current-limited -24 V power supply per channel
- JPxA jumper for configuring the open circuit check support and 3 mA constant current feed for Velometers
- JPxB configures the JA1 and JB1 outputs for the Bently Nevada 3500 rack
- JPxC configures PR0xL as Open for true differential input or connects PR0xL to PCOM for a -24 V return.

Input Channels 9 through 12:

- Support Proximity sensors only
- Current-limited -24 V power supply per channel
- No jumper configuration

Input Channel 13:

- Support Proximity sensors or Keyphasor<sup>®</sup> proximity sensors
- Current-limited -24 V power supply per channel
- No jumper configurations

-28 V power supply board, WNPS:

- Converts +28 V from PVIB to -28 V used by the current-limited -24 V outputs
- One WNPS per PVIB
- Independent +28 V inputs and common -28 V bus for all three WNPSs



### Customer Terminal Points

| Signal Name | Pin # | Description                                                                    |
|-------------|-------|--------------------------------------------------------------------------------|
| N24V01      | 1     | -24V power supply output feed for input #1                                     |
| PR01H       | 2     | Input #1 signal high side                                                      |
| PR01L       | 3     | Input #1 signal low side                                                       |
| N24V02      | 4     | -24V power supply output feed for input #2                                     |
| PR02H       | 5     | Input #2 signal high side                                                      |
| PR02L       | 6     | Input #2 signal low side                                                       |
| N24V03      | 7     | -24V power supply output feed for input #3                                     |
| PR03H       | 8     | Input #3 signal high side                                                      |
| PR03L       | 9     | Input #3 signal low side                                                       |
| N24V04      | 10    | -24V power supply output feed for input #4                                     |
| PR04H       | 11    | Input #4 signal high side                                                      |
| PR04L       | 12    | Input #4 signal low side                                                       |
| N24V05      | 13    | -24V power supply output feed for input #5                                     |
| PR05H       | 14    | Input #5 signal high side                                                      |
| PR05L       | 15    | Input #5 signal low side                                                       |
| N24V06      | 16    | -24V power supply output feed for input #6                                     |
| PR06H       | 17    | Input #6 signal high side                                                      |
| PR06L       | 18    | Input #6 signal low side                                                       |
| N24V07      | 19    | -24V power supply output feed for input #7                                     |
| PR07H       | 20    | Input #7 signal high side                                                      |
| PR07L       | 21    | Input #7 signal low side                                                       |
| N24V08      | 22    | -24V power supply output feed for input #8                                     |
| PR08H       | 23    | Input #8 signal high side                                                      |
| PR08L       | 24    | Input #8 signal low side                                                       |
| N24V09      | 25    | -24V power supply output feed for input #9                                     |
| PR09H       | 26    | Input #9 signal high side                                                      |
| PR09L       | 27    | Input #9 signal low side                                                       |
| N24V10      | 28    | -24V power supply output feed for input #10                                    |
| PR10H       | 29    | Input #10 signal high side                                                     |
| PR10L       | 30    | Input #10 signal low side                                                      |
| N24V11      | 31    | -24V power supply output feed for input #11                                    |
| PR11H       | 32    | Input #11 signal high side                                                     |
| PR11L       | 33    | Input #11 signal low side                                                      |
| N24V12      | 34    | -24V power supply output feed for input #12                                    |
| PR12H       | 35    | Input #12 signal high side                                                     |
| PR12L       | 36    | Input #12 signal low side                                                      |
| N24V12      | 37    | -24V power supply output feed for input #13                                    |
| PR12H       | 38    | Input #13 signal high side                                                     |
| PR12L       | 39    | Input #13 signal low side                                                      |
| PCOM        | 40    | -24V power supply output feed for input #14 (used only with Bently monitoring) |
| SIG9        | 41    | Input #14 signal high side (used only with Bently monitoring)                  |
| P24V9       | 42    | Input #14 signal low side (used only with Bently monitoring)                   |
| NC          | 48-48 | Unused                                                                         |

## Operation

The TVBA supports 14 sensor connections:

- Eight Vibration or position (ckts 1 through 8)
- Four Position only (ckts 9 through 12)
- One Reference probe (Keyphasor) or position, (ckts 13)
- One Reference probe (Keyphasor) or position, (ckt 14) (for Bently Nevada 3500 interface only)

### Keyphasor Inputs

**Vibration Inputs** accommodate the following transducers:

- Proximator
- Seismic
- Velometer
- Accelerometers (first three inputs on PVIB only)

Vibration signal is superimposed upon a dc bias voltage to make up the defined input voltage range from table 1.

- Add a -11 V dc,  $\pm 5\%$ , bias to the B/N buffered signal

When configured for seismic transducer:

- Add a negative bias to the input for open circuit detection
- Open the PRxxL signal to allow a true differential reading and meet common mode rejection requirements

The open circuit reading for the gap voltage (dc component) has the following value:

- Prox, Accel, Velometer more positive than -1.0 V dc
- Seismic more negative than -15 V dc

**Position Inputs** open circuit reading for the gap voltage (dc component) has a value more positive than -1.0 V dc.

**Phasor Inputs** open circuit reading for the gap voltage (dc component) has a value more positive than -1.0 V dc.

### Probe Power Supplies

Each channel provides a -24 V power supply. The supply is capable of producing a maximum of 12 mA. The supply is current limited to meet Class 1, Div. 2 requirements.

Output: -24.5 V (-23 to -26)

I<sub>out</sub>: 12 mA maximum

## **Buffered Outputs**

Each channel provides additional outputs other than the standard 37-pin connection. The signal output is a buffered version of the monitored signal. Each channel is output on a BNC connector. Each channel is also output through a 25-pin (Vib/Position) or 9-pin (Keyphasor) connector designed to interface with the Bently Nevada 3500 monitoring system. Requirements on the buffers are as follows:

- Amplitude accuracy 0.1%
- Add a -11 V dc,  $\pm 5\%$ , bias on seismic signals
- Sink 3 mA when interfacing with a Velomitors
- Unity-gain buffered output drives an impedance of 1500  $\Omega$ , capacitive up to 1000pF, with less than 10% overshoot.
- The buffered outputs drive both DB25, DB9, and BNC coaxial connectors in parallel. Both the center pin and the shell of the BNC are resistively isolated from the DB connectors. The isolation is sufficient that the DB connector's voltage remains within spec if the BNC connector is shorted.

## **WNPS Power Supply Daughterboard**

Three redundant external power supplies provide the power for the TVBA. If one power supply goes down, the offline power supply can be replaced without bringing down the terminal board. To maintain this feature, the TVBA has three removable daughterboards to provide +28 to -28 V power converters. The daughterboards can be removed while the TVBA is online by disconnecting the I/O pack power (R, S, or T), and removing the WNPS. The daughterboards must be mounted to meet all vibration and seismic standards.

The WNPS uses the corresponding channel (R, S, or T) 28 V bus to manufacture the required power for the vibration probes and on any board chips requiring power. A monitor feed for each -28 V supply should be fed back to the I/O pack for monitoring. The TVBA combines three -28 sources using diodes from the daughterboards to create the TVBA N28 bus. A TVBA configured with the TMR daughterboards provide enough current to supply 14 Proximitors at 18 mA, 14 buffered outputs at 12 mA, with one channel shorted at approximately 200 mA for a total of 540 mA without failure. Current sharing by the supplies make this condition possible. A TVBA with a single WNPS is not expected to handle this condition.

Electrical Characteristic:

Input: 28 V  $\pm 5\%$   
Output: -28 V  $\pm 5\%$   
Output Ripple: 1% of dc value  
I<sub>out</sub>: 400 mA maximum



## ***Specifications***

| <b>Requirement</b>                                                                   | <b>Limits</b>                                             |
|--------------------------------------------------------------------------------------|-----------------------------------------------------------|
| <b>Vibration Input Options</b>                                                       |                                                           |
| Number of channels supporting vibration probes (Proximitors, Seismic, or Velomitors) | 8                                                         |
| Number of channels with selectable pull up of $\pm 28$ , or constant current.        | 8                                                         |
| Number of channels with PRxxL Open/Pcom jumper (Seismic support)                     | 8                                                         |
| Number of buffered outputs with selectable bias (Seismic support)                    | 8                                                         |
| <b>Buffered Outputs</b>                                                              |                                                           |
| Number of N24 outputs                                                                | 14                                                        |
| N24 voltage                                                                          | -24.5 normal<br>(-23 to -26) V dc                         |
| N24 maximum current                                                                  | 12 mA                                                     |
| <b>Power Supply</b>                                                                  |                                                           |
| Number of buffered outputs                                                           | 14                                                        |
| Amplitude accuracy                                                                   | $\pm 0.1\%$                                               |
| Amplitude accuracy at DB connectors with BNC shorted                                 | $\pm 0.1\%$                                               |
| Ability to drive load                                                                | Min. 1500 $\Omega$ ,<br>Max 1000 pF<br>w/ < 10% overshoot |
| <b>WNPS</b>                                                                          |                                                           |
| N28 voltage                                                                          | 28 normal<br>(-26.6 to -29.4) V dc                        |
| N28 ripple                                                                           | 280 mV pk (1%)                                            |
| N28 maximum current                                                                  | 400 mA                                                    |

## ***Diagnostics***

Diagnostic tests are made on the terminal board as follows:

- The board provides the open circuit detection for each vibration input. The I/O processor creates a diagnostic alarm (fault) if any one of the inputs has an out-of-range voltage.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

## ***Configuration***

Jumper settings for TVBA as follows:

Jumpers J1A through J8A

- Seismic (S) N28 high-impedance bias for open-circuit protection
- Prox or Accel (P, A) P28 high-impedance bias for open-circuit protection
- Velomitor (V) 3 mA constant current N24 voltage source select

Jumpers J1B through J8B

- Prox, Velomitor or Accel (P, V, A) bypass dc blocking capacitor for BN outputs
- Seismic (S) select dc block capacitor for BN outputs

Jumpers J1C through J8C

- PCOM provides N28 return path for power supply
- OPEN no N28 return path through terminal board

All other configuration is for PVIB is done from the toolbox. For the location of these jumpers, refer to the installation diagram.

# ***Power Distribution Modules***

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## ***PDM Power Distribution Modules***

### ***Functional Description***

The Power Distribution Modules (PDM) are designed specifically for the Mark\* VIe system. The PDM uses individual boards to accept and condition primary control power inputs of 125 V dc, 24 V dc, and 115/230 V ac for use in redundant combinations. Applied power is distributed to system terminal boards for use in field circuits and converted to 28 V dc for operation of the Mark VIe I/O packs. The term PDM is used as a name for all of the individual pieces forming the power distribution for a system. The PDM is divided into two different categories:

Core distribution circuits are a portion of the PDM serving as the primary power management for a cabinet or series of cabinets. Input power from one or more sources is received by a corresponding module or board. The power is distributed to terminal boards and one or more bulk power supplies producing 28 V dc power to operate the control electronics. The 28 V power is monitored and distributed by one or more 28 V output boards.

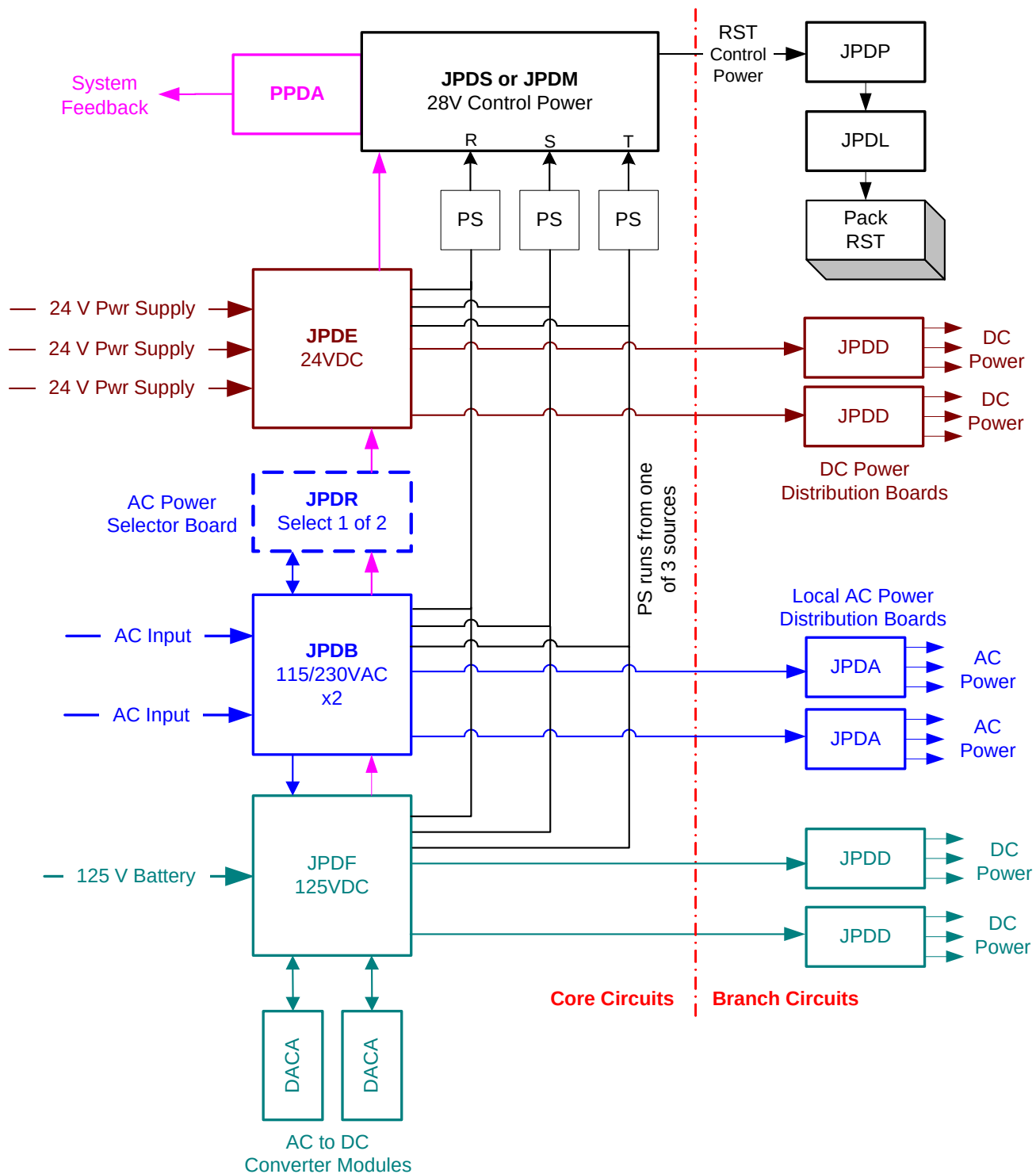
Ac input power is received by a JPDB module. JPDB accepts two independent ac sources. Dc input power is managed by JPDE (24 V/48 V) and JPDE (125 V).

The 28 V dc control power output board (JPDS or JPDM) hosts a PPDA I/O pack providing system feedback. Ribbon cables can daisy chain other core boards in the system to the board holding the PPDA I/O pack. The PPDA produces system feedback signals for all power bus voltages, branch circuit status, ground fault detection, and bulk power supply health. Complete monitoring and system feedback sets this power system apart from conventional methods of power distribution.

Bulk power supplies are considered a part of the core PDM system.

Branch circuit boards split the power output from the PDM core components into individual ac and dc circuits for use in the cabinets. Branch circuits do not connect to the PPDA I/O pack for system feedback. Elements receiving power from the branch circuits provide their own power status feedback signals to the control system. Branch circuit elements are usually single circuit boards rather than modules.

The following figure shows all of the possible elements of the PDM.



Power Distribution Module (PDM) Basic Layout

# Operation

## Core Components

Core components of the PDM receive primary control power inputs of 125 V dc, 24 V dc, and 115/230 V ac for use in redundant combinations. These components are identified as:

- **IS2020JPDB** ac module – The JPDB module consists of a sheet metal structure containing two sets of input line filters and an IS200JPDB circuit board. Power input from two separate ac sources passes through the line filters to the JPDB board. The board provides output for bulk 28 V dc control power supplies, terminal boards, and other loads. There are two versions of the IS200JPDB board: IS2020JPDBG2 has provisions for the connection of an external ac selector module and IS2020JPDBG1 omits this feature. The JPDB board uses ribbon cable connections for system feedback through PPDA including both ac bus voltages and individual branch circuit feedback.
- **IS2020JPDF** 125 V dc module – The JPDF module consists of a sheet metal structure containing a dc circuit breaker, input filter, series diode, current limiting resistors, and an IS200JPDF circuit board. Power from a 125 V dc battery feeds through the circuit breaker, filter, and diode to the JPDF board. The board also has connections for two DACA modules providing ac input/125 V dc output. When one or both DACA modules are used, the ac is provided by a wire harness between JPDB and JPDF. The result is a module that could accept power from a battery and / or one or two ac sources creating a highly reliable dc supply. The IS200JPDF board distributes dc power to bulk dc: dc supplies, terminal boards, and other loads. Two special output circuits, with series current limiting resistors, are provided for specific applications. The JPDF board uses ribbon cable connections for system feedback through PPDA including dc bus voltage, ground fault detection, and individual branch circuit status.
- **IS200JPDE** 24/48 V dc input board – The JPDE board mounts on a sheet metal structure. Power input is accepted from a battery and two dc power supplies. It could be provided with an optional dc circuit breaker and filter when using a battery power source. The JPDE board distributes the dc power to terminal boards and other loads. In small systems, JPDE could be used between a battery and 150 W dc power supplies. The JPDE board uses ribbon cable connections for system feedback through PPDA including dc bus voltage, ground fault detection, and individual branch circuit status.
- **IS200JPDS** 28 V dc control power output board – The JPDS board mounts on a sheet metal structure. Provisions are made supporting a PPDA I/O pack mounted on the JPDS circuit board. The JPDS circuit board contains three independent 28 V dc power buses with one bulk power supply input for each bus. Barrier screw terminals connect the power buses when a single bus with multiple supplies is desired. Output circuits from JPDS do not contain fuses with the exception of three auxiliary circuits. The JPDS board design depends on the current limit of the attached power supplies for branch circuit protection. The JPDS board uses ribbon cable connections for system feedback through PPDA including dc bus voltage, power supply status contact feedback, and auxiliary circuit status.
- **IS200JPDM** 28 V dc control power output board – JPDM is similar to JPDS except it has fewer output connectors and includes branch circuit fuses. JPDM is used for systems requiring 28 V dc supplies with current limit exceeding branch circuit capability. This includes systems that use two or more 500 W systems connected together forming a redundant control power source.

- **IS220PPDA I/O pack** – The power diagnostic pack mounts on either a JPDS or a JPDM board. Ribbon cables are used to daisy chain other core boards to the board hosting the PPDA. The pack can identify connected core boards and pass feedback signals to one or two IONet connections. PPDA has numerous indicator LEDs providing visual power distribution system status.

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**Note** PPDA does not take direct protective actions. It only reports information to the system controllers where corrective action can be programmed.

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- **DACA** ac to dc conversion module – This module takes incoming ac power and converts it to 125 V dc. It is used in conjunction with or in place of 125 V battery power. DACA provides capacitive energy storage for power-dip ride through when required.
- **PS** control power supplies – There are six different control power supplies used on the Mark VIe. There are two power supply ratings; 150 W and 500 W for voltage inputs of 24 V dc, 125 V dc, and 115/230 V ac.

### **Status Feedback**

The Mark VIe Controller uses a PPDA I/O pack for system feedback. The core JPDx boards can function without a working connection to the PPDA making it a non-critical element of the system. There are no provisions for PPDA redundancy without using a fully redundant set of JPDx boards. The PPDA pack provides timely information supporting system maintenance. PPDA provides five analog signal inputs with an electronic ID for each connected core PDM component. PPDA checks the ID lines to determine what boards are attached and then populates the corresponding signal space values. PPDA also operates local indicator lamps showing system status.

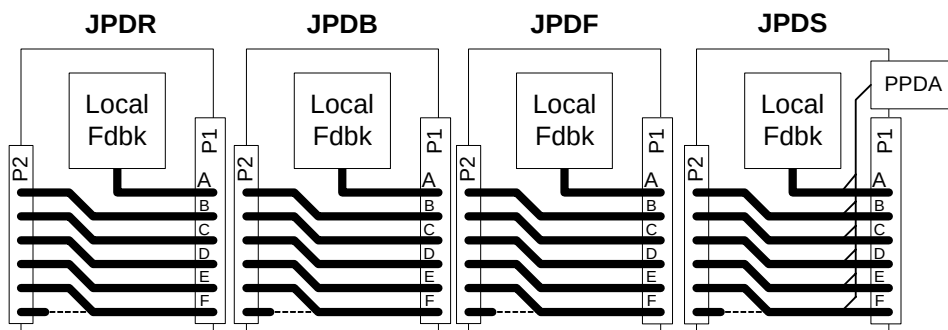
### **Branch Circuit Boards**

Branch circuit boards JPDP, JPDL, JPDA, and JPDD provide additional distribution of dc/ac power for output of the core PDM elements. These boards are not connected to the PPDA feedback cable. Branch circuit boards are identified as:

- **IS200JPDP** – The local power distribution board (JPDP) receives R, S, and T power from the 28 V control power board (JPDS or JPDM) and distributes it to the local pack power distribution board (JPDL). JPDP contains no fuses or indicators.
- **IS200JPDL** – The JPDL board provides two control power I/O pack power output connectors for each of the R, S, and T power sources. JPDL can be connected in series with other JPDL boards providing power to a vertical column of terminal boards and their associated I/O packs. Each output is protected with a self-resetting fuse that is coordinated with the wire size the pack connectors can accept.
- **IS200JPDD** – The dc power distribution board (JPDD) board is used to distribute a single dc power output into multiple loads. It can be used with a single input of 24 V, 48 V, or 125 V dc. Each load has a switch for maintenance purposes and fuses with a local indicator light. JPDDG1A has 15 A fuses for wire protection. JPDDG3A has empty fuse holders accepting a ¼ in x 1- ¼ in fuse.
- **IS200JPDA** – The JPDA board is used to distribute a single ac power output into multiple loads. This board has four switched ac outputs. Each load has a switch, for maintenance purposes, and a fuse on the line side with LEDs for each load. JPDAG1A has 15 A fuses for wire protection. JPDAG3A has empty fuse holders accepting a ¼ in x 1- ¼ in fuse.
- **IS200JGND** – JGND is used with terminal boards when field wire grounding is kept separate from the terminal board ground.

## Signal Routing

The PPDA I/O pack is mounted to either a JPDS or JPDM board. Additional boards are connected using 50-pin ribbon cable jumpers that are wired pin 1 to pin 1. Each board contributes one feedback group to PPDA. This connection passes through up to five previous boards. The following drawing show this hookup.

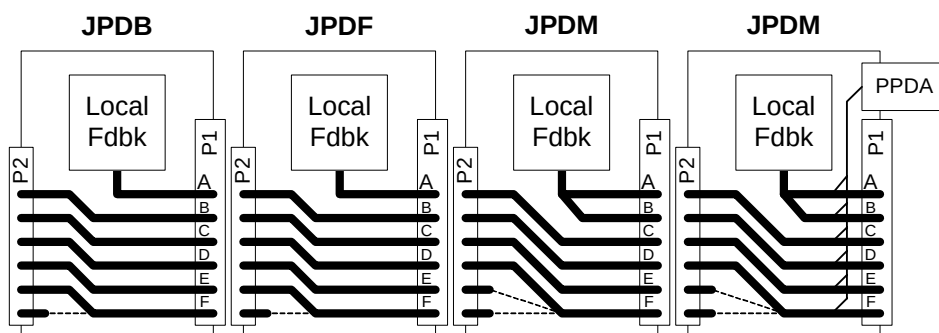


*PPDA Basic Hookup Diagram*

In the above figure, feedback groups are shown as bold lines and connectors P1 and P2 of each board are shown. From right to left, the JPDS board hosts the PPDA I/O pack and hookups are as follows:

- Local feedback from JDPS is on signal group A
- Feedback from JPDF is on signal group B
- Feedback from JPDB is on signal group C
- Feedback from JPDR is on signal group D
- An Additional board would use signal group E

JPDM uses two sets of feedback signals due to the large number of feedback lines from that board. JDPM does support the use of two boards. The arrangement would look like the following:



*PPDA Wiring Using Two JPDM Boards*

## ***PPDA Configuration Values***

The PPDA I/O pack's configuration values set it to operate with the desired PDM boards. Control System ToolboxST\* provides the correct options for the version of PDM hardware in use in a given system. A brief summary of the types of configurations encountered follows:

- PPDA: The I/O pack needs to know what PDM boards are in the diagnostic daisy chain.
- JPDS / JPDM: The PPDA needs to know if P28R, S, and T can be present in a system. If it is indicated that one is not present, the low voltage diagnostics for that power bus can be turned off.
- JPDE: The 24 V bus magnitude and centering tolerance can be configured, and the diagnostic associated with switched branch circuit fuse status can be turned on or off.
- JPDE: The 125 V bus magnitude and centering tolerance can be configured, and the diagnostic associated with switched branch circuit fuse status can be turned on or off.
- JPDB: The nominal voltage magnitude is selected, the magnitude tolerance specified, and a correction factor for neutral voltage is provided for each of the two ac buses. Each of the switched branch circuit fuse status can be turned on or off.
- JPDR: The expected voltage magnitude is specified.

## ***Valid PDM Core Card Combinations***

PPDA can receive feedback from as many as six connected core PDM components. The following rules apply when cabling components into a PPDA:

- JPDS or JPDM is selected as the power distribution board that hosts a PPDA I/O pack.
- A maximum of six boards can be used with a single PPDA I/O pack. A JPDM board counts as two boards due to the large number of PPDA feedback signals used. The following table shows valid combinations for either JPDS or JPDM as green. Combinations that are only valid for JPDS are shown in yellow.
- Either JPDM or JPDS can be used. The two board types cannot be mixed in a system. A maximum of two of any given board type can be used.
- Source selector JPDR for ac must be used with the JPDB board.



The following table uses single columns to show either JPDS or JPDM. It shows a list of all possible combinations of cards with a maximum of two each. The first column is always shown populated.

*JPDS/JPDM Core Card Combinations*

| JPDS1<br>JPDM1<br>P28 | JPDS2<br>JPDM2<br>P28 | JPDE1<br>24 V<br>dc | JPDE2<br>24 V dc | JPDF1<br>125 V<br>dc | JPDF2<br>125 V<br>dc | JPDB1<br>ac | JPDB<br>2<br>ac | JPDR1<br>Src<br>Select | JPDR2<br>Src<br>Select |
|-----------------------|-----------------------|---------------------|------------------|----------------------|----------------------|-------------|-----------------|------------------------|------------------------|
| 1                     | 0                     | 0                   | 0                | 0                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 0                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 0                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 1                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 1                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 1                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 1                    | 1                    | 0           | 0               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 0                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 0                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 0                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 1                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 1                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 1                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 1                    | 1                    | 1           | 0               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 0                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 0                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 0                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 1                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 1                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 1                    | 1           | 1               | 0                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 0                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 0                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 0                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 1                   | 1                | 1                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 1                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 1                    | 1           | 0               | 1                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 0                    | 0                    | 1           | 1               | 1                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 0                    | 0                    | 1           | 1               | 1                      | 1                      |
| 1                     | 0                     | 1                   | 0                | 0                    | 0                    | 1           | 1               | 1                      | 0                      |
| 1                     | 0                     | 1                   | 0                | 0                    | 0                    | 1           | 1               | 1                      | 1                      |

| JPDS1<br>JPDM1<br>P28 | JPDS2<br>JPDM2<br>P28 | JPDE1<br>24 V<br>dc | JPDE2<br>24 V dc | JPDF1<br>125 V<br>dc | JPDF2<br>125 V<br>dc | JPDB1<br>ac | JPDB<br>2<br>ac | JPDR1<br>Src<br>Select | JPDR2<br>Src<br>Select |
|-----------------------|-----------------------|---------------------|------------------|----------------------|----------------------|-------------|-----------------|------------------------|------------------------|
| 1                     | 0                     | 1                   | 1                | 0                    | 0                    | 1           | 1               | 1                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 0                    | 1           | 1               | 1                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 0                    | 1           | 1               | 1                      | 1                      |
| 1                     | 0                     | 1                   | 0                | 1                    | 0                    | 1           | 1               | 1                      | 0                      |
| 1                     | 0                     | 0                   | 0                | 1                    | 1                    | 1           | 1               | 1                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 0                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 0                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 1                | 0                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 1                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 1                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 1                | 1                    | 0                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 1                    | 1                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 1                    | 1                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 1                | 1                    | 1                    | 0           | 0               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 0                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 0                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 1                | 0                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 1                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 1                    | 1                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 0                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 1                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 1                | 1                    | 0                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 1                    | 1                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 1                    | 1                    | 1           | 0               | 0                      | 0                      |
| 1                     | 1                     | 1                   | 1                | 0                    | 0                    | 1           | 1               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 1                    | 1                    | 1           | 1               | 0                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 0                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 1                     | 1                   | 0                | 0                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 1                     | 1                   | 1                | 0                    | 0                    | 1           | 0               | 1                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 1                    | 1                    | 1           | 0               | 1                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 0                    | 0                    | 1           | 1               | 1                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 0                    | 0                    | 1           | 1               | 1                      | 1                      |
| 1                     | 1                     | 1                   | 0                | 0                    | 0                    | 1           | 1               | 1                      | 0                      |
| 1                     | 1                     | 0                   | 0                | 1                    | 0                    | 1           | 1               | 1                      | 0                      |

## Circuit Protection

Circuit protection for the Mark VIe PDM include:

- Fault current protection limits the current to the capability of the system components.
- Branch circuit system feedback
- Ground fault protection in floating systems
- Redundant applications, if possible

## Connector Conventions

Systems using multiple power applications create the possibility of making wrong connections such as applying the wrong power to a load or interconnecting power buses. The Mark VIe PDM use specific connector conventions to eliminate this problem. The specific connectors are shown in the following table.

| Power from main PDM                        | Connector                           |
|--------------------------------------------|-------------------------------------|
| 125 V dc from JPDP to JPDD                 | 2 pin Mate-N-Lok                    |
| 125/230 V ac from JPDB to JPDA             | 3 pin Mate-N-Lok                    |
| 24 V dc from JPDE to JPDD                  | 4 pin in-line Mate-N-Lok            |
| 28 V dc control power from JPDS to JPDP    | 3x2 pin Mate-N-Lok                  |
| 28 V dc control power from JPDP to JPDL    | 5 pin in-line Mate-N-Lok            |
| Dc power supply output to JPDE, JPDS, JPDM | 3x3 pin Mate-N-Lok (power + status) |
| DACA connection to JPDP                    | 3x4 pin Mate-N-Lok                  |

Exceptions to the above table exist. An effort has been made to clearly mark the connector function on the boards. For example: a 5-pin in-line Mate-N-Lok<sup>®</sup> connector is used on JPDB and JPDP to pass ac power between the boards. Both connectors are clearly marked for their intended use and are physically placed to ensure proper connection.

Existing terminal boards designs present the greatest risk of being improperly connected. These boards use a three position Mate-N-Lok for power input regardless of whether it is an ac or dc connection. The existing boards also have two parallel connectors to allow power daisy-chain wiring within a panel.

The JPDP board can detect an improper wiring connection, such as applying ac power on a floating 125 V dc battery buss, and report it through the PPDA I/O pack.

## P28 Control Power Protection

JPDS/JPDM control power characteristics are as follows:

- The negative side of JPDS/JPDM is grounded at every I/O pack to FE. This grounding aids in the conduction of transient noise to earth.

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**Note** It is impossible to float the JPDM/JPDS power supply.

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- The supply voltage provided by the approved power sources can be  $28\text{ V} \pm 5\%$ .
- The I/O packs are designed with minimal power disturbance ride-through capability.
- Bulk energy storage is provided by the control power supplies.
- Control power cannot be used for tasks such as contact wetting for field inputs. External connections are controlled and filtered by the terminal board/pack combination.
- JPDS/JPDM, JPDP, and JPDL support independent control power systems for each controller and associated I/O pack. A redundant control system maintains a separation of control power ensuring system reliability.

### System Monitoring

Incoming power is monitored as follows:

- Incoming power is monitored by every I/O pack. An alarm will signal any incoming power that falls below  $28\text{ V} - 5\%$ . The control can continue to operate depressed voltage in most cases.
- Depressed voltage effects are dependent on the connected field devices. Determining the voltage required for failure can only be accomplished if the entire system is analyzed.
- A second alarm will be sounded if the control power falls below  $16\text{ V}$ . The  $16\text{ V}$  alarm can help isolate the source of failure during further analysis.
- JPDS and JPDM provide voltage monitoring for R, S, and T power buses.
- Mark VIe power supplies include a dry contact status feedback circuit. This contact will be closed when the power supply is operating normally and will open if it is not. The controller reads the status signals as a Boolean value. These values are necessary when multiple supplies are connected in parallel for redundant systems. They provide the only way to determine when one supply is not functioning correctly.
- The JDPM monitors all fused output branch circuits and indicates a fuse failure.
- Both JDPM and JPDS power supplies provide four test points, with current limited by  $10\text{ k}\Omega$  series resistors, used to connect external test equipment.

### Branch Circuit Protection

Branch circuit protection, starting at the terminal board and working back toward the power source is shown below:

- Terminal boards supplying output power to field devices provide individual branch circuit protection using a small three terminal regulator. The regulator includes a thermal shut down feature that responds quickly to any overload condition.
- All I/O packs have a fast acting solid-state circuit breaker at the power input point. This breaker ensures that any problem with a connected terminal board can not propagate to other system components.

- The pack circuit breaker is used as a soft-start feature for the pack. Hot-plugging the 28 V dc power into a pack results in a very gradual turn-on of the pack. This ensures no other system component can be affected.
- The JPDL includes a self-recovering fuse coordinated with the wiring to the pack. This device limits current in the event of a short circuit or failure of the protection within the pack. The fuse can protect the wiring, but it doesn't always act fast enough to prevent disturbance of other packs on the same power bus.
- The JPDP board uses only copper conductors and connections. It can carry the same circuits as the JPDL.
- The JPDM board uses individual branch circuit fuses in the positive output to the JPDP board. These fuses can protect wiring and circuit boards between JPDM and the protection on JPDL. Auxiliary outputs are protected by self-resetting devices rated at 1.4 A.
- The JPDS board does not use fuses like JPDM. The board is rated for Class I Division 2 (potentially explosive atmosphere) and the use of fuses is not desired. The JPDS wiring is protected by self-restarting devices rate at 1.4 A.
- Each power supply has current limiting on the output. Current limiting is sufficient to protect the wiring through the JPDP and JPDL when a single 500 W power supply or up to three 150 W supplies are wired together to power a system bus. When JPDS is used for distribution, this current limit protects branch circuit wiring. Multiple supplies, exceeding 500 W, use JPDM or JPDS with external fuses.

Distribution component design provides control power branch circuit protection. Specific areas that require monitoring are:

- Supply current limit protecting wiring cannot exceed 500 W. The maximum allowable wire size must be used in the Mate-N-Lok connectors.
- Maximum allowable wire sizes must also include wiring to Ethernet switches and control rack power supplies.
- Parallel supplies, yielding a total capability greater than 500 W, must use JPDM or JPDS with external branch circuit protection.

### ***Ac Power Protection***

Specific characteristics of ac power distribution components are:

- Ac power distribution components are designed for using a grounded neutral supply.
- By design, the JPDB board can not be damaged if the line and neutral connections are reversed.
- JPDB and JPDA boards have fuses in the line side only. Reversing the connections between line and neutral can eliminate series circuit protection.
- An ac power source, similar to US domestic applications could have a 230 V ac winding with the grounded neutral on a center tap. In this case, both neutral connections of the JPDB must be wired.
- The connectors on JPDB are arranged on the board edge in an AC1, AC2, AC1, and AC2 pattern. A wire harness can be created to pick up line connections from two adjacent connectors yielding 230 V ac from dual 115 V ac feeds. This arrangement puts a fuse on both line connections for proper circuit protection.

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**Note** The preceding items do not apply when using a 230 V ac input power source with a grounded neutral connection.

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- JPDB is designed with sufficient voltage clearance between the two ac inputs, such as two 208 V or 230 V, from a three-phase source and cannot cause voltage clearance problems.
- JPDB uses input filtering to provide a *transients known and controlled* voltage environment for the circuit board. These filters are part of JPDB module and no additional filters are required.
- JPDB delivers 10 A per ac input to both the DACA feed JAF1 and protected branch circuit outputs for a total of 20 A per ac input.

## System Monitoring

System monitoring is provided as follows:

- JPDB provides ac voltage magnitude feedback for both input circuits.
- JPDB provides on/off value system feedback for all switched or fused branch circuit outputs.
- JPDA provides a visible LED indicator all four switched/fused branch circuit outputs.
- JPDB provides test point outputs from the two ac inputs for connection of external test equipment. Each test point has a series current limiting 100 k $\Omega$  resistor.

## Branch Circuit Protection

Branch circuit protection for ac power distribution components is as follows:

- JPDB inputs must be protected by a maximum 30 A circuit breaker with normal trip characteristics.

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**Note** Using a slow trip circuit breaker or one rated more than 30 A could cause damage to the board in the event the breaker must be opened.

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- JPDB is designed for a grounded neutral ac connection. Voltage clearances on the neutral circuit are the same as the line inputs. This prevents board damage from incorrect connections.
- JPDB includes a 5 A fuse on the line side of each output. This fuse was selected to coordinate with the output switch maximum current rating.
- Two un-switched fused outputs have a 5 A fuse while the board artwork and connector list a 10 A fuse. This was done so all the board fuses have the same value and reduces errors of replacing fuses with the wrong sizes.
- JPDB is designed to deliver 10 A continuously to two DACA modules connected through JAC1 and JPDA.
- JPDA has four switched ac outputs with a fuse in the line side. The board is powered from JPDB through one of the 5 A fused branch circuits. The switch used on JPDA is the same as used on JPDB. Both switches use a 5 A fuse. JPDA uses 15 A fuses. JPDA is connected to JPDB and any occurring fault can open the fuse on JPDB first. JPDB is connected to the system through PPDA. JPDAG2A has empty fuse holders accepting 5 mm X 20 mm fuses and features a black fuse holder cap. JPDAG3A has empty fuse holders accepting a ¼ in x 1-¼ in fuse. Both JPDAG2A and JPDAG3A allow the use of a JPDA board with custom fuse rating that is coordinated with a load device limited to less than 5 A.
- JPDA should be used with a power feed of a fused 5 A JPDB feed. JPDA fusing applications should be addressed if other power feeds are used.

## 125 V dc Power Protection

Characteristics for using a 125 V dc battery as a power source for the PDM are as follows:

- A nominal 125 V dc battery is used as a dc power source for the Mark VIe PDM system.
- The maximum voltage the dc battery can feed to the system is 145 V dc.

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**Note** The Mark VIe control can go into over-voltage shutdown should the supplied dc power exceed 145 V dc.

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- The 125 V dc input to 28 V dc output supply, used to supply control electronics, can function down to 70 V dc. Field devices must be reviewed on an individual basis.
- The 125 V dc battery must be floating with respect to earth. This arrangement eliminates a hard ground on both the positive and negative bus. A single ground fault applied to the system can pass current defined by the centering resistor value and dc bus magnitude. Shift in bus voltage, in respect to earth, can then be detected to indicate a ground fault.
- Ground fault current in a floating battery system is defined by the fixed centering resistance value. The Mark VIe system is classified as Non-hazardous Live because the ground fault current is below dangerous levels. JPDP is designed so that when using provided centering resistors (JP1 in place), the resulting ground resistance is within Non-hazardous Live requirements. When two JPDP boards are wired in parallel for greater current capacity or branch circuit count, only one set of centering resistors should be used.
- When JPDP centering resistors are not used and voltage centering is provided by other means, calculation of centering impedance must allow for the fixed voltage attenuators, 1,500,000  $\Omega$  resistors, between the positive bus and earth and the negative bus and earth on JPDP. The resistors provide attenuated bus voltage feedback to PPDA. All other branch circuit feedback signals use isolating devices that do not a path to ground.
- JPDP applications with dc input filtering yield a transients known and controlled environment for the board voltage clearance class. Required filtering is provided as part of the JPDP module. No additional input filters are needed.
- The DACA module is designed to coordinate power delivery with a 125 V dc battery. One or two DACA modules, powered by a reliable ac power source, could be used to provide backup power in the event of battery failure.

## System Monitoring

Monitoring for the 125 V dc power systems is as follows:

- JPDP provides voltage magnitude feedback through PPDA for positive and negative dc voltage with respect to earth. The difference between the two signals equals the bus magnitude. The difference between the two bus voltage magnitudes could be used to detect a system ground fault in a floating system.
- JPDP includes additional circuitry on the bus voltage feedback that detects ac current. PPDA can issue an alarm when a JPDP board shows more 30 V ac on the dc bus.
- JPDP has a visible LED for each switched and fused branch circuit outlet.

## Branch Circuit Protection

Branch circuit protection for the 125 V dc power system is as follows:

- The JPDF module has a 30 A dc circuit breaker in the input power feed to ensure correct input power protection.
- JPDF has 5 A fuses on both sides of the J1 R, S, and T output branch circuits. The fuses coordinate with the rating of the switches provided with these outputs.
- JPDF has 5 A fuses on both sides of the J7 X, Y, and Z output branch circuits. The fuses coordinate with the rating of the switches provided with these outputs. There is a series 1  $\Omega$  resistor in each leg, with the same rating as the switches, provided with these outputs.
- JPDF has 12 A fuses on both sides of the J8A and J8B output branch circuits. The connector uses 12 AWG wire.
- JPDF has 3 A fuses on both sides of the J12 output branch circuit. The J12 circuit has 22  $\Omega$  resistors in series limiting fault current to [ ] V dc/44 A.
- JPDD has six switched and fused dc outputs. The board is powered by JPDF. The fuses on JPDD are 15 A. The board is fed by a 5 A branch circuit from JPDF. JPDD is visible to the system through PPDA. A fault on the JPDF circuit cannot result in opening the 15 A fuses on JPDD. JPDDG2A has empty fuse holders accepting 5 mm x 20 mm fuses with a black fuse holder cap. JPDDG3A has empty fuse accepting ¼ in x 1- ¼ in fuses with a gray fuse holder cap.

## 24/48 V dc Power Protection

Characteristics of the 24 V dc power protection system is as follows:

- 24 V dc power distribution is a utility system using a 24 V nominal dc battery. A typical ac system uses one or more dc power supplies for contact wetting and relay outputs.
- The maximum allowable battery voltage is 36 V dc. The Mark VIe controller can initiate over-voltage shutdown when the battery output voltage exceeds the allowable limit.
- The 24 V dc input to 28 V dc output powers Mark VIe control electronics.
- The 24 V dc battery has no hard ground on either the positive or the negative dc bus. A high resistance from the positive and negative dc is applied to earth in order to center the bus on earth. A single ground fault applied to this system can pass current defined by centering resistor value and dc bus magnitude. The shift in voltage, with respect to earth, can be detected and signal the presence of a ground fault.
- The JPDE board provides centering resistors selected by using J1. In the event the battery has external centering resistors on the battery bus, J1 could be eliminated to avoid higher ground fault currents.
- The JPDE board is designed application using dc input filtering. Additional input filters are not needed.

Characteristics of the 48 V dc power protection system is as follows:

- The JPDE can be configured to operate correctly using 48 V dc input power for power distribution.



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# **PPDA Power Distribution System Feedback**

## **Functional Description**

The Power Distribution System Feedback (PPDA) pack accepts inputs from up to six different power distribution boards. It conditions the board feedback signals and provides a dual redundant Ethernet interface to the controllers. PPDA feedback is structured to be plug and play uses electronic IDs to determine the power distribution boards wired into it. This information is then used to populate the IONet output providing correct feedback from connected boards.

## **Compatibility**

The PPDA I/O pack is hosted by the JPDS or JPDM 28 V dc Control Power boards on the Mark\* VIe Modular Power Distribution (PDM) system. It is compatible with the feedback signals created by JPDB, JPDE, and JPDE.

## **Installation**

The PPDA I/O pack mounts on either a JPDS or JPDM 28 V dc control power terminal board.

### **➤ To install the PPDA pack**

- 1** Securely mount the desired terminal board.
- 2** Directly plug one PPDA I/O pack for simplex or three PPDA I/O packs for TMR into the terminal board connectors.
- 3** Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4** Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5** Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6** Configure the I/O pack as necessary.
- 7** Connect ribbon cables from connector J2 on JPDS or JPDM to daisy chain other core boards feeding information to PPDA.

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**Note** Additional PDM feedback signals may be brought into the PPDA I/O pack through the P2 connector on the host board. The P1 connector is never used on a board that hosts the PPDA I/O pack, PPDA must always be at the end of the feedback cable daisy chain.

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## Diagnostics

The PPDA performs the following self-diagnostic tests:

- A power-up self-test including checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition card, and processor card confirming the hardware set matches, followed by a check confirming the application code loaded from flash memory is correct for the hardware set
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the A/D converter circuits.
- Details of the individual diagnostics are available from the ToolboxST\* application. The diagnostic signals are individually latched, and then reset with the RESET\_DIA signal if they go healthy.

## Configuration

| Variable       | Description                      | Direction   | Type |
|----------------|----------------------------------|-------------|------|
| L3DIAG_PPDA_R  | I/O Diagnostic Indication        | Input       | BOOL |
| L3DIAG_PPDA_S  | I/O Diagnostic Indication        | Input       | BOOL |
| L3DIAG_PPDA_T  | I/O Diagnostic Indication        | Input       | BOOL |
| LINK_OK_PPDA_R | I/O Link Okay Indication         | Input       | BOOL |
| LINK_OK_PPDA_S | I/O Link Okay Indication         | Input       | BOOL |
| LINK_OK_PPDA_T | I/O Link Okay Indication         | Input       | BOOL |
| ATTN_PPDA_R    | I/O Attention Indication         | Input       | BOOL |
| ATTN_PPDA_S    | I/O Attention Indication         | Input       | BOOL |
| ATTN_PPDA_T    | I/O Attention Indication         | Input       | BOOL |
| PS18V_PPDA_R   | I/O 18 V Power Supply Indication | Input       | BOOL |
| PS18V_PPDA_S   | I/O 18 V Power Supply Indication | Input       | BOOL |
| PS18V_PPDA_T   | I/O 18 V Power Supply Indication | Input       | BOOL |
| PS28V_PPDA_R   | I/O 28 V Power Supply Indication | Input       | BOOL |
| PS28V_PPDA_S   | I/O 28 V Power Supply Indication | Input       | BOOL |
| PS28V_PPDA_T   | I/O 28 V Power Supply Indication | Input       | BOOL |
| IOPackTmpr_R   | I/O pack Temperature (deg F)     | AnalogInput | REAL |
| IOPackTmpr_S   | I/O pack Temperature (deg F)     | AnalogInput | REAL |
| IOPackTmpr_T   | I/O pack Temperature (deg F)     | AnalogInput | REAL |
| Pbus_R_LED     | Pbus R is in Regulation          | Input       | BOOL |
| Pbus_S_LED     | Pbus S is in Regulation          | Input       | BOOL |
| Pbus_T_LED     | Pbus T is in Regulation          | Input       | BOOL |
| Src_R_LED      | All R Pbus Sources OK            | Input       | BOOL |
| Src_S_LED      | All S Pbus Sources OK            | Input       | BOOL |
| Src_T_LED      | All T Pbus Sources OK            | Input       | BOOL |
| Aux_LED        | Aux 28 outputs OK                | Input       | BOOL |
| Batt_125V_LED  | 125 V battery volts OK           | Input       | BOOL |
| Batt_125G_LED  | 125 V battery floating           | Input       | BOOL |
| JPDD_125D_LED  | 125 V JPDD feeds OK              | Input       | BOOL |
| Pbus_125P_LED  | 125 V Pbus feeds OK              | Input       | BOOL |
| Batt_24V_LED   | 24 V battery volts OK            | Input       | BOOL |

| Variable        | Description                     | Direction   | Type |
|-----------------|---------------------------------|-------------|------|
| Batt_24G_LED    | 24 V battery floating           | Input       | BOOL |
| JPDD_24D_LED    | 24 V JPDD feeds OK              | Input       | BOOL |
| Pbus_24P_LED    | 24 V Pbus feeds OK              | Input       | BOOL |
| AC_Input1_LED   | Ac input 1 OK                   | Input       | BOOL |
| AC_Input2_LED   | Ac input 2 OK                   | Input       | BOOL |
| AC_JPDA_LED     | Ac JPDA feeds OK                | Input       | BOOL |
| AC_Pbus_LED     | Ac Pbus feeds OK                | Input       | BOOL |
| JPDR_LED        | JPDR Src Select OK              | Input       | BOOL |
| Accelerometer_X | Vibration input, X-coordinate   | AnalogInput | REAL |
| Accelerometer_Y | Vibration input, Y-coordinate   | AnalogInput | REAL |
| App_1_LED       | Application driven              | Output      | BOOL |
| App_2_LED       | Application driven              | Output      | BOOL |
| App_3_LED       | Application driven              | Output      | BOOL |
| Fault_LED       | Fault Led - Application driven) | Output      | BOOL |

| Parameter  | Description                                   | Selections      |
|------------|-----------------------------------------------|-----------------|
| InFiltEnb1 | Enable inputs filtering for terminal board #1 | Disable, Enable |
| InFiltEnb2 | Enable inputs filtering for terminal board #2 | Disable, Enable |
| InFiltEnb3 |                                               | Disable, Enable |
| InFiltEnb4 |                                               | Disable, Enable |
| InFiltEnb5 |                                               | Disable, Enable |
| InFiltEnb6 |                                               | Disable, Enable |

## ***DS2020DACAG2 ac-dc Power Conversion***

### ***Functional Description***

The DS2020DACAG2 is a drop in replacement for the DS2020DACAG1. It is backward compatible in systems that used the previous version and it should be used as a replacement part for the previous model. The DACA converts 115/230 V ac input power into 125 V dc output power, and the output power rating is approximately 1000 W.

A DACA is used when the primary power source for a control system is 125 V dc with or without a battery. In addition to power conversion, DACA provides additional local energy storage to extend the ride-through time whenever the Mark VIe Control has a complete loss of control power.

The DS2020DACAG2 model has a higher power rating than the previous module. Also, this new model can be paralleled for greater output current, whereas paralleling was not recommended for the previous model. The DS2020DACAG2 is recommended for all new panel designs.

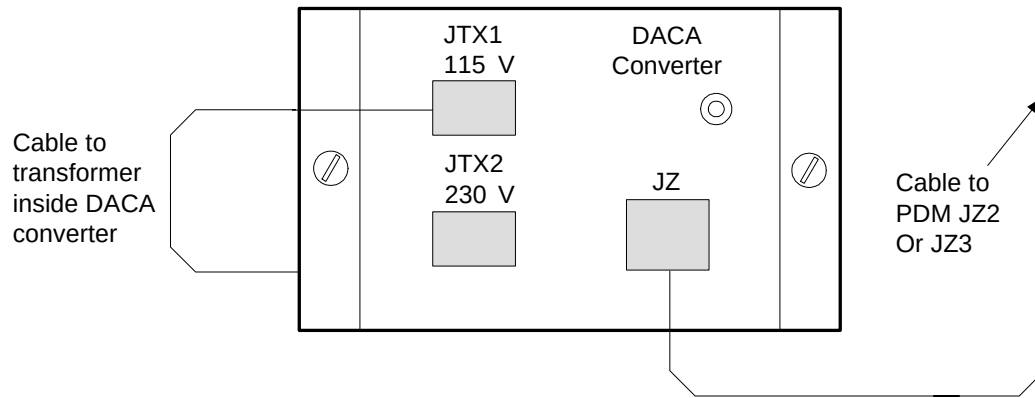
## Installation

The DACA module has four mounting holes in its base. Ac power input and dc output is through a single 12-position connector JZ that is wired into connector JZ2 or JZ3 of the PDM. Selection of 115 V ac or 230 V ac input is made by plugging the DACA internal cable into connector JTX1 for 115 V or JTX2 for 230 V.



**Ensure the proper voltage is selected before power is applied to the equipment.**

### Caution



*DACA Module Wiring*

### DACA Filter Capacitor Wear Out

The electrolytic capacitors in the DACA module wear out over time due to the ambient temperature of the environment where they are used. The following table shows the calculated life expectancy and recommended replacement schedule for the DACA modules.

*DACA Replacement Schedule*

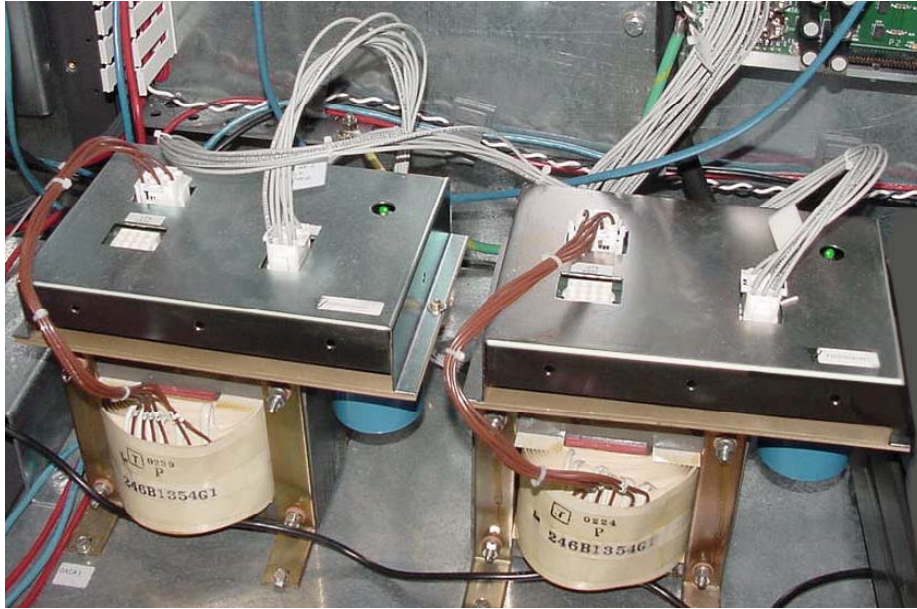
| Calculated Life Expectancy of DACA Capacitor | Recommended Replacement Schedule* |
|----------------------------------------------|-----------------------------------|
| At 20°C (68 °F) ambient                      | 100 years                         |
| At 45°C (113 °F) ambient                     | 20 years                          |
| At 65°C (149 °F) ambient                     | 5 years                           |

\*Due to wear out of Electrolytic Capacitor

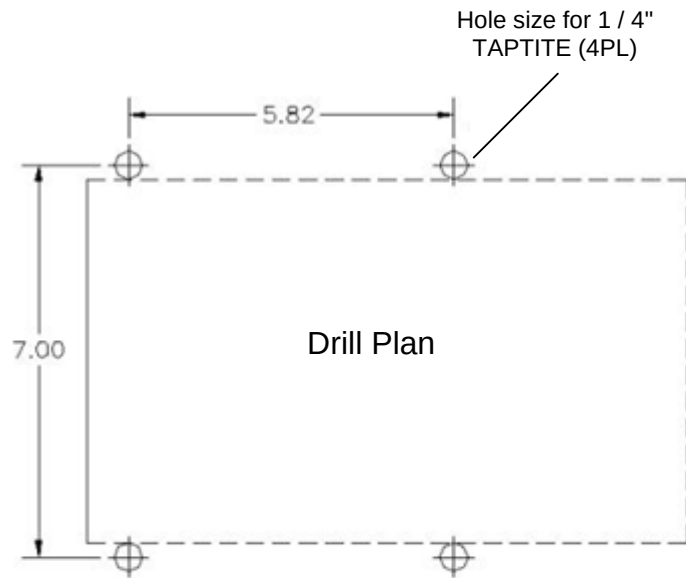
#### ➤ To replace a DACA power conversion module

- 1 Remove power from the DACA module. Allow 1 minute for the output voltage to discharge.
- 2 Remove the power input/output cable (JZ) on the right side of the module top.
- 3 Remove the four bolts securing the DACA module to the floor of the cabinet.
- 4 Remove the DACA module.
- 5 Make note of which receptacle the capacitor power plug is in. This is on the left side of the module top. JTX1 is for 115 V ac and JTX2 is for 230 V ac.
- 6 Ensure the capacitor power plug is in the same position as the one removed. JTX1 is for 115 V ac and JTX2 is for 230 V ac.
- 7 Place the new DACA module in the same position as the one removed.

- 8 Secure the DACA module to the cabinet floor with the four bolts removed from the previous module.
- 9 Install the power input/output plug (JZ) on the right side of the module top.
- 10 Restore power to the DACA module.



*DACA Power Conversion Modules*



Note: Keep out area is 8.65 in. x 13.9 in.

*DACA Mounting Pattern*

## Operation

DACA receives ac power through the cable harness that is plugged into connector JZ. DACA uses a full wave bridge rectifier and an output filter capacitor. If needed, the user must provide an input filter to attenuate harmonic currents injected into the incoming line.

*Single DACA Module, Maximum Output Current is 9.5 A dc*

| Input to DACA<br>V ac RMS | Input Current<br>at Max Load | Output Voltage<br>Load = 1 A dc | Output Voltage<br>Load = 9.5 A dc |
|---------------------------|------------------------------|---------------------------------|-----------------------------------|
| 115 V ac                  | 11 A                         | 119 V dc                        | 107 V dc                          |
| 230 V ac                  | 6 A                          |                                 |                                   |

The DACAG2 can be paralleled for greater output current. In parallel operation, current sharing between the two DACAs is critical. Uneven current sharing can cause one of the DACAs to operate beyond its output current rating.

*Two DACA Modules with Outputs Paralleled, Maximum Output Current is 16.5 A dc\**

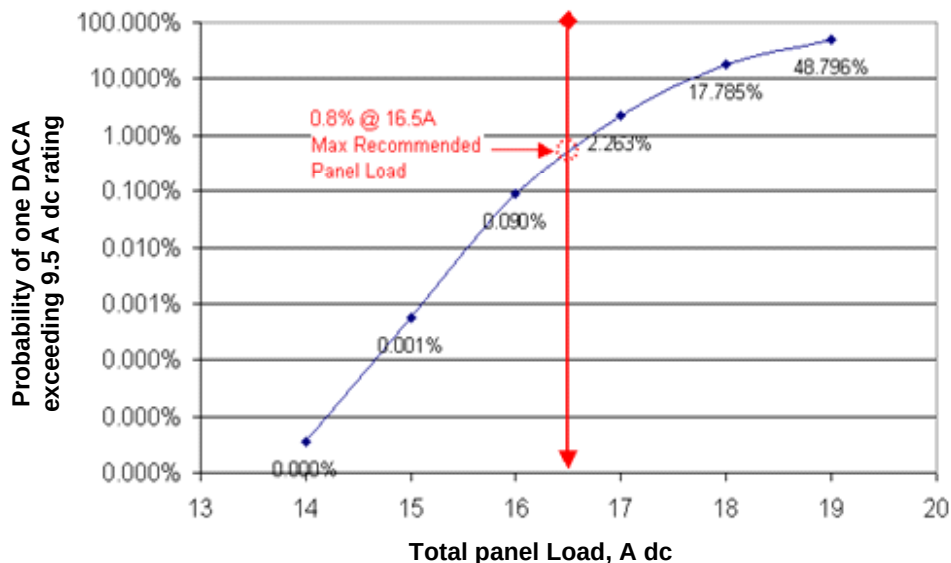
| Input to DACA<br>V ac RMS | Input Current<br>at Max Load | Output Voltage<br>Load = 1 A dc | Output Voltage<br>Load = 15 A dc |
|---------------------------|------------------------------|---------------------------------|----------------------------------|
| 115 V ac                  | 20 A                         | 120 V dc                        | 110 V dc                         |
| 230 V ac                  | 11 A                         |                                 |                                  |

\* The two paralleled DACAs must be connected to one ac voltage source for even output current sharing.

For proper implementation of parallel DACAs, the following must be observed:

- The DACAs must be connected to the same ac source to ensure equal input voltages to the DACAs.
- The maximum output current per DACA is derated for parallel operation. This derating accounts for variance in DACA open circuit voltages and variance in DACA output impedances. The following curve should be used. The maximum recommended total panel current is 16.5 A dc.

**Probability of overloading one DACA when two DACAs are paralleled; Plotted at various panel loads**



## ***Specifications***

| <b>Item</b>                                                                | <b>Specification</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |      |      |      |
|----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|
| Input Voltage                                                              | 105-132 V ac or 210-265 V ac, 47 to 63 Hz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |      |      |      |
| Output Voltage                                                             | 90 to 145 V dc with a load of 1 to 9.5 A<br>Over the full range of input voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |      |      |      |
| Output Current Rating                                                      | 9.5 A dc, -30 to 45°C (-22 to 113 °F)<br>Linearly derate to 7.5 A dc at 60°C (140 °F)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |      |      |      |
| Output Ripple Voltage                                                      | 4 V p-p                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |      |      |
| Discharge Rate                                                             | Nominal input of 115 or 230 V ac, no load, discharge to less than 50 V dc within 1 minute of removal of input power.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |      |      |      |
| Hold Up (time for output to discharge to 70 V dc with constant power load) | V in (V ac)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 105  | 115  | 132  |
|                                                                            | Initial Load (A dc)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 9.5  | 9.5  | 9.5  |
|                                                                            | Pout (W)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 882  | 974  | 1131 |
|                                                                            | Hold Up Time (ms)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 19.5 | 29.5 | 48.8 |
| Temperature                                                                | -30 to 60°C (-22 to +140 °F) free convection                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |      |      |      |
| Humidity                                                                   | 5 to 95%, non-condensing<br>UL 508C Safety Standard Industrial Control Equipment<br>CSA 22.2 No. 14 Industrial Control Equipment<br>EN 61010 Section 14.7.2 – Overload Tests<br>EN 61010 Section 14.7.1 – Short Circuit Test<br>EN 61000-4-2 Electrostatic Discharge Susceptibility<br>EN 61000-4-3 Radiated RF Immunity<br>EN 61000-4-4 Electrical Fast Transient Susceptibility<br>EN 61000 –4-5 Surge Immunity<br>EN61000-4-6 Conducted RF Immunity<br>EN 50082-2:1994 Generic Immunity Industrial Environment<br>ENV 55011:1991 - ISM equipment emissions<br>IEC 529 Intrusion Protection Codes/NEMA 1/IP 20 |      |      |      |

## ***Diagnostics***

No diagnostic features are provided on this module.

## ***Configuration***

Input voltage selection is made on DACA by plugging the captive cable harness into connector JTX1 for 115 V ac nominal input or connector JTX2 for 230 V ac nominal input.

# JPDA Local ac Power Distribution

## Functional Description

The Local ac Power Distribution (JPDA) board provides ac power distribution, power isolation, and branch circuit protection for each control or I/O function requiring ac power. Typical applications include ac relay and solenoid control power, ignition transformer excitation, and contact wetting. Each output includes a fuse, a switch for power isolation, and a lamp to indicate the presence of output voltage.

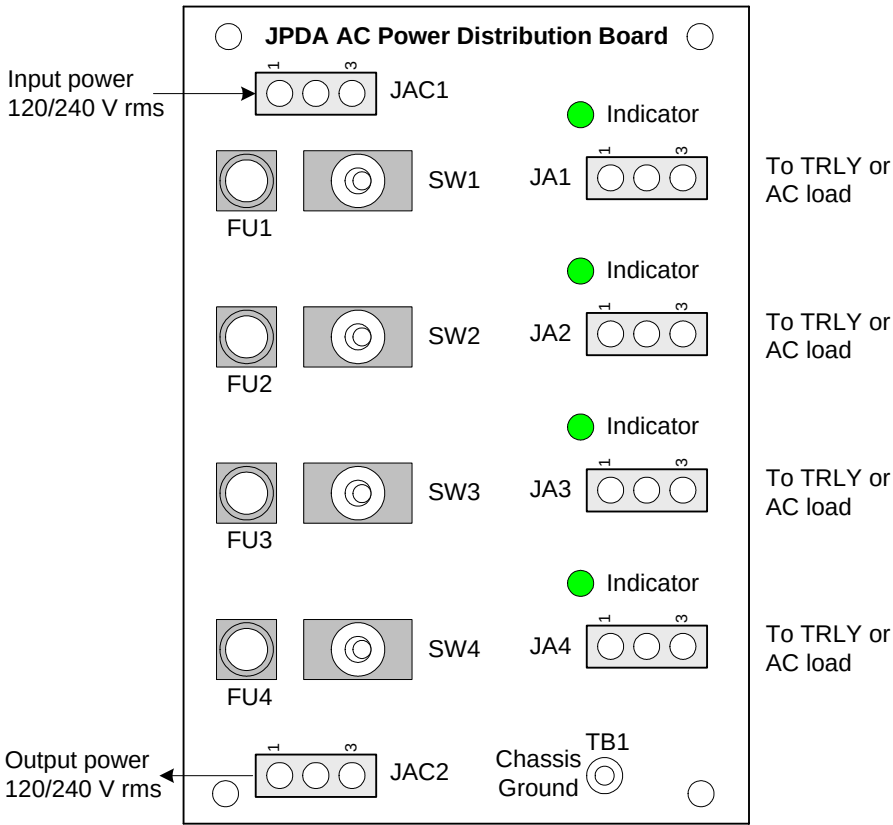
## Board Versions

| Terminal Board | Fusing                                                         |
|----------------|----------------------------------------------------------------|
| JPDAG1         | Each circuit provided with ¼ in x 1¼ in 15 A 250 V fuse        |
| JPDAG2         | Empty fuse holders with black caps accepting 5 x 20 mm fuses   |
| JPDAG3         | Empty fuse holders with grey caps accepting ¼ in x 1¼ in fuses |

JPDAG1 provides fuses that are coordinated with the rating of the system wiring and connectors. JPDAG2 and G3 are used when fuse ratings coordinated with a specific application are required. Two different fuse sizes are provided for to best accommodate local fuse preferences.

## Installation

JPDA mounts in a plastic holder, which fits on a vertical DIN-rail.



JPDA Cabling

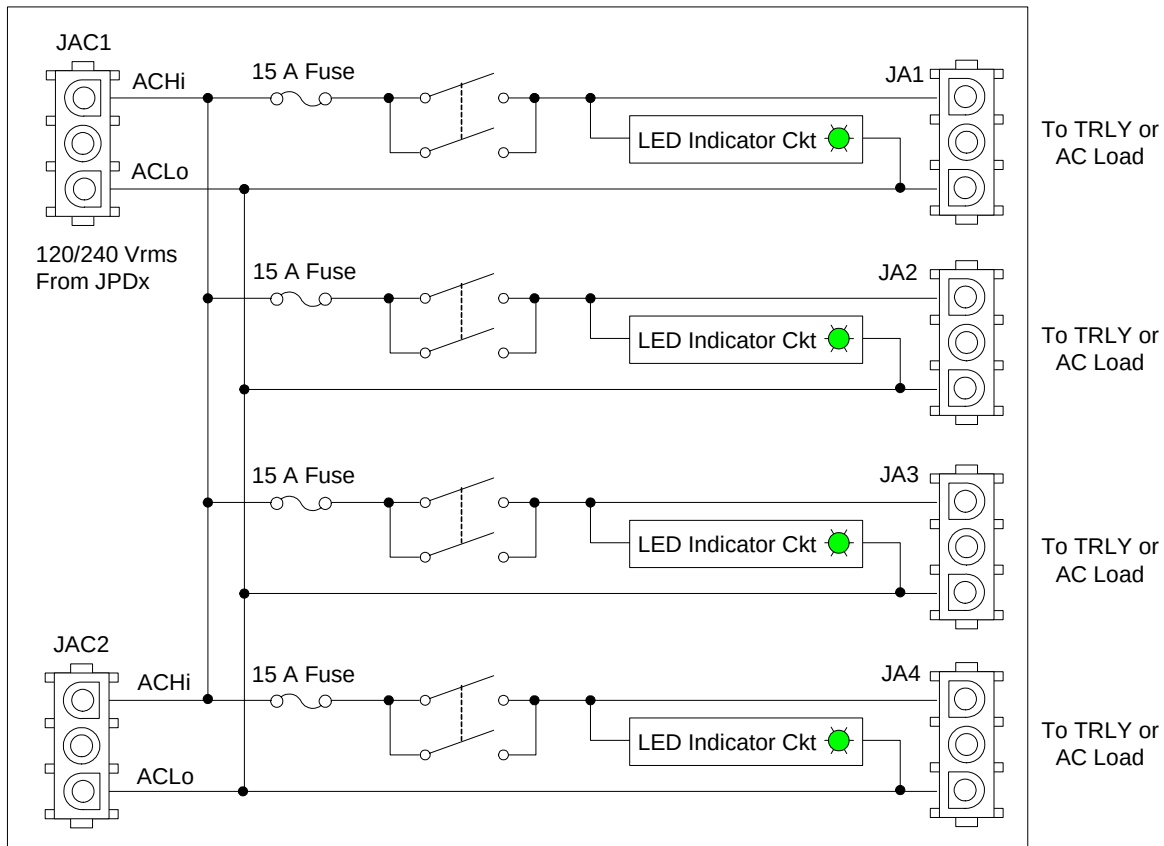


Power input and output cables have three-position Mate-N-Lok<sup>®</sup> connectors. For cable destinations, refer to the circuit diagram.

TB1 is the chassis ground connection. When installing the JPDA it is important to provide a ground lead from TB1 to the system PE. This creates a ground path for the metal switch bodies.

## Operation

The following figure shows how the 120/240 V rms power is distributed in JPDA, and how it reaches the TRLY board or ac load.



*JPDA Simplified Circuit Diagram*

## Inputs

Multiple JPDA boards receive power from a single JPDM Main Power Distribution Module. This power input is either 120 V rms or 240 V rms, 50/60 Hz.

Two 3-Pin Mate-N-Lok connectors are provided. One connector receives ac input power and the other can be used to distribute ac power to another JPDA board in daisy chain fashion. It is expected that the low or neutral side of the input power is grounded.

## Outputs

Four output circuits are provided with three-pin Mate-N-Lok connectors. Each output circuit includes branch circuit protection, and a pair of isolation contacts for the non-grounded line. There is also a green lamp to indicate the presence of voltage across the output terminals.

## Specifications

| Item         | Description                                                 |                              |
|--------------|-------------------------------------------------------------|------------------------------|
| Inputs       | One 3-pin connection for input power from JPDx              | 120 or 240 V rms, 15 A limit |
| Outputs      | Four 3-pin connections for TRLY and ac loads                | 120 or 240 V rms, fused 15 A |
|              | One 3-pin connection for output power to another JPDA board | 120 or 240 V rms             |
| Output fuses | Four fuses, one per output, Bussmann® ABC-15 A typical.     | 250 V, 15 A                  |
| Temperature  | -30 to +65°C (-22 to +149 °F)                               |                              |
| Board Size   | 15.875 cm high x 10.795 cm wide (6.25 in x 4.25 in)         |                              |
| Mounting     | DIN-rail, card carrier mounting                             |                              |
|              | Base mounted steel bracket, 4 holes                         |                              |

## Diagnostics

No diagnostic features are provided on this module.

## Configuration

There are no jumpers on JPDA. Check the position of the four output load switches.

It is possible to use other fuse ratings with this board to provide specific branch circuit ratings. A typical series of fuses that work with this board are the Bussmann ABC series of fuses with ratings from ¼ A through 15 A. Fuses above 15 A shall not be used with this board. If alternate fuse ratings are used, configuration of the board requires the insertion of the proper fuse in each branch circuit.

---

## JPDB ac Power Distribution

### Functional Description

The ac Power Distribution (JPDB) board conditions, monitors, and distributes ac power. The module contains two line filters and a IS200JPDB circuit board. The module features two separate ac distribution circuits, each rated for 20 A at 115 or 230 V ac. The input circuits should be wired in parallel to avoid PPDA alarms when a single source of ac power is provided.

For each circuit, one fused, and three fused and switched branch circuit outputs are provided. Connection to an optional JPDB 125 V dc distribution module is provided. The IS200JPDB includes passive monitoring circuits for both ac magnitudes as well as status feedback for all fused circuits. The monitoring circuits are on connector P1, compatible with cable connection to a board containing a power diagnostic PPDA I/O pack. IS200JPDB also has a P2 connector for pass-through of monitoring signals from other power distribution system cards.

Two JPDB modules could be cabled into a single PPDA I/O pack when needed.

IS2020JPDBG2 provides an additional connector when an ac source selector is required in a system. The connector intercepts the two ac sources supplied to JPDB and routes them to the JSS1 connector on the board edge. Output of the ac selector is then wired to JSS1 and conducted to the individual branch circuit outputs.

---

**Note** Circuit breakers are not provided as part of the basic IS2020JPDB module. Options exist to provide circuit breakers on a mounting plate that fastens to the JPDB sheet metal support. Please refer to job specific documentation for information regarding any circuit breakers attached to JPDB.

---

## ***Compatibility***

The IS2020JPDB is compatible with the feedback signal P1 / P2 connectors on JPDE, JPDE, JPDS, and JPDM leading to a PPDA I/O pack. Connector JAF2 is compatible with the ac input on the JPDE module of the same name.

## ***Installation***

The IS2020JPDB module is base-mounted vertically on a metal back base in a cabinet used by the PDM. A connection must be made between the IS2020JPDB sheet metal and the system Protective Earth.

Input power is applied to terminals AC1H (line) and AC1N (neutral) for the first ac circuit, and AC2H (line) and AC2N (neutral) for the second ac circuit. Both ac inputs are required to have grounded neutral connections. Output circuits are connected as documented for the system.

If the power distribution system includes a PPDA power diagnostic I/O pack, a 50-pin ribbon cable is required from JPDB connector P1 to the P2 connector on the board holding PPDA. It is permissible for this connection to pass through other core PDM boards using the P2 connector.

## ***Grounding***

Mark\* Vle systems divide ground into a protective earth (PE) and a functional earth (FE). The PE ground must be connected to an appropriate earth connection in accordance with all local standards. The minimum grounding must be capable of carrying 60 A for 60 seconds with no more than a 10 volt drop. The FE ground system must be bonded to the PE ground system at one point.

The JPDB is grounded through metal mounting supports fastened to the underlying sheet metal of a metal module. The ground is applied to the metal switch bodies on JPDB. Additionally, the ground is used as a local reference point when creating the feedback signals appearing on P2. The sheet metal of the module is insulated to the surface upon which it is mounted. This is done specifically to allow definition of the JPDB ground independent of the mounting surface. Typically, JPDB is mounted to a back base grounded to FE. JPDB would be located low in the cabinet and a separate ground wire from the JPDB module would be provided to PE. The minimum length of the ground wire is important to keep impedance low at radio frequencies, this allow the input line filters to function properly.

## ***Physical Arrangement***

When JPDB is used with an optional source, the selector should be positioned above the JPDB, thus allowing a short power connection between the two components using the JSS1 connector. When JPDB is used with a JPDP (125 V dc) board, the JAF1 connector provides ac power to JPDP. The best location for JPDP in this arrangement is below the JPDB, to minimize wiring lengths. The P1 and P2 ribbon cable headers on all of the JPDB boards are positioned, so the JPDS or JPDM holding the PPDA I/O pack is best located at the top of the board arrangement. This allows ribbon cables to flow from one card to the next, exiting the top, and entering the bottom of the next card until the PPDA host is reached. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

## ***Application Notes***

When JPDB is used with a single ac input, the two ac inputs should be wired in parallel to the source. All output branch circuits are now live and there can be no diagnostics generated. If only one ac input is used, a diagnostic for loss of ac on the un-switched branch circuit can appear.

## ***Operation***

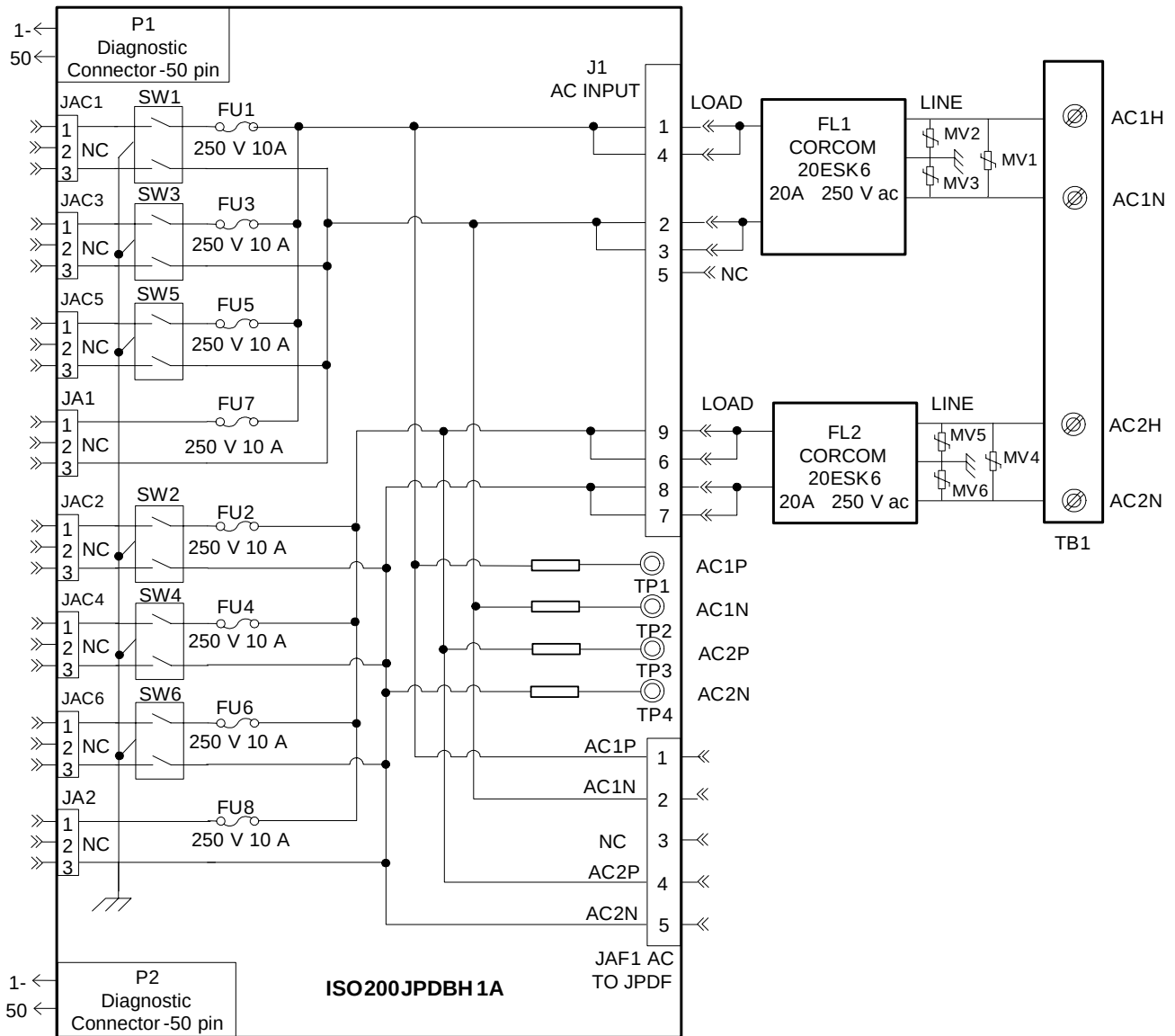
Two sources of ac power are wired to a terminal board on the right side of the JPDB module. The ac power goes to the ac line filter assemblies underneath the IS200JPDB circuit board. A wire harness connects the filter assemblies to the JPDB circuit board J1 connector.

The IS2020JPDBG01 module uses the IS200JPDBH1A circuit board. This board does not provide connection for an ac source selector and J1 ac power is wired directly to the output branch circuits.

The IS2020JPDBG02 module uses the IS200JPDBH2A circuit board. The board is designed for use with an ac source selector. It features the JSS1 connector mounted to the board. External filtered ac from connector J1 is fed to JSS1. The source selector output returns to the JSS1 to supply the branch circuit outputs.

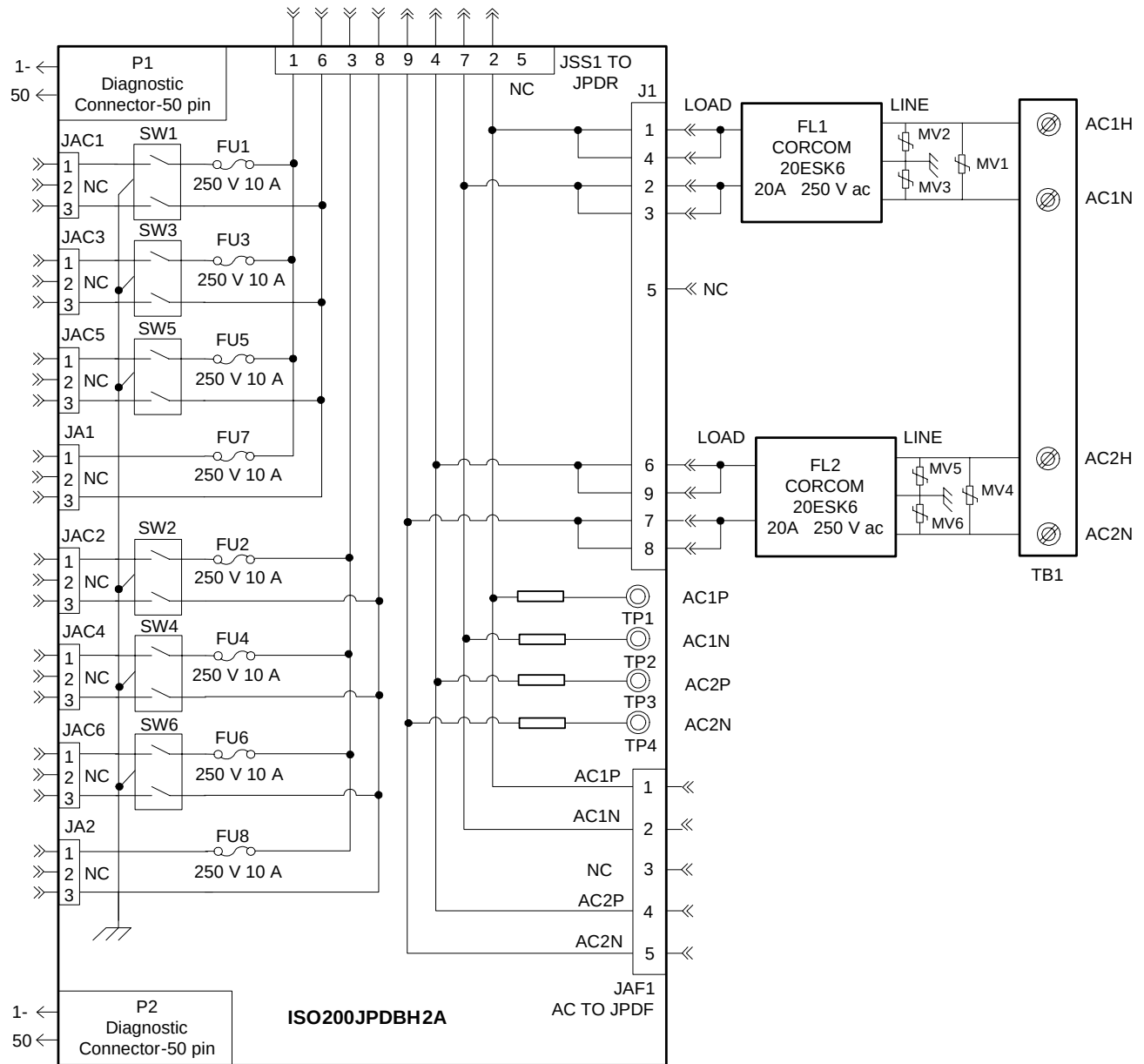
JAF1 feeds power directly from input connector J1 to an adjacent optional JPDP board to power two DACA power conversion modules. The DACA modules convert the ac power to 125 V dc to be used as an ac backup for systems using a 125 V dc battery.

The figure below shows the JPDBG01 module with the JPDBH1A circuit board.



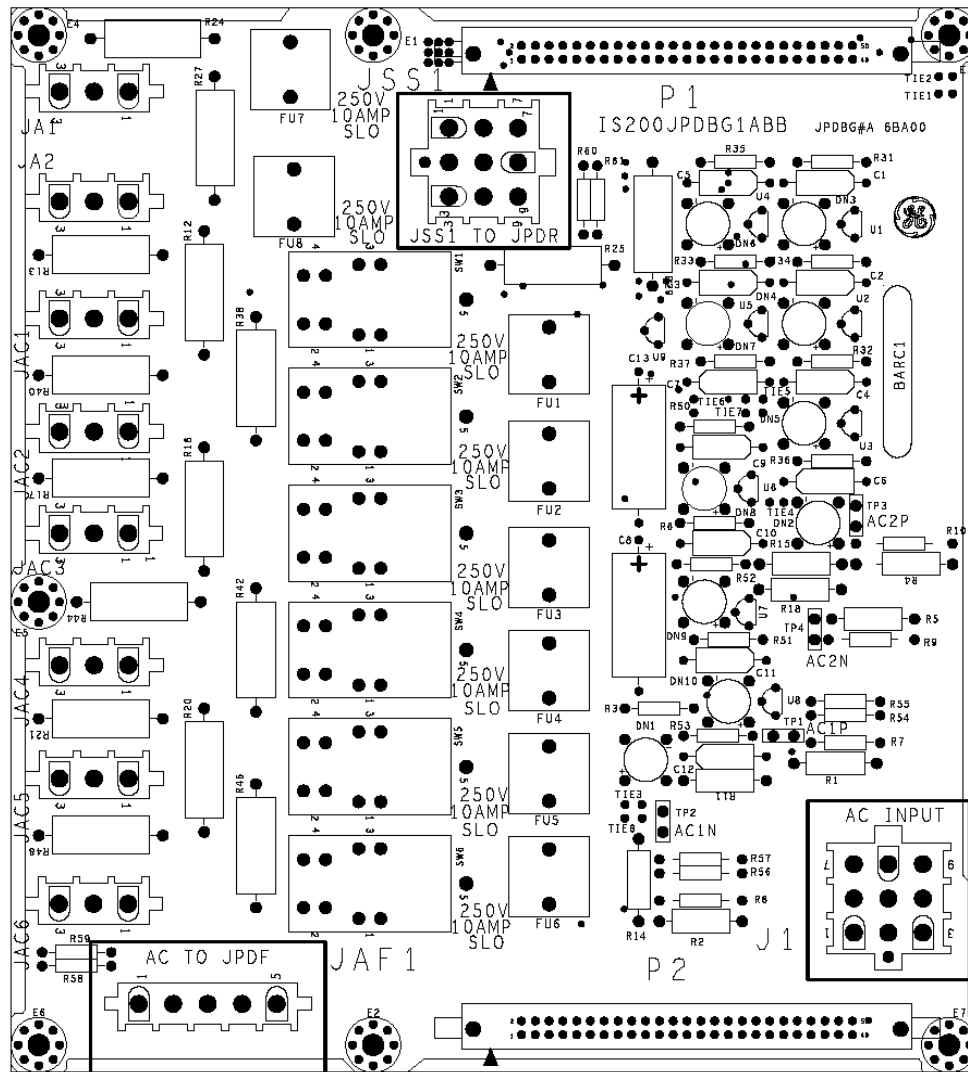
JPDB Module for Use without the JPDR Source Selector

The figure below shows the JPDBG02 modules with the JPDBH2A circuit board.



JPDB Module for Use with the JPDR Source Selector

The following figure shows the mechanical layout of the JPDB board.



JPDB Module Mechanical Layout

## I/O Characteristics

- A terminal strip (TB1) mounted with the JPDB module has two ac input screw terminal pairs. These terminals are rated at 20 A RMS. Branch circuit protection can be no larger than a 30 A circuit breaker. The rating for the ac circuits is 115/230 V ac, 20 A for each of the two circuits feeding JAF1. The circuits use a grounded neutral connection.
- A nine-position Mate-N-Lok<sup>®</sup> connector, J1, accepts power from line filters into the JPDB board. Dual pins are used for each connection point to support the current rating. J1 comes with a wire harness that is part of the module. Refer to previous wiring diagrams for proper hookup.
- A five-position Mate-N-Lok connector, JAF1, provides direct ac power output. This connector matches the one on the JPDBF board. Ac current passes through the JPDBF board providing ac to dc conversion using DACA modules.
- A nine-position Mate-N-Lok connector, JSS1, is included on the JPDBH2A board and provides a connection point for an external ac source selector. The JSSI connector is not used on the JPDBH1A board and there is no connection for a source selector.

- Two un-switched ac outputs, JA1 and JA2, are provided with each ac circuit using a three-pin Mate-N-Lok connector to feed optional JPDA branch circuit boards. The circuits are fused and rated at 10 A/250 V.
- Six switched and fused output connectors, JAC1 through JAC6, are provided with each using a three pin Mate-N-Lok connector. Fuses are rated at 10 A/250 V. Additionally these connectors could be used to feed ac/28 V dc power converters making I/O pack control power.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

## Specifications

| Item                                               | Description                                                                                                      |
|----------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| Board Rating                                       | 115/230 V ac either circuit<br>50/60 Hz<br>30 A circuit breaker protection                                       |
| Total ac circuit loading                           | 10 A on JAF1 AC1 plus 20 A total on JA1+JAC1+JAC3+JAC5<br>10 A on JAF1 AC2 plus 20 A total on JA2+JAC2+JAC4+JAC6 |
| Fuse for connectors JAC1-JAC6 and JA1-JA2: FU1-FU8 | 10 A on 250 V, Bussmann <sup>®</sup> MDA-10 typical                                                              |
| Module size                                        | 26.41 cm High x 21.33 cm Wide x 16 cm Deep (10.4 in. x 8.4 in. x 6.3 in.)                                        |
| Mounting                                           | Four mounting holes, #10 screws                                                                                  |

## Diagnostics

Diagnostic signals routed into PPDA through connector P1 include:

- An electronic ID identifying the board type, revision, and serial number
- Two 115/230 V ac analog feedbacks
- Six switched/fused ac supply indications yielding six Boolean values after PPDA decodes the signals
- Two fused ac supply indications yielding two Boolean values after PPDA decodes the signals
- A local ground signal for sensing analog signals

Additional core PDM board feedback passes through JPDB using the P2 connector. Test points with 100 k series resistors are provided to allow connection of testing equipment:

- TP1 is the AC1 line
- TP2 is the AC1 neutral line
- TP3 is the AC2 line
- TP4 is the AC2 neutral line

## Configuration

There are no jumpers or hardware settings on the board.



---

# JPDC Power Distribution Module

## Functional Description

The IS2020JPDC Power Distribution Module (JPDC) combines input and output functions from several previous designs to provide distribution of 125 V dc, 115/230 V ac, and 28 V dc to other boards within a turbine control system.

### Compatibility

JPDC can host a Power Distribution System Feedback (PPDA) pack used in the Mark\* VIe Power Distribution System. JPDC can also receive diagnostic feedback signals from other distribution boards and route these signals to the PPDA I/O pack as well.

The intent is that the PPDA I/O pack should be mounted on the JPDC module. Therefore, no provision is made to transmit diagnostic signals from JPDC to another distribution board.

## Installation

The JPDC module is typically mounted vertically with the 115/230 V ac input connector (JAC) at the bottom. It is attached with four screws using the mounting holes located at the top and bottom of the module base. Location within the control cabinet is not critical, however, distribution boards are usually mounted low in the cabinet to facilitate grounding. Refer to the section, Grounding.

The optional PPDA I/O pack is plugged into connector JA1. It is secured to the JPDC base using an angle bracket, held in place with nuts threaded onto studs, that are permanently attached to the base for that purpose.

Diagnostic feedback inputs from other distribution boards are routed to JPDC through a 50-pin ribbon cable attached to connector P2.

Input power connections include:

- Either one or two 125 V dc battery input connections through connectors JD1 and JD2
- 125 V dc DACA module connection made using connector JZ2
- 115 or 230 V ac input applied to connector JAC

Up to three separate 28 V dc sources can be made to connectors JR, JS, and JT respectively. The positive sides of these three inputs are isolated from each other and designated as 28PR, 28PS, and 28PT power busses. If only one 28 V dc input is used, the three power busses can be linked together if desired. Refer to the section, Operation.



### Attention

**To replace a JPDC, replace the entire module. Refer to the section, Module Replacement. Do not remove the board from its mounting plate.**

## Grounding

Mark VIe systems divide ground into a protective earth (PE) and a functional earth (FE). The PE ground must be connected to an appropriate earth connection in accordance with all local standards. The minimum grounding must be capable of carrying 60 A for 60 seconds with no more than a 10 volt drop. The FE ground system must be bonded to the PE ground system at one point.

The FE circuitry on the JPDC board is grounded through metal mounting supports fastened to the underlying sheet metal of the module. The FE ground is used as a local reference point when creating the feedback signals appearing on P2. Typically, the JPDC module is mounted to a back base grounded to FE, completing the path to ground.

The metal switch bodies on the JPDC are tied to PE circuitry on the board. Separate ground wires from the JPDC module, screw connections E5 and or E6 must be connected to the enclosure PE bus.

When input line filters are inserted in line with the JPDC, the filters should be located either on a PE grounded base or near the enclosure PE bus. When PE ground wires are run from the filters to the PE bus, minimum length of the ground wire is important to keep impedance low at radio frequencies, allowing the input line filters to function properly.

## Physical Arrangement

The IS2020JPDC module consists of a 6.75 x 19.0-inch IS200JPDC board, a diode assembly, and two resistors mounted on a steel base.

Voltage levels on the JPDC board increase from top to bottom with 28 V dc circuits on the top and left side, 125 V dc in the center and right side, and 115/230 V ac on the bottom.

## Operation

### Ac Power Distribution

An input of either 115 V ac or 230 V ac is supplied to JPDC through connector JAC. The maximum allowable current is 12.5 amps rms. It is expected that the low or neutral side of the input power is grounded. (Refer to the functional diagram)

Two ac outputs are provided. Both are protected by a 10 A time-delay fuse on the high side only (Pin 1 of each connector). The output at JAC1 is controlled by toggle switch SWAC1. The JAC2 output is not switched.

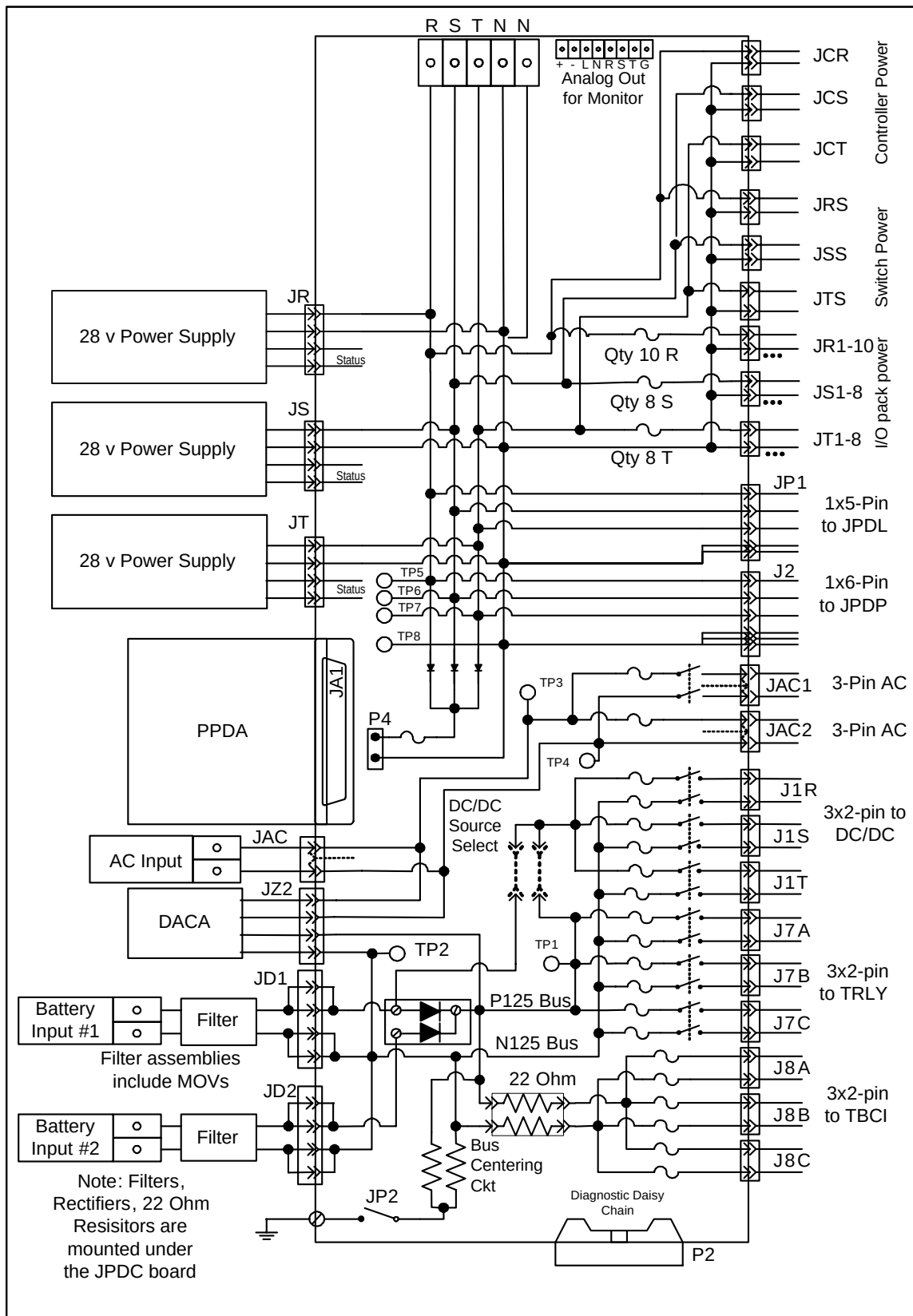
### 125 V Dc Power Distribution

JPDC can accept two battery inputs through connectors JD1 and JD2. Provision is also made for a third 125 V dc input from an ac/dc converter such as IS2020DACA through connector JZ2. Each input is typically routed through an external filter.

Input voltage range 90 – 145 V dc.

The two battery inputs are OR'ed together by diode module D1 and are OR'ed with 125 V dc from DACA by a diode on the DACA module. The OR'ed 125 V dc inputs combine on JPDC to form a 125 V dc bus labeled PDC. The return paths of the 125 V dc inputs are connected together and labeled NDC. Total 125 V dc current flow should not exceed 20 amps.

All three 125 V dc inputs are floating with respect to ground. When jumper JP2 is installed, each side of the 125 V dc bus is connected to FE ground through approximately 84 k ohms of resistance in order to provide a means of ground fault detection.



JPDC Functional Diagram

### Nine 125 V dc outputs are provided:

- Three outputs J1R, J1S, and J1T provide power to the inputs of three external 28 V dc power supplies which supply JPDC with 28 V dc power. These outputs are fuse-protected and controlled by toggle switches SW1R, SW1S, and SW1T.



#### **Caution**

**When SW1R, SW1S, and SW1T are switched OFF, wait at least 30 seconds before turning them back ON. This prevents damage to the input circuits of the 28 V dc power supplies.**

- Outputs J1R, J1S, and J1T can be powered from either the PDC bus or from Battery A only. Refer to the section, Configuration.
- Three outputs J7A, J7B, and J7C are fuse-protected and controlled by toggle switches. They provide output power to the Relay Output (TRLY) terminal board and similar boards.
- Three outputs J8A, J8B, and J8C are only fuse-protected. A 22 W resistor is inserted in series with each side to limit output power. These outputs supply power to boards such as the Contact Input (TBCI) terminal board, which require a source with limited short circuit capability to meet agency requirements.

### 28VDC Power Distribution

JPDC provides for TMR or Simplex 28 V dc power distribution. Three separate 28 V input connectors; JR, JS, and JT are provided. On each connector, two pins are connected in parallel to increase current-carrying capacity.

Eight output connectors do not have fuse protection: J1, JP1, JCR, JCS, JCT, JRS, JSS, and JTS. Output current should not exceed 12.5 A.

Twenty-six outputs have 1.6 A polyfuse protection. In TMR configuration, ten of these, JR1 through JR10, provide 28 PR power, eight provide 28 PS power, and eight provide 28 PT power.

One output, P4, has 0.5 A polyfuse protection and provides power to the PPDA I/O pack.

### Diagnostic Feedback Signals

FDBK\_A1: Attenuated voltage difference from PDC bus to ground.  $V\_A1/VPDC = 0.033316V/V$ .

FDBK\_A2: Attenuated voltage difference from NDC bus to ground  $V\_A1/VPDC = -0.033316V/V$ .

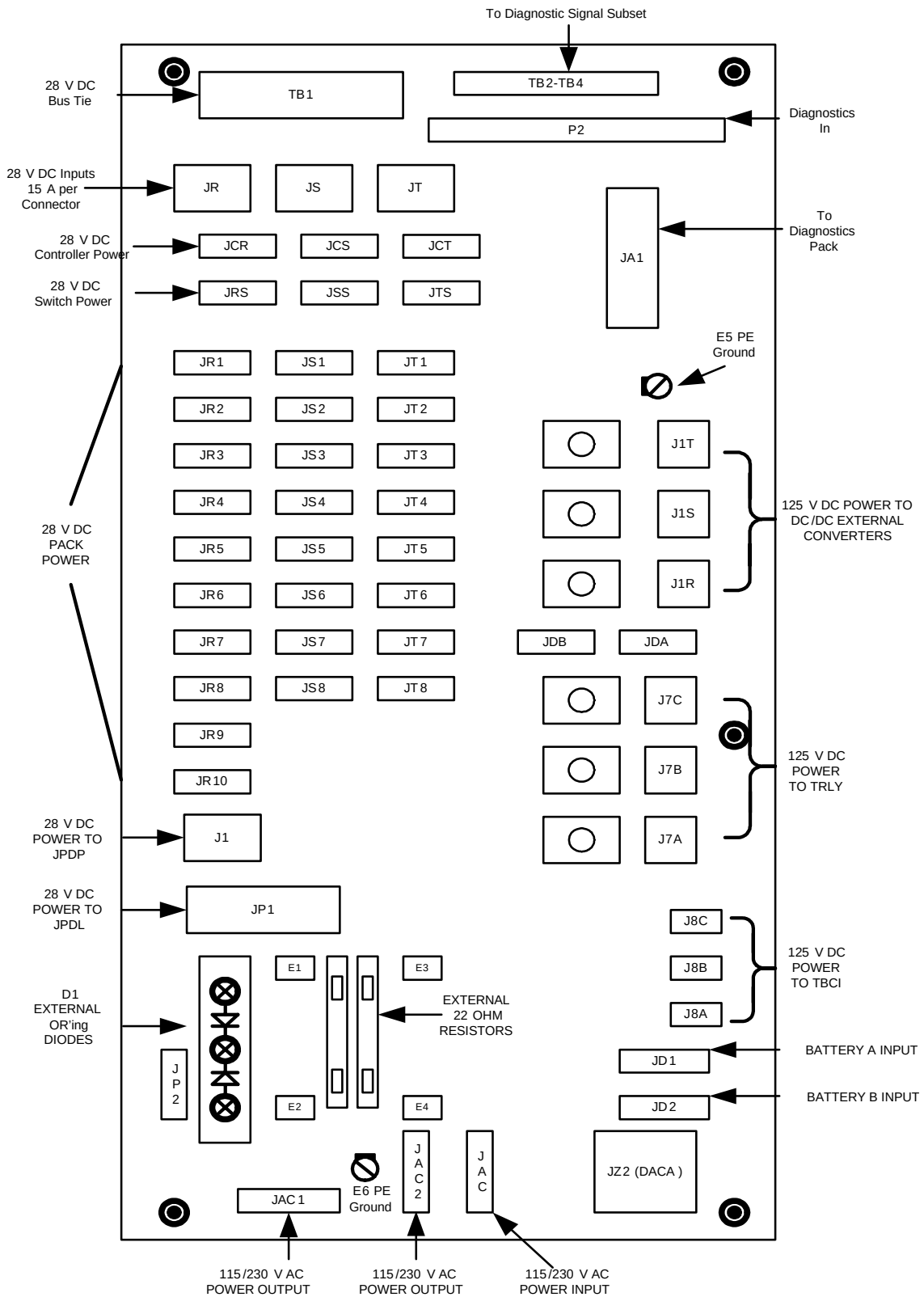
FDBK\_A3 and FDBK\_A4: Multiplexed feedbacks from J1S-T and J7A-C. (Requires PPDA I/O pack).

FDBK\_A5: Attenuated AC input voltage:  $V\_A5/VAC$  is approximately  $0.01885V/V$ .

FDBK\_B1: Multiplexed feedbacks from Battery 1 input, Battery 2 input, JAC1 output, and JAC2 output. (Requires PPDA I/O pack).

FDBK\_B2 – FDBK\_B4: Attenuated 28VDC R, S, and T inputs. Attenuation ratio =  $V_{feedback}/V_{in} = 0.143V/V$ .

Feedback\_B5: Multiplexed feedbacks from external 28VDC power supplies. (Requires PPDA I/O pack).



JPDC Connector Locations

## Specifications

|                         | Item                                                                                                        | Description                                                               |
|-------------------------|-------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|
| 28 V dc inputs          | Three 9-pin Mate-n-Lok connectors for 28 V dc Power Supply inputs: (JR, JS, JT)                             | 19 A max each                                                             |
|                         | One 50-pin ribbon cable with diagnostic data from upstream boards (P2)                                      | 15 V max                                                                  |
|                         | One 5-screw terminal block for daisy chaining power distribution boards                                     | 35 A max per screw                                                        |
| 28 V dc outputs         | One 6-pin Mate-n-Lok connector for a JPDP board (J1)                                                        | 13 A max per pin                                                          |
|                         | One 5-pin Mate-n-Lok connector for a JPDL board (JP1)                                                       | 13 A max per pin                                                          |
|                         | Three 2-pin Mate-n-Lok connectors for CPCI control rack power (JCR, JCS, JCT)                               | 13 A max per pin                                                          |
|                         | Three 2-pin Mate-n-Lok connectors for LAN switch power (JRS, JSS, JTS)                                      | 13 A max per pin                                                          |
|                         | Twenty six 2-pin mini-Mate-n-Lok connections fused, for auxiliary devices (JR1-JR10), (JS1-JS-8), (JT1-JT8) | 1.6 A polyfuse                                                            |
|                         | One 5-screw terminal block for daisy chaining power distribution boards (TP1)                               | 35 A max per screw                                                        |
|                         | One 2-pin connection for 28 V dc power to the PPDA I/O pack (P4)                                            | 0.5 A polyfuse                                                            |
|                         | One 62-pin D-shell connection for PPDA I/O pack (JA1)                                                       | 15 V max                                                                  |
| 115/230 V Ac input      | One 3-pin Mate-N-Lok connector (JAC)                                                                        | 13 A max.                                                                 |
|                         | Board Rating                                                                                                | 115/230 V ac<br>50/60 Hz<br>30 A circuit breaker protection               |
| 115/230 V Ac output     | Two 3-pin Mate-N-Lok connectors (JAC1, JAC2)                                                                | 10 A max. each                                                            |
|                         | Fuses for connectors JAC1-JAC2 and FUAC1-FUAC2: FU1-FU8                                                     | 10 A, 250 V, Littelfuse® 218010 is typical.                               |
| 125 V dc battery inputs | Two 4-pin Mate-n-Lok connectors (JD1, JD2)                                                                  | 20 A max. total current                                                   |
| 125 V dc DACA input     | One 12-pin Mate-n-Lok connector (JZ2)                                                                       | 10 A max.                                                                 |
|                         | Board Rating                                                                                                | 125 V dc nominal, 145 V dc maximum,<br>30 A circuit breaker protection    |
|                         | Impedance to ground                                                                                         | JP1 jumper in place > 75 kΩ<br>JP1 jumper removed > 1500 kΩ               |
|                         | Fuses for connectors J1R: FU1R- FU2R, J1S: FU1S-FU2S, J1T: FU1T-FU2T                                        | 10 A 250 V, Littelfuse® 218010 is typical                                 |
|                         | Fuses for connectors J7A: FU71-FU72, J7B: FU73-FU74, J7C: FU75-FU76                                         | 10 A 250 V, Littelfuse 217010 is typical                                  |
|                         | Fuses for connectors J8A: FU81-FU82, J8B: FU83-FU84, J8C: FU85-FU86                                         | 3.15 A 250 V, Littelfuse 2173.15 is typical                               |
|                         | Temperature Range                                                                                           | –30°C to 65°C (-22 to +149 °F)                                            |
|                         | Board Size                                                                                                  | 17.2 cm Wide x 48.26 cm High (6.75 in x 19.0 in)                          |
|                         | Module Size                                                                                                 | 17.78 cm Wide x 51.81 cm High x 7.62 cm Deep (7.0 in. x 20.4 in. x 3 in.) |
|                         | Mounting                                                                                                    | Back-panel mounting, adjacent to other power distribution boards          |

## Diagnostics

### Diagnostic Feedbacks

JPDC provides for the connection of a PPDA I/O pack for power distribution feedback to the IONet. The PPDA I/O pack mounts on the JPDC.

JPDC uses two feedback signal groups on the PPDA I/O pack connector comprised of the following ten diagnostic signals:

| Signal | Description                                           |
|--------|-------------------------------------------------------|
| A1     | PDC bus volts to earth magnitude                      |
| A2     | NDC bus volts to earth magnitude                      |
| A3     | J7A, J7B, J7C (125 V dc outputs) feedback multiplexed |
| A4     | J1R, J1S, J1T (125 V dc outputs) feedback multiplexed |
| A5     | AC1 feedback magnitude                                |
| B1     | JAC1, JAC2, BATT1, and BATT2 feedback multiplexed     |
| B2     | 28 V dc R feedback magnitude                          |
| B3     | 28 V dc S feedback magnitude                          |
| B4     | 28 V dc T feedback magnitude                          |
| B5     | 28 V dc R, S, T P.S. contacts multiplexed             |

There are no feedback signals provided for the three fused TBCI terminal board outputs (J8A, J8B, and J8C) since each TBCI terminal board has its own voltage monitoring circuit.

Feedbacks also include an electronic ID identifying the board type, revision, and serial number.

A 50-pin ribbon cable connector (P2) is used to daisy chain the diagnostic signals from other distribution boards to JPDC. Up to four additional boards may be cabled into JPDC for PPDA I/O pack reception. In a JPDC-based PDM system, the PPDA I/O pack must be mounted on JPDC.

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**Note** A P1 connector is not provided to feed JPDC diagnostic signals to another location.

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Three terminal boards (TB2, TB3, and TB4) are mounted end to end at the top of JPDC and permit access to the analog diagnostic feedback signals without the need for a PPDA I/O pack.

### Diagnostic Circuits

Test rings TP1 and TP2 are connected to ACH and ACL respectively of the ac input line to allow monitoring ac bus voltage. Each has a 30.1 K buffer resistor in series. Test rings TP3 and TP4 are connected to positive and negative sides respectively of the 125 V dc bus. Each has a 30.1 K buffer resistor. Test ring TP5 is connected to the negative or return side of all three 28 V dc inputs. (No buffer resistor is provided). Test rings TP6, TP7, and TP8 are connected to 28PR, 28PS, and 28PT respectively. These are the positive lines of the three 28 V dc TMR power inputs. (No buffer resistors are provided).

## Configuration

### 28 V dc TMR Configuration

- Separate power inputs are received through connectors JR, JS, and JT.
- The positive sides of the three inputs are connected to separate power busses, designated as 28PR, 28PS, and 28PT respectively. The return sides of the three inputs are connected together and designated as 28N.
- Output power is distributed from the three busses through separate R, S, and T output connectors.

### 28 V dc Simplex Configuration

- One, two, or three 28 V dc power inputs can be received through connectors JR, JS, and JT.
- The three power busses can be connected into a single bus by inserting jumpers between terminals 1, 2, and 3 of terminal board TB1.
- All output connectors are fed from the single 28 V dc bus.

### 125 V dc outputs to external 125 V dc/28 V dc power supplies

- Two options are provided for the selection of power outputs through connectors J1R, J1S, and J1T.
- For normal operation, a shorting plug is inserted in connector JDB. This configuration selects 125 V dc power from the entire P125 bus, which is fed by both battery inputs and the DACA input.
- A second mode of operation allows the user to replace the DACA supply with an ac/dc converter of lower power rating. In such a case the shorting plug should be moved to connector JDA. This configuration selects power for connectors J1R, J1S, and J1T from Battery A only and allows the lower-rated ac/dc converter to supply power only to the other 125 V dc outputs.



#### Caution

Never jumper connectors JDA and JDB at the same time.

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## Handling Precautions



#### Caution

To prevent component damage caused by static electricity, treat all boards with static sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation.

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#### Warning

This equipment contains a potential hazard of electric shock, burn, or death. Ensure that all Lockout/Tagout procedures are followed prior to replacing terminal boards. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

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## Module Replacement

### ➤ To replace the module

- 1 Lockout and/or tagout all energy sources to the module.
- 2 Check the voltage on each terminal to ensure no voltage is present.
- 3 Note the orientation of the module and the location of any jumpered connections. Verify the label and unplug all connectors.

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**Note** Do NOT remove any jumpers, if applicable.

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- 11 Unscrew and remove the board grounding wires.
- 12 Remove the hardware used to fasten the module to the cabinet.
- 13 Inspect the new module for shipping damage.
- 14 Install the new module into the cabinet in the same orientation as the old module.
- 15 Verify all jumpered connections on the new module, are the same as those jumpered on the old module.
- 16 Reconnect the board grounding wires.
- 17 Reconnect all wire and cable connectors.
- 18 Remove the Lockout and/or tagout and restore power to the module.
- 19 Test/verify that all switches, fuses, LEDs, and I/O packs function properly.

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## JPDD dc Power Distribution

### Functional Description

The dc Power Distribution (JPDD) board provides dc power distribution, power isolation, and branch circuit protection for control or I/O functions requiring 125 V dc or 24 V dc power. Typical applications include dc relay and solenoid control power, and contact wetting. Each output includes a fuse, a switch, and a lamp to indicate the presence of output voltage. JPDD is not intended for power distribution to the I/O packs.

### Board Versions

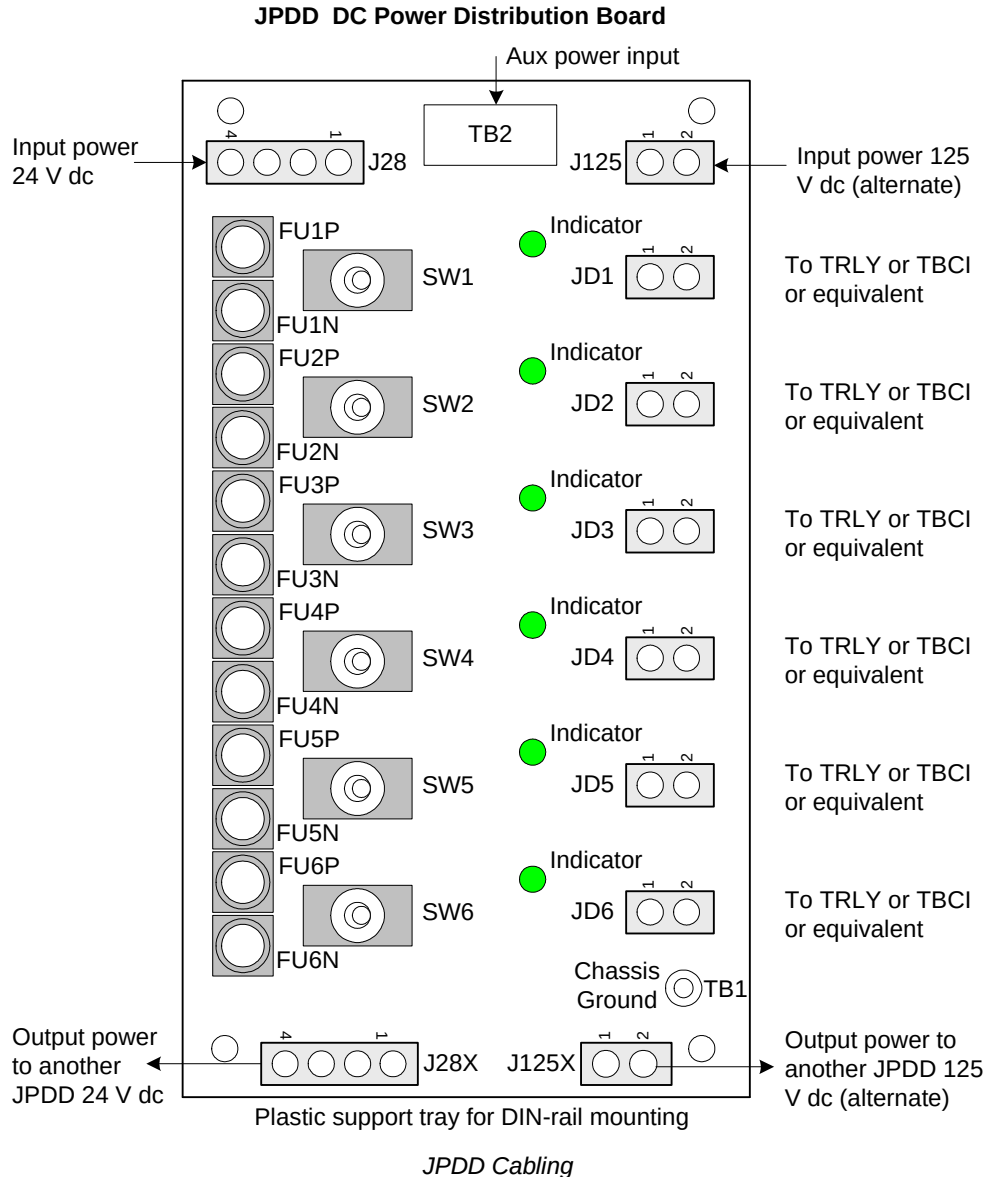
| Terminal Board | Fusing |
|----------------|--------|
|----------------|--------|

|        |                                                                |
|--------|----------------------------------------------------------------|
| JPDDG1 | Each circuit provided with ¼ in x 1¼ in 15 A 250 V fuse        |
| JPDDG2 | Empty fuse holders with black caps accepting 5 x 20 mm fuses   |
| JPDDG3 | Empty fuse holders with grey caps accepting ¼ in x 1¼ in fuses |

JPDDG1 provides fuses that are coordinated with the rating of the system wiring and connectors. JPDDG2 and G3 are used when fuse ratings coordinated with a specific application are required. Two different fuse sizes are provided to accommodate local fuse preferences.

## Installation

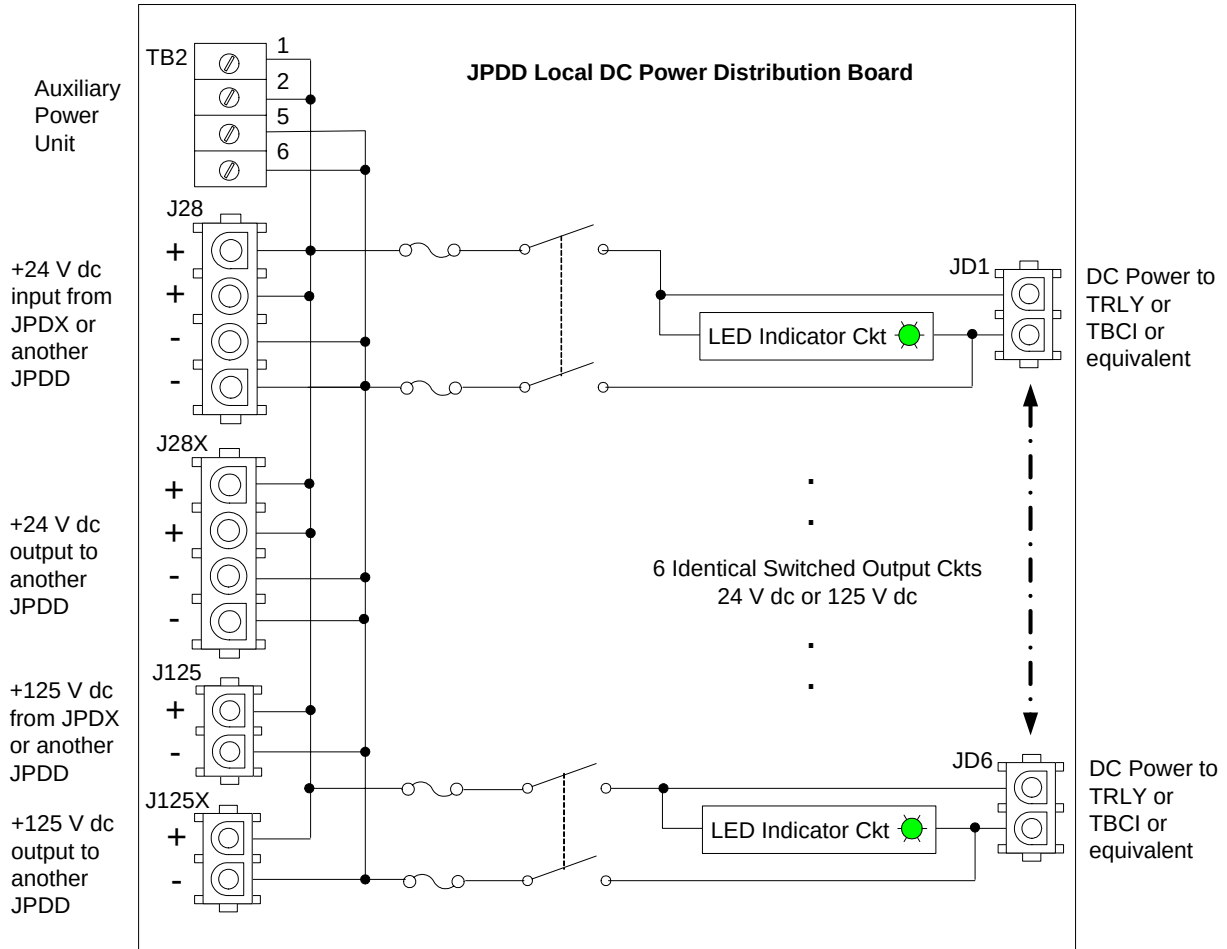
JPDD is held in a plastic holder, which mounts on a vertical DIN-rail. When installing the JPDD, it is important to provide a ground lead from TB1 to the system ground. This creates a ground path for the metal switch bodies.



Power input can be either 24 V dc or 125 V dc, but not both together. For cable destinations, refer to the circuit diagram. TB1 should be connected to system ground.

## Operation

The following figure shows how the 125 V dc or 24 V dc power is distributed in JPDD, and how it reaches the TRLY and TBCI boards.



JPDD Simplified Circuit Diagram

### Inputs

Multiple JPDD boards can receive power from a single Main Power Distribution Module branch circuit. Power input can be either 125 V dc or 24 V dc nominal.



### Caution

**Both inputs share a common electrical path, therefore, both the 125 V dc and 24 V dc cannot be applied at the same time.**

Two 2-Pin Mate-N-Lok connectors are provided for 125 V dc power. One connector receives input power and the other can be used to distribute 125 V dc power to another JPDD board in daisy chain fashion.

Two 4-pin Mate-N-Lok connectors are provided for 24 V dc power. These perform functions similar to those of the 2-pin connectors above. The 4-pin connector permits parallel connection of two pin-pairs for increased current capacity. It is expected that neither side of the dc power input is grounded.

## Outputs

Six identical output circuits are provided. Each output circuit includes two fuses, a switch with a pair of isolation contacts in each side of the output, and a green lamp to indicate the presence of voltage across the output terminals. The provision of a fuse and switch contact in each side of the dc path allows use of this board with floating power sources.

## Specifications

| Item         | Description                                                        |                            |
|--------------|--------------------------------------------------------------------|----------------------------|
| Inputs       | One 2-pin connection for input power from JPDx or another JPDD     | 125 V dc, 15 A             |
|              | One 4-pin connection for input power from JPDx or another JPDD     | 24 V dc, 30 A              |
|              | One auxiliary power input through TB2                              |                            |
| Outputs      | Six 2-pin connections for power to TRLY or TBCI                    | 24 V dc or 125 V dc, fused |
|              | One 2-pin connection for output power to another JPDD              | 125 V dc                   |
|              | One 4-pin connection for output power to another JPDD              | 24 V dc                    |
| Output Fuses | 12 fuses, two per output                                           | 250 V, 15 A                |
| Temperature  | -30 to +65°C (-22 to +149 °F)                                      |                            |
| Board Size   | 23.495 cm high x 10.795 cm wide (9.25 in x 4.25 in)                |                            |
| Mounting     | DIN-rail, card carrier mountingBase mounted steel bracket, 4 holes | Vertical rail              |

## Diagnostics

No diagnostic features are provided on this module.

## Configuration

There are no jumpers on JPDD. Check the position of the six output load switches.

It is possible to use other fuse ratings with this board to provide specific branch circuit ratings. A typical series of fuses that work with this board are the Bussmann ABC series of fuses with ratings from ¼ A through 15 A. Fuses above 15 A shall not be used with this board. If alternate fuse ratings are used, configuration of the board requires the insertion of the proper fuse in each branch circuit.

---

# ***JPDE dc Battery Power Distribution***

## ***Functional Description***

The dc Battery Power Distribution (JPDE) board receives dc power from a battery or power supplies and distributes it to terminal boards and other system loads. JPDE supports a floating dc bus that is centered on earth using resistors and provides voltage feedback through PPDA to detect system ground faults. It provides inputs for two power supplies. JPDE is able to operate at either 24 V dc or 48 V dc. JPDE integrates into the PDM system feedback offered through the PPDA I/O pack.

This board is limited by the current that can be passed through it using conventional board construction. JPDE does not supply power to bulk 500 W - 24 V input/28 V output power supplies providing I/O pack control power.

## ***Compatibility***

The IS200JPDE board is compatible with the feedback signal P1/P2 connectors on JPDB, JPDB, JPDS, and JPDM leading to a PPDA I/O pack.

## ***Installation***

JPDE is base-mounted vertically on a metal bracket in a cabinet used by the PDM. Refer to the wiring diagrams for power input and output routing. There is a 50-pin diagnostic connector mounted on the top and bottom of the board.

## ***Grounding***

The IS200JPDE board is grounded through the sheet metal bracket to the underlying back base. In most cases, this is the system FE.

## ***Physical Arrangement***

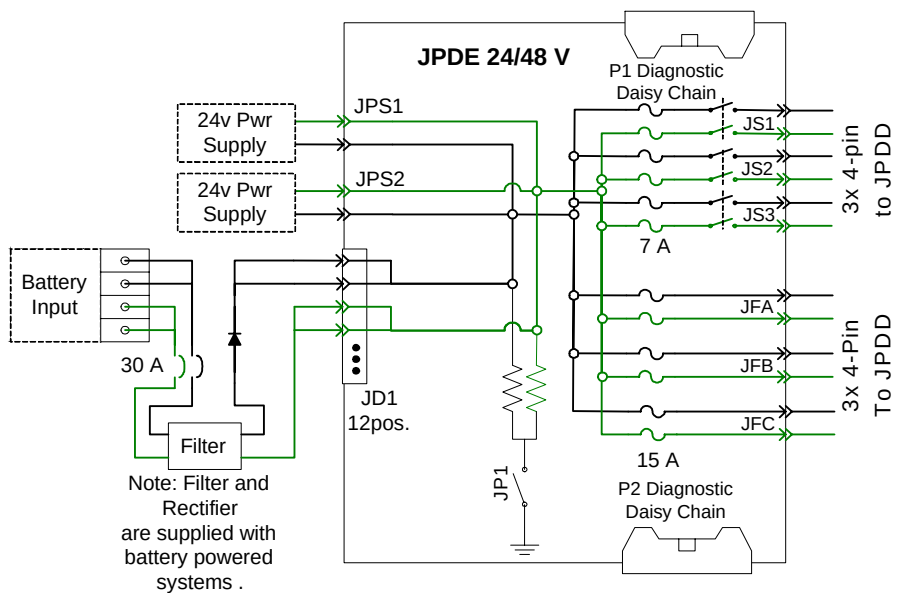
The location of JPDE is not critical in a panel. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA. If a cable connection from JPDE to a board containing PPDA is planned, consideration should be given to the feedback cable routing between JPDE P1 and the P2 connector on the board receiving the feedback cable.

## ***Application Notes***

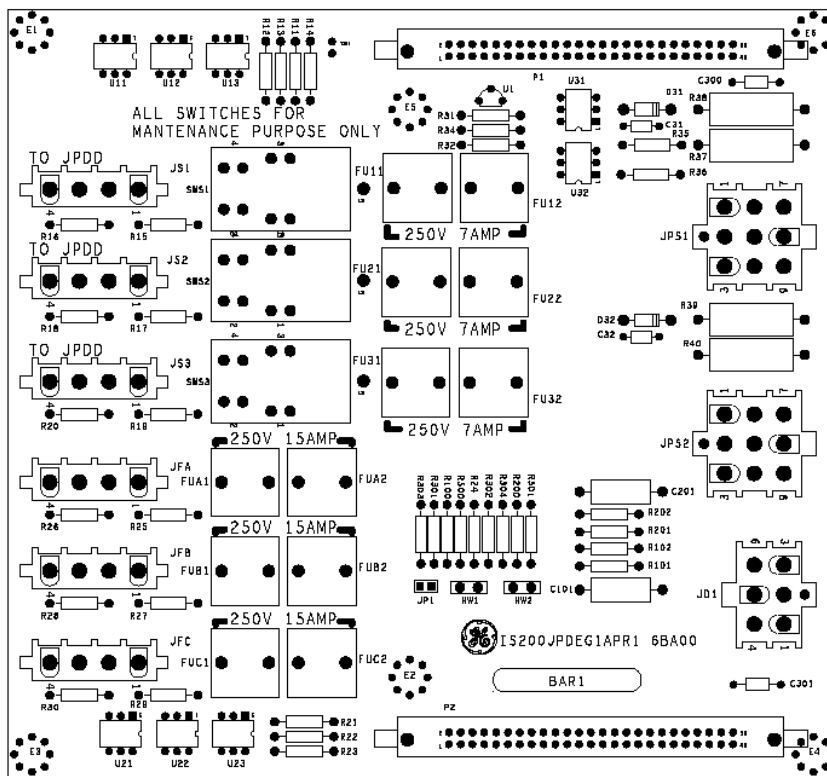
JPDE can be used with one or two power supplies to create a dc power system for terminal boards and other system loads. When this is done, float the dc power system and use the grounding resistors on JPDE to center the bus on earth. This permits detection of ground faults through the PPDA bus voltage feedback. Jumper JP1 is required to be in place, connecting the centering resistors to earth.

When JPDE is used to distribute battery power, it is supplied with a dc circuit breaker and a 30 A input filter.

## Operation



*JPDE Simplified Electrical Diagram*



## JPDE Mechanical Layout

## I/O Characteristics

- JD1 is a 12-pin Mate-N-Lok<sup>®</sup> connector that accepts power input from a battery. Six connector pins are used for each of the two input circuits to provide adequate current rating
- JPS1 and JPS2 are nine-pin Mate-N-Lok connectors used for power supply input. The connector uses pins 7 and 9 for positive 24/48 V dc and pins 1-3 for 24 V return providing 24 A steady state capacity. Pin 4 provides positive 10 V dc wetting to a supply status feedback switch and pin 5 provides the return.
- JS1, JS2, and JS3 are fused and switched four-pin Mate-N-Lok output connectors. Positive power is on pins 1 and 2, and negative power is on pins 3 and 4. This matches the pin use on JPDD J28 and J28X. The fuse rating for these switched connectors is 7 A.
- JFA, JFB, and JFC are fused four-pin Mate-N-Lok output connectors. Positive power is on pins 1 and 2, and negative power is on pins 3 and 4. This matches the pin use on JPDD J28 and J28X. These connectors have a fuse rating of 15 A.
- JP1 is the ground reference jumper. The dc bus is normally operated without a hard ground connection. The dc bus is centered on earth as part of the ground fault detection scheme. Normally, the 24 V operation of the dc positive terminal would measure  $\frac{1}{2} * 24$  V above ground and the negative terminal has the same magnitude below ground potential. Resistors to center the bus on earth are supplied externally to the JPDE, or on-board resistors can be used by closing jumper JP1.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

## Specifications

| Item                                                         | Description                                                                    |
|--------------------------------------------------------------|--------------------------------------------------------------------------------|
| Total board rating                                           | 30 A total dc current from all branch circuits<br>50 V maximum nominal voltage |
| Fuse for connectors JS1-JS3:<br>FU11-12, FU21-22, FU31-32    | 7 A, 250 V, Bussmann <sup>®</sup> ABC-7 typical                                |
| Fuse for connectors JFA, JFB, JFC:<br>FUA1-2, FUB1-2, FUC1-2 | 15 A 250 V, Bussmann ABC-15 typical                                            |
| Board Size                                                   | 16.51 cm High x 17.8 cm Wide (6.5 in. x 7 in.)                                 |
| Mounting                                                     | six mounting holes                                                             |

## Diagnostics

Diagnostic signals routed into PPDA through connector P1 include:

- An electronic ID identifying the board type, revision number, and serial number
- Two analog battery voltage feedbacks. One is for positive bus and one is for negative bus. Voltage feedback accuracy is  $\pm 1\%$ .
- Three switched/fused dc branch circuit status signals
- Two dc power converter output status dry contact status signals
- Three fused branch circuit status signals
- Two test points with series 2.15 k $\Omega$  resistors are provided on the 24/48 V dc bus for external test equipment. HW1 is connected to the positive bus and HW2 is connected to the negative bus.

## ***Configuration***

When jumper JP1 is in place, the JPDE provides 6 k $\Omega$  voltage-centering resistors from positive and negative dc to the local earth connection. When JP1 is removed, the connection to earth is opened. Insert JP1 when a floating dc bus needs to be centered on earth.

---

## ***JPDF 125 V Power Distribution***

### ***Functional Description***

The 125 V Power Distribution (JPDF) board accepts redundant 125 V dc power inputs and distributes power to other system boards. JPDF works with a floating dc bus that is centered on earth rather than with a grounded system. This permits detection of a system ground fault and carries a non-hazardous live 125 V dc rating.

Input 125 V dc battery power is connected to a terminal board on the IS2020JPDF module. The power is then routed through a 125 V dc 30 A circuit breaker and line filter before being connected to the IS200JPDF board through the J1 connector. Dc voltage is then routed to three fused, non-switched outputs and six fused, switched outputs.

Ac power is routed through the board to the DACA modules where it is converted to dc power. Dc power returns to JPDF where it is combined with the battery power input. JPDF can operate with any combination of one or more inputs active creating a high-reliability source of 125 V dc power for the control system.

The IS2020JPDF module provides full status feedback using a connection to a PPDA I/O pack. Feedback includes bus magnitude, ground fault detection, and detection of excessive ac voltage on the dc bus. Each fused branch circuit is monitored to indicate the presence of output power.

### ***Compatibility***

The IS2020JPDF is compatible with the feedback signal connectors, P1/P2, on JPDB, JPDE, JPDS, and JPDM leading to a PPDA I/O pack. Connector JAF1 is compatible with the ac power output on the IS2020JPDB module. Connectors JZ2 and JZ3 are compatible with the connectors on the IS2020DACA module.

### ***Installation***

The IS2020JPDF module is base-mounted vertically on a metal back base in a cabinet used by the PDM. A connection must be made between the IS2020JPDF sheet metal and the system protective earth (PE).

Input battery power is applied to terminals DCHI and DCLO. If one or two DACA modules are used, ac power is applied to JAF1, typically from an IS2020JPDB module. DACA modules connect to JPDF through connectors JZ2 and JZ3.

Output circuits are connected as documented for the system.

A power distribution system featuring a PPDA power diagnostic I/O pack requires a 50-pin ribbon cable from JPDF connector P1 to the P2 connector on the board holding PPDA. This connection can pass through other core PDM boards using the P2 connector.



## ***Grounding***

Mark\* Vle systems divide ground into a protective earth (PE) and a functional earth (FE). The PE ground must be connected to an appropriate earth connection in accordance with all local standards. The minimum grounding must be capable of carrying 60 A for 60 seconds with no more than a 10 volt drop. The FE ground system must be bonded to the PE ground system at one point.

The JPDP is grounded through metal mounting supports fastened to the underlying sheet metal of a metal module. The ground is applied to the metal switch bodies on JPDP. Additionally, the ground is used as a local reference point when creating the feedback signals appearing on P2. The sheet metal of the module is insulated to the surface upon which it is mounted. This is done specifically to allow definition of the JPDP ground independent of the mounting surface. Typically, JPDP is mounted to a back base grounded to FE. JPDP would be located low in the cabinet and a separate ground wire from the JPDP module would be provided to PE. The minimum length of the ground wire is important to keep impedance low at radio frequencies allowing the input line filters to function properly.

## ***Physical Arrangement***

JPDP accepts power input from the right side of the board and delivers power out of the left side. When JPDB is used with JPDP, the JAF1 connector provides ac power to JPDP. JPDP should be physically located beneath JPDB minimizing the length of the JAF1 power wiring. JPDP is mounted to allow a minimum length of grounding wire between the module sheet metal and the nearest PE connection point. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA. The P1 and P2 ribbon cable headers on all of the core boards are mounted so the JPDS or JPDM, holding the PPDA I/O pack, is located at the top of the board arrangement. This allows ribbon cables to flow from the top of one board and into the bottom of the next board until the PPDA host is reached.

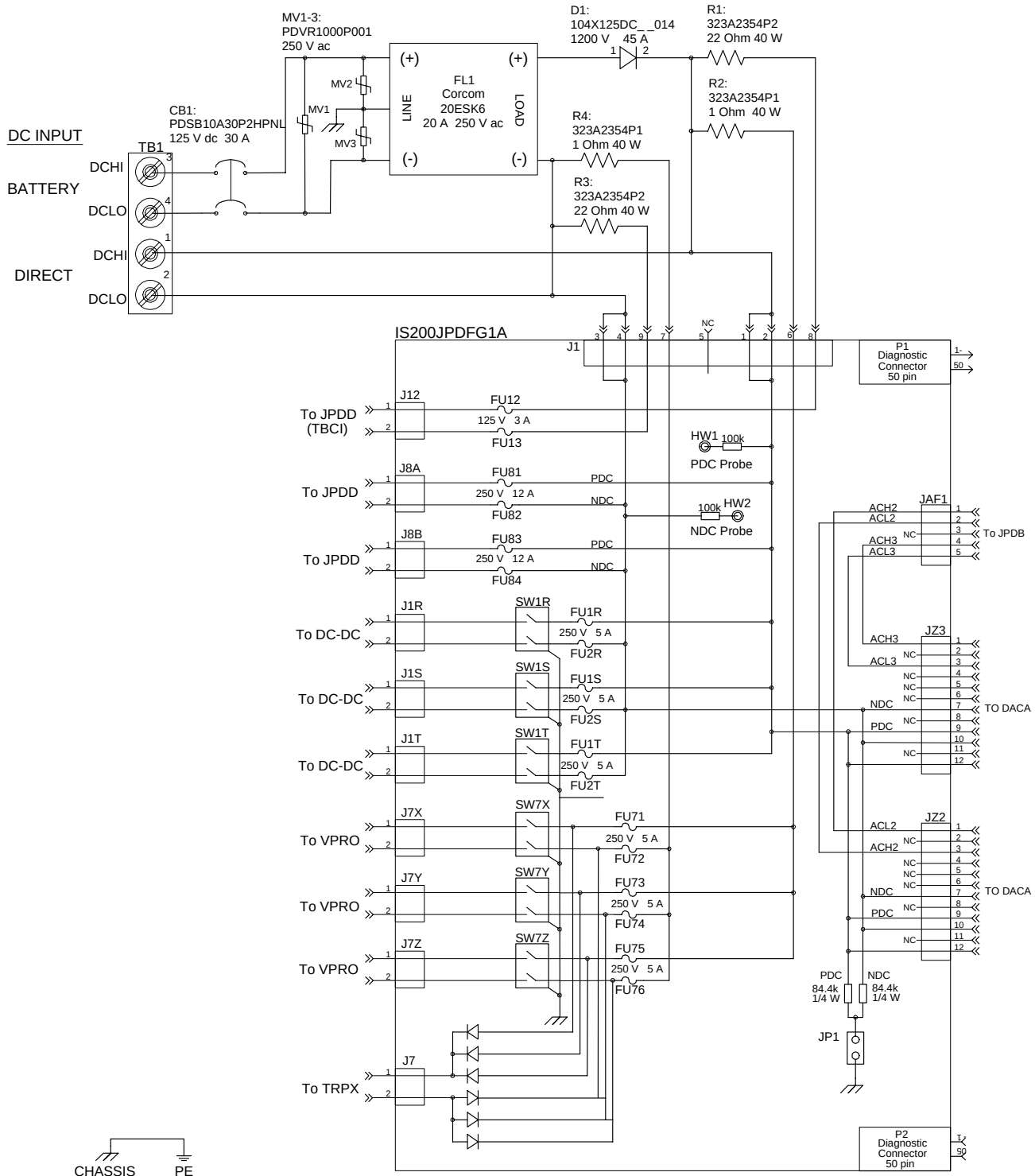
## ***Ground Fault Detection***

The IS2020JPDP module supports the use of a dc bus that is centered on ground potential by a high resistance. This arrangement allows the detection of a ground fault when the positive bus or negative bus voltage goes to ground potential. In support of this arrangement, the IS2020JPDP includes separate voltage feedback sensing for positive and negative power with respect to ground. When the feedback is cabled into a PPDA I/O pack detection of ground faults is provided to the system.

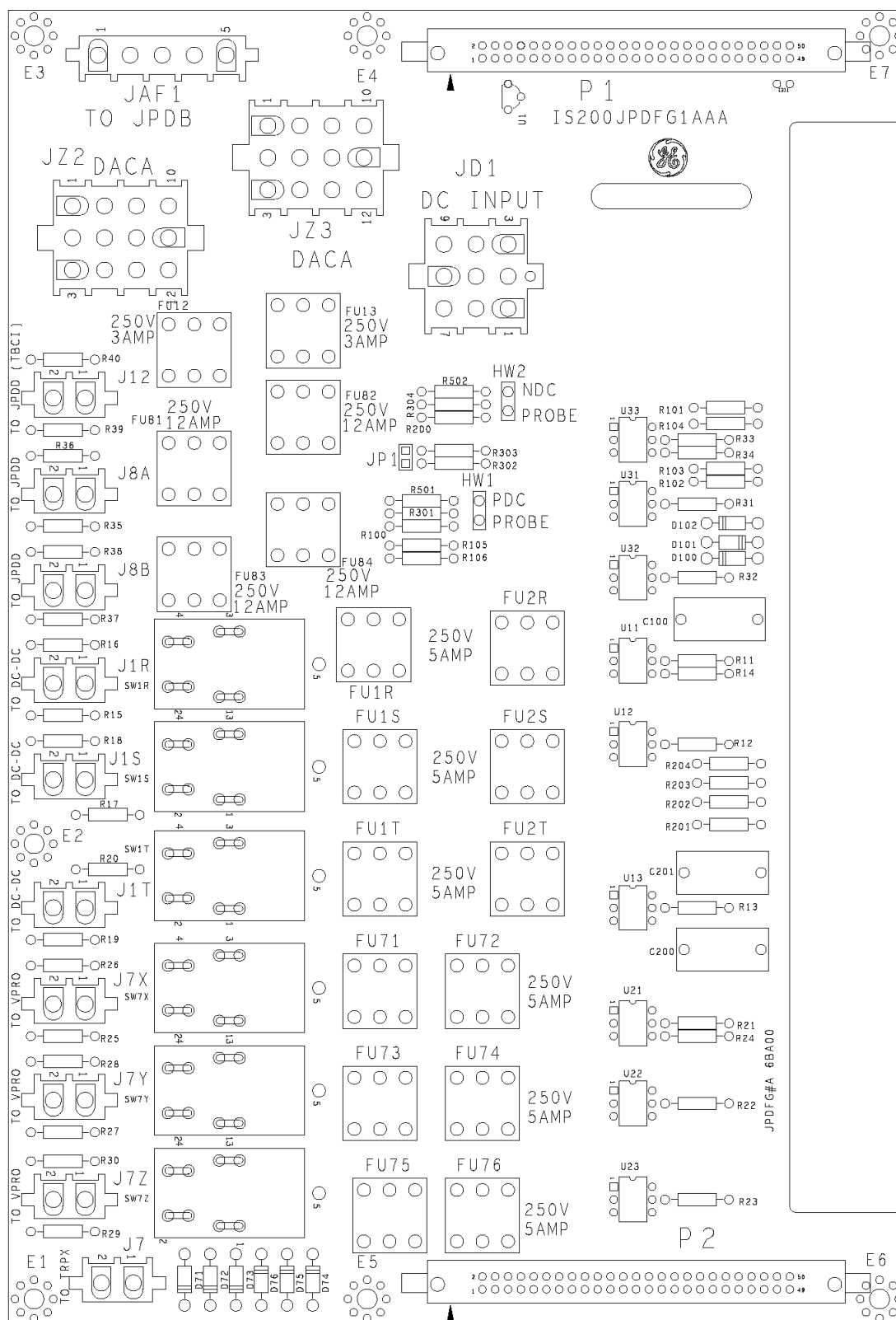
The resistance used centering the dc bus on ground sets the ground detection sensitivity and ground fault currents that can flow. IS2020JPDP contains centering resistors selected by jumper JP1. Should centering resistance be provided elsewhere, then the jumper on JPDP should be open. JPDP is designed to then insert minimal centering resistance in the system. If JPDP is providing the centering function, JP1 should be closed. If two JPDP modules are used, only one should have a closed JP1 jumper.

## Operation

Dc battery power is applied to terminals DCHI and DCLO. It then goes through a 30 A dc circuit breaker into a filter assembly located under the IS200JPDF circuit board. Filtered output is then passed through a series diode to the JPDD circuit board. Ac power is applied to the JAF1 connector. The 115/230 V ac is routed to two connectors, JZ2 and JZ3, and out to two DACA modules. The DACA modules convert the ac power to 125 V dc. The dc power returns to JPDD through the same JZ2 and JZ3 connectors and combined with battery power if present.



JPDD Electrical Diagram



JPDF Mechanical Board Layout

## ***I/O Characteristics***

The following I/O characteristics apply to the IS2020JPDF module:

- The JPDF module has a barrier terminal strip containing two battery input screw terminals located on the right side of the circuit board. The dc input is rated at 30 A, and the voltage should never exceed 145 V dc. Protection of the Branch circuit protection supplying power to this input is a 30 A circuit breaker, supplied by default as part of the module. This is the primary power input.
- Two dc output screw terminals, located on the same barrier terminal strip, are not normally used, but are provided to allow two JPDF boards to work in parallel.
- JD1 is a nine-pin Mate-N-Lok<sup>®</sup> connector that accepts the power input from the components that are mounted under the JPDF board. JD1 uses a wire harness that is part of the JPDF module assembly.
- JAF1 is a five-pin Mate-N-Lok connector that accepts the 115/230 V ac input from the JPDB board. The 115/230 V ac is routed to two connectors, JZ2 and JZ3, and out to two DACA modules. The DACA modules convert the ac power to 125 V dc.
- Two 12-pin Mate-N-Lok connectors, JZ2 and JZ3, pass ac power to two DACA modules. The DACA modules convert 115/230 V ac to 125 V dc. Dc power returns through the JZ2 and JZ3 connectors.
- Three fused and switched two-pin Mate-N-Lok output connectors, J1R, J1S, and J1T, are provided for powering 125 V dc/28 V dc converters. The 28 V dc is the control power for I/O packs. Positive power is on pin 1 and negative power is on pin 2. The fuses are rated at 5 A.
- Three fused and switched two-pin Mate-N-Lok output connectors, J7X, J7Y, and J7Z, are provided for powering up to three Mate-N-Lok modules. Positive power is on pin 1, negative power is on pin 2, and fuse rating is 5 A. Two 1  $\Omega$  resistors mounted under the board define the minimum source impedance for these circuits.
- A two-pin Mate-N-Lok output connector, J7, is provided to supply power to the system trip boards. Positive power is on pin 1 and negative power is on pin 2. The output power comes from the circuits associated with J7X, J7Y, and J7Z. The output power is combined through diodes and is only lost when all three circuits have blown fuses or open switches.
- There are two 12 A fused two-pin, Mate-N-Lok output dc connectors on both J8A and J8B. They feed remote JPDD boards to provide individual switched/fused circuits to TRLY boards and other system loads. Positive power is on pin 1 and negative power on pin 2.
- A two-pin Mate-N-Lok output connector, J12, is provided specifically to operate TBCI contact input boards. Two 22  $\Omega$  resistors mounted under the JPDF board define the minimum source impedance for this circuit. Positive power is on pin 1 and negative power is on pin 2.
- The ground reference jumper is JP1. The dc bus is normally operated without a hard ground connection, but it is desirable to center the dc on earth as part of the ground fault detection scheme. In normal operation, the positive terminal would measure  $\frac{1}{2}$  \* 125 V above ground and the negative terminal would measure the same magnitude below ground potential. The resistors used to center the bus on earth can be supplied externally to the JPDF, or on-board resistors can be used by closing jumper JP1.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA.

## Specifications

| Item                                                                   | Description                                                                           |
|------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Board rating                                                           | 125 V dc nominal, 145 V dc maximum 30 A circuit breaker protection                    |
| Impedance to ground                                                    | With JP1 jumper in place > 75 k $\Omega$<br>With JP1 jumper removed > 1500 k $\Omega$ |
| Fuse for connectors J1R, J1S, J1T - FU1R, FU2R, FU1S, FU2S, FU1T, FU2T | 10 A 250 V, Bussmann <sup>®</sup> MDA-10 typical                                      |
| Fuse for connectors J7X, J7Y, J7Z - FU71-FU76                          | 5 A 250 V, Bussmann ABC-5 typical                                                     |
| Fuse for connectors JBA, JBB - FU81-FU84                               | 12 A 250 V, Bussmann ABC-12 typical                                                   |
| Fuse for connector J12: FU12 - FU13                                    | 3 A, 250 V, Bussmann ABC-3 typical                                                    |
| <b>Physical</b>                                                        |                                                                                       |
| Modules Size                                                           | 30.48 cm High x 21.33 cm Wide x 16 cm Deep (12 in. x 8.4 in. x 6.3 in.)               |
| Mounting                                                               | Four mounting holes, #10 screws                                                       |

## Diagnostics

Diagnostic signals routed into PPDA through connector P1 include:

- An electronic ID identifying the board type, revision, and serial number
- Two 125 V dc voltage feedbacks for voltage magnitude determination, ground fault detection, and ac signal present detection
- Six switched/fused dc supply indications for J1R, J1S, J1T, J7X, J7Y, and J7Z
- Three fused dc supply indications for J8A, J8B, and J12
- Two hardware test rings, with series 100 k $\Omega$  resistors, are provided for attaching test equipment. HW1 is labeled PDC Probe and HW2 is labeled NDC Probe.

## Configuration

**TBCI** boards, when powered by JPDPF, should use connector J12 using a JPDD fan-out board. The 44  $\Omega$  source impedance is coordinated with the circuit ratings on TBCI.

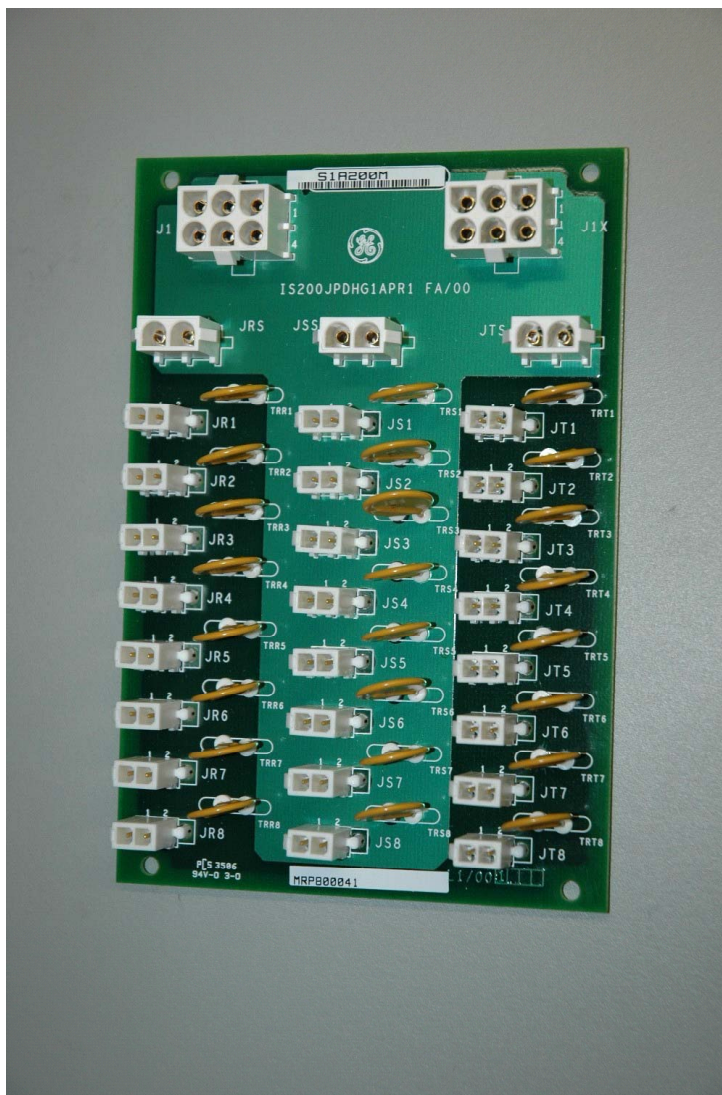
**TRPG/TREG** board pair, critical to system operation, should be powered by the J7 connector.

**JP1** should be in place if JPDPF is providing bus voltage centering resistors for ground fault detection. JP1 should be omitted if another location is providing centering resistance.

# JPDH High Density Power Distribution

## Functional Description

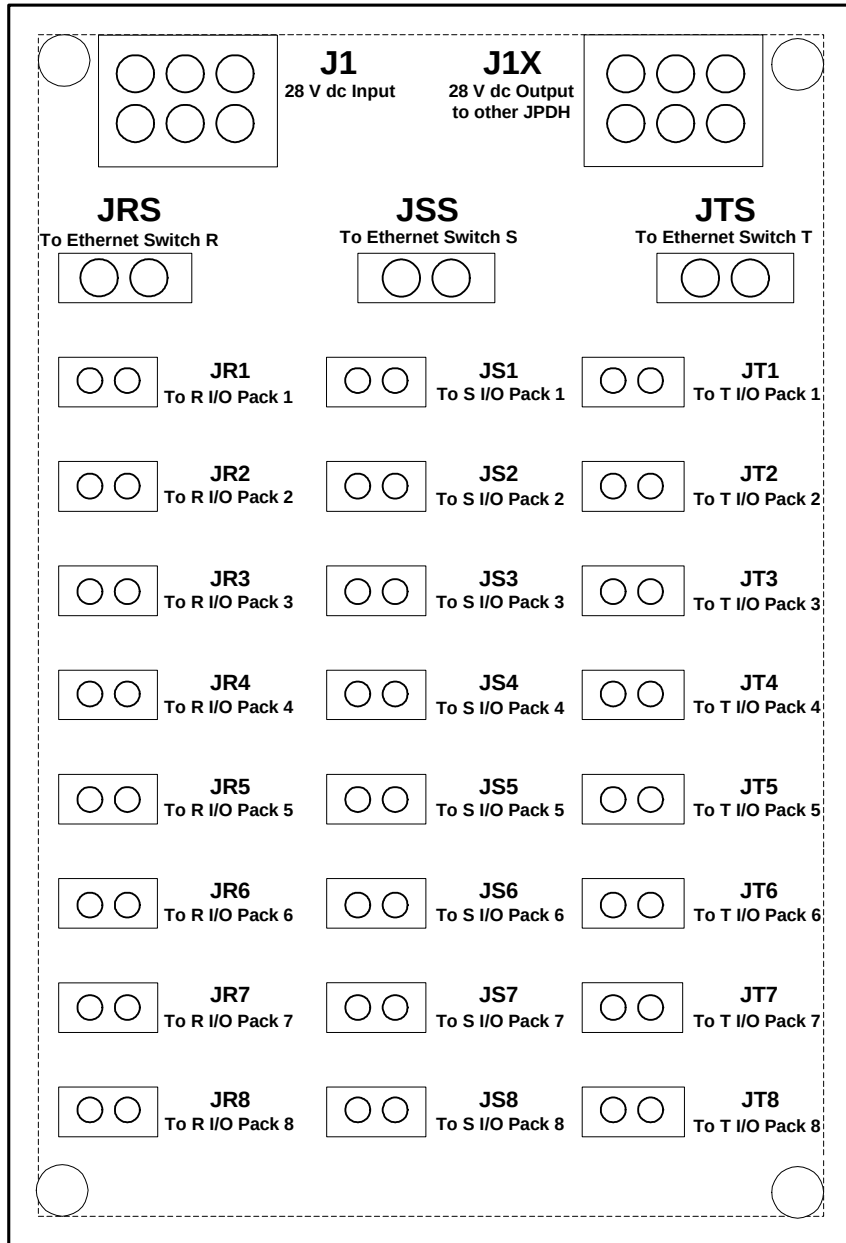
The High Density Power Distribution (JPDH) board provides 28 V dc power to 24 Mark\* VIE I/O packs and 3 Ethernet switches from a 28 V dc supply. Additional JPDHs can be connected in a daisy-chain arrangement to provide power to more I/O packs as required. The circuit for each I/O pack connector is protected with a positive temperature coefficient fuse device.



*JPDH Power Distribution Board*

## Installation

Mount JPDH on a vertical surface by inserting #6 machine screws through the mounting holes at each corner of the board. Insert Mate-N-Lok connectors as described in the following figure. The 6-pin and larger 2-pin connectors have a nominal rating of 600 V and 13 A, while the smaller two-pin connectors have a nominal rating of 600 V and limited by fuse rating to 0.8 A max.



JPDH Connections

## Operation

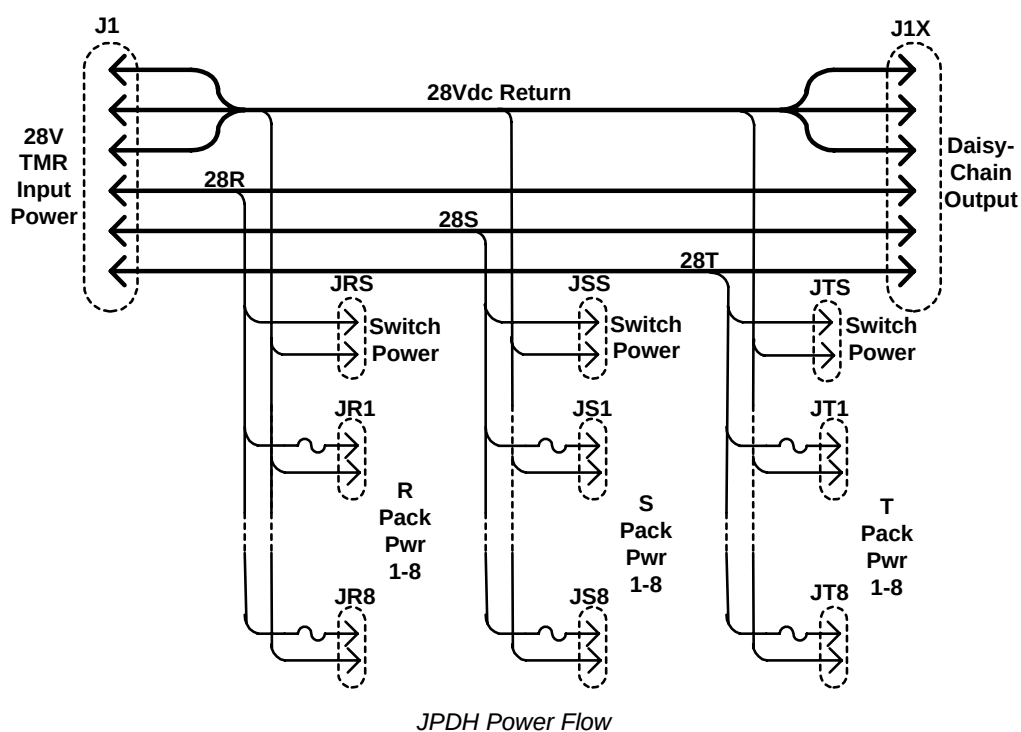
JPDH is designed to provide TMR I/O packs with adequate 28 V dc power distribution while taking up as little space as possible. Additional JPDHs can be connected in a daisy-chain arrangement through the unfused J1X connector.

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**Note** The user must provide suitable branch circuit protection when connecting multiple JPDHs. Each pin is rated at 13 A.

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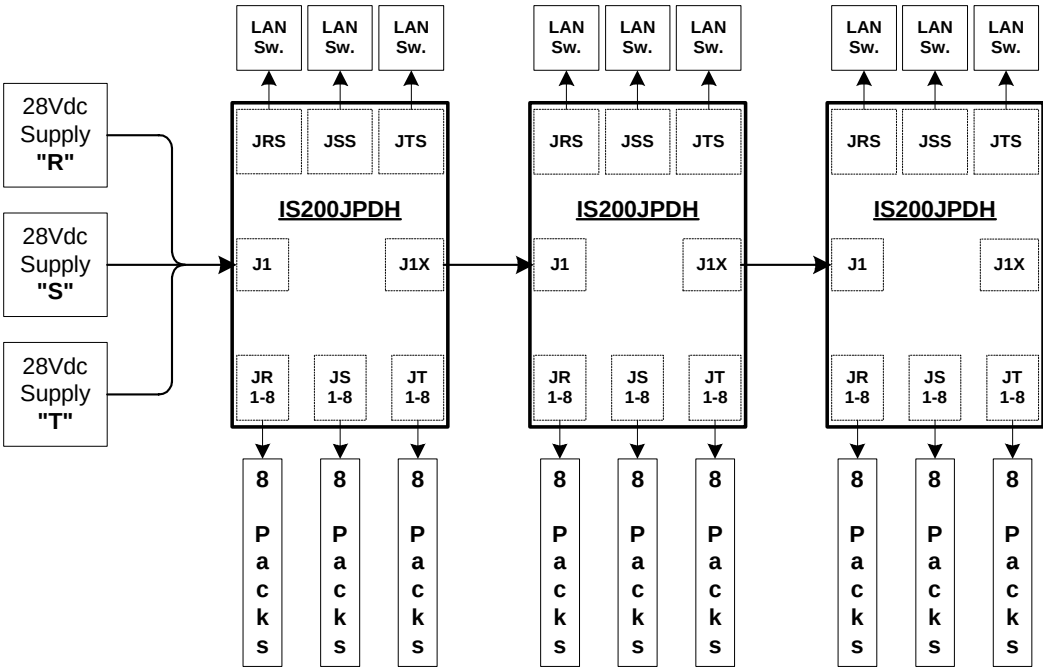
The 6-pin J1 connector brings in three separate 28 V dc feeds on three different pins for triple redundancy. The return current is common among the TMR and daisy-chain feeds and is brought in on the remaining three pins. The following figure shows how the R, S, and T 28 V dc power is distributed by JPDH to the I/O packs and Ethernet switches.



JPDH has 24 identical output circuits to provide power to the individual I/O packs. The R, S, and T feeds each provide power to eight circuits. Each I/O pack circuit includes a positive temperature coefficient fuse device for branch circuit protection. The board also has three identical unfused output circuits to provide power to each Ethernet switch.



The following figure shows an example application with 72 I/O packs and nine Ethernet switches powered through three daisy-chained JPDH boards.



JPDH Application Example

### Specifications

| Item              | Description                                                                            |                         |
|-------------------|----------------------------------------------------------------------------------------|-------------------------|
| Inputs            | One 6-pin connection for 28 V dc power input                                           | Mate-N-Lok 600 V, 13 A  |
| Outputs           | Three 2-pin connections for Ethernet switches                                          | Mate-N-Lok 600 V, 13 A  |
|                   | Twenty-four 2-pin connections for I/O packs                                            | Mate-N-Lok 600 V, 0.8 A |
| Output fuses      | 1.6 A positive temperature coefficient fuse or equivalent on each I/O pack output      |                         |
| Temperature       | -30 to +65°C (-22 to +149 °F)                                                          |                         |
| Relative humidity | 5 – 95% non-condensing                                                                 |                         |
| Safety standards  | UL 508A Safety Standard Industrial Control Equipment                                   |                         |
|                   | CSA 22.2 No. 14 Industrial Control Equipment                                           |                         |
|                   | EN 61010-1 Safety of Electrical Equipment, Industrial Machines (Low Voltage Directive) |                         |
| Board Size        | 15.875 cm high x 10.795 cm wide (6.25 in x 4.25 in)                                    |                         |
| Mounting          | DIN-Rail, card carrier mounting                                                        |                         |
|                   | Base mounted steel bracket, 4 holes                                                    |                         |

### Diagnostics

There are no diagnostic features on this board.

### Configuration

There are no jumpers or hardware settings on this board.

# JPDL Local Pack dc Power Distribution

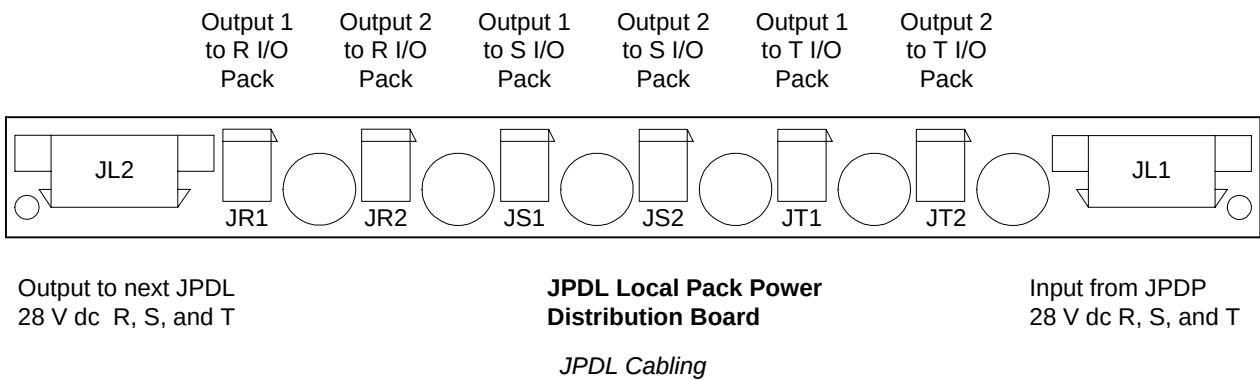
## Functional Description

The Local Pack dc Power Distribution (JPDL) board provides dc power distribution between the source of control power (possibly JPDP or JPDS) and multiple I/O packs, as well as provides daisy chain style connections for multiple downstream JPDL boards. Branch circuit protection is provided for each I/O pack connection with positive temperature coefficient fuse devices.

The board is designed to make it easy to maintain up to three isolated control power distribution circuits to complement control hardware redundancy. In a TMR system, it will be common to have separate control power for R, S, and T hardware. By providing for three separate power circuits on one board JPDL allows organized separation of the control power.

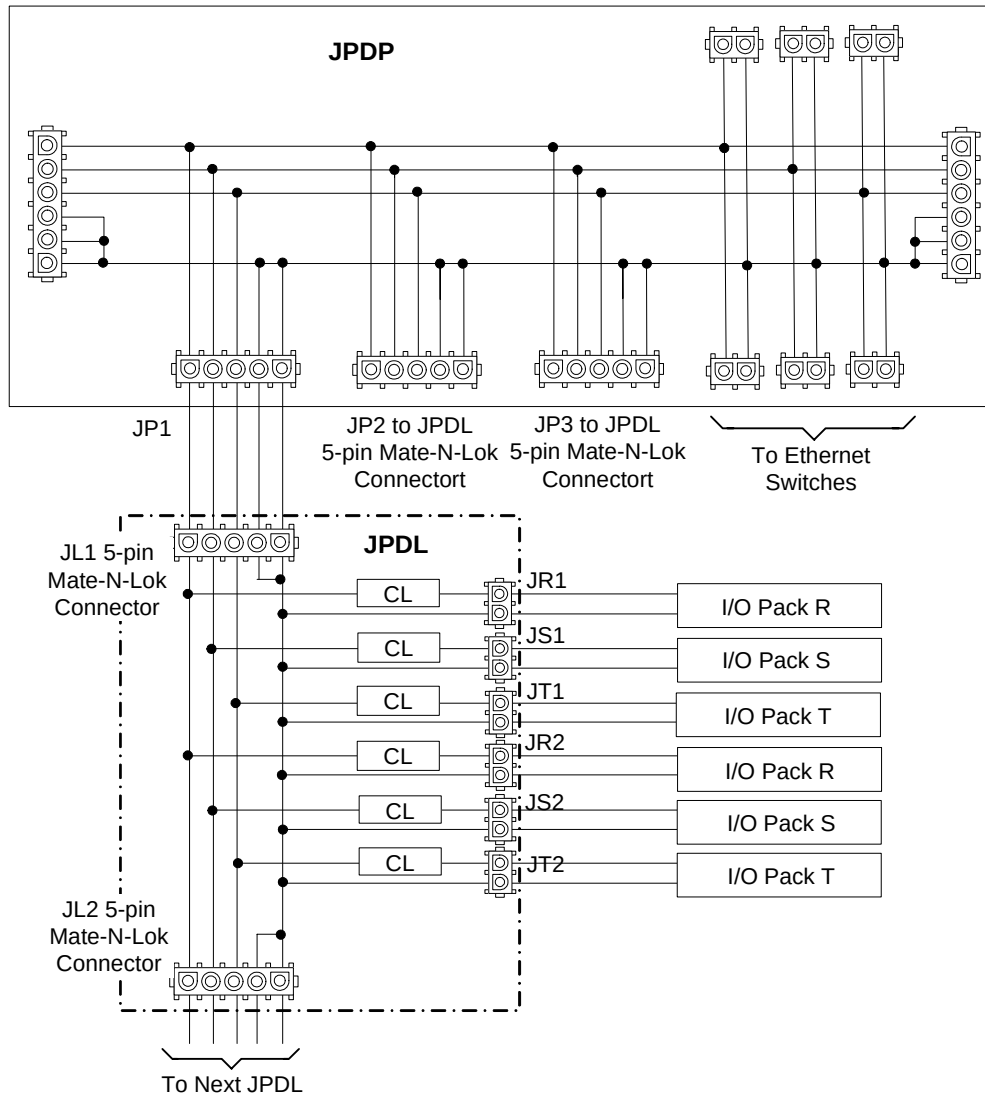
## Installation

JPDL mounts vertically on a metal bracket next to the I/O packs. Power input cables come in from the back and the output cables come out of the front. All have Mate-N-Lok<sup>®</sup> connectors. For cable destinations, refer to the circuit diagram.



## Operation

The following figure shows how the R, S, and T 28 V dc power is distributed in JPDL, and how it reaches the I/O packs. Connector JL2 is used to daisy chain power to multiple downstream JPDL boards.



*JPDL Simplified Circuit Diagram with JPDP*

## Inputs

Input power is typically 28 V dc, received from JPDP or JPDS as up to three redundant feeds. The 5-pin Mate-N-Lok input connector receives the three separate power feeds on three different pins for triple redundancy. The feeds are designated Red, Blue, and Black. The JP1, 2, and 3 connectors on JPDP provide this connection. Return current is common among the three TMR feeds and is passed on the remaining two pins of the 5-pin Mate-N-Lok connector.

## Outputs

Six identical output circuits provide power feeds to individual I/O packs. Two are sourced from each of the R, S, and T feeds (red, blue, and black). Each of the six I/O pack feeds includes a re-setting positive temperature coefficient fuse device, labeled CL (current limit) to provide branch circuit protection that is coordinated with the wire between JPDL and the I/O pack.

## Specifications

| Item             | Description                                                                                                                                                                                       |                                                      |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|
| Inputs           | One 5-pin connection with three separate 28 V dc power feeds                                                                                                                                      | red, blue, black, and return                         |
| Current          | Three power traces will each take 7.5 A continuous                                                                                                                                                | Each trace will take 15 A max. peak                  |
| Outputs          | Six 2-pin connections for I/O packs<br>Each one with positive temperature coefficient fuse protection to 2 A<br>One 5-pin connection with three separate 28 V dc power feeds to downstream JPDLs. | 2 red, 2 blue, 2 black<br>red, blue, black, & return |
| Temperature      | -30 to +65°C (-22 °F to +149 °F)                                                                                                                                                                  |                                                      |
| Safety Standards | UL 1604, for use in Class I, Division 2 potentially hazardous environments.                                                                                                                       |                                                      |
| Board Size       | 29.21 cm high x 2.54 cm wide (11.5 in x 1.0 in)                                                                                                                                                   |                                                      |
| Mounting         | Three mounting holes                                                                                                                                                                              |                                                      |

## Diagnostics

No diagnostic features are provided on this module.

## Configuration

There are no jumpers or hardware settings on the board.

---

## JPDM Power Distribution

### Functional Description

The Power Distribution (JPDM) board receives 28 V dc input power from external ac/dc or dc/dc converters and distributes power to the control system. JPDM provides fuse protection for all outputs. JPDM integrates into the PDM system feedback through the PPDA I/O pack.

JPDM is designed to maintain three separate power buses for R, S, and T applications. Jumpers can be used to provide a single bus with redundant supplies. Two adjacent JPDM boards can be wired together.

### Compatibility

The IS200JPDM board is compatible with the feedback signal P1/P2 connectors on JPDB, JPDE, and JPDE leading to a PPDA I/O pack. The DC-62 connector on JPDM is compatible with the IS220PPDA I/O pack.

## ***Installation***

The JPDM is base-mounted vertically on a metal bracket in a cabinet used by the PDM. Refer to the wiring diagrams for power input and output. There is a 50-pin diagnostic connector, P1/P2, mounted on the top and bottom of the board.

## ***Grounding***

The IS200JPDM board is grounded through the sheet metal bracket to the underlying back base. In most cases, this is the system FE.

## ***Physical Arrangement***

JPDM accepts power from cables and distributes it to the JR, JS, and JT connectors. JPDM, when hosting a PPDA I/O pack, will be mounted so indicator lights on the pack are easily visible. Two JPDM boards, when used together, will be mounted so that all terminal board connections are easily accessible. The location of JPDM is not critical in a panel. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 optionally receives feedback from another power distribution board and passes the signals out of P1 towards the PPDA. If a feedback cable connection from JPDM P2 to another power distribution board is used, consideration should be given to the feedback cable routing.

## ***Application Notes***

The internal wiring is designed so that three independent 28 V dc power buses can be maintained, or all three can be combined into a single internal bus. Each bus is sized to handle 25 A. They share a common ground sized for 75 A. With three supplies, it is possible to operate R, S, and T controllers and their I/O from separate power supplies. Failure of a supply can cause its controller and I/O to go offline while not affecting the other two channels. There is a dedicated 28 V power output for the PPDA I/O pack ensuring power system feedback is available in the event of a channel power failure.

A second method of operation has jumpers placed between the R, S, and T 28 V bus connection screws on TB1 and TB2. The board then provides a single highly reliable source of 28 V. Up to three supplies could power this bus with parallel operation capability designed into the external supplies.

The screw terminals can be used to parallel the power buses from two adjacent JPDM boards. Features offered by two boards include:

- Two sets of control rack output for Duplex or TMR applications using redundant supplies in the control racks, or systems where more than three supplies are to be paralleled
- Six JPDP outputs instead of three
- Separated R, S, and T power can have two input power supplies providing supply redundancy on each bus.

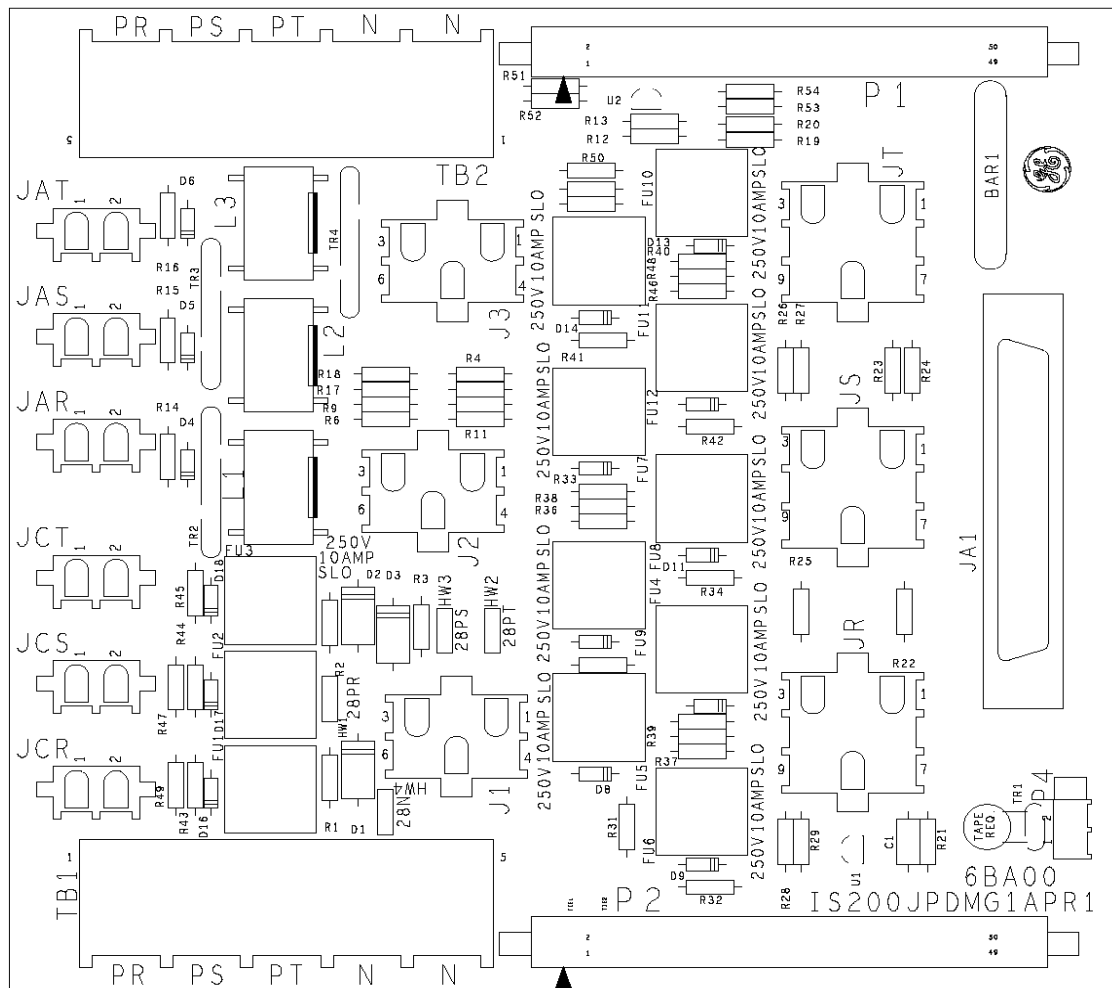
In some applications, it could be desirable to apply a battery bus as a power backup. It is possible to use a grounded battery system as input to this board using the screw terminals on the end of the board. This requires diodes not on JPDM to provide isolation between the battery and internal bus, because the JPDM is not designed to function as a battery charger.

During installation or repair, any configuration performed through the barrier terminal strips must match system documentation.

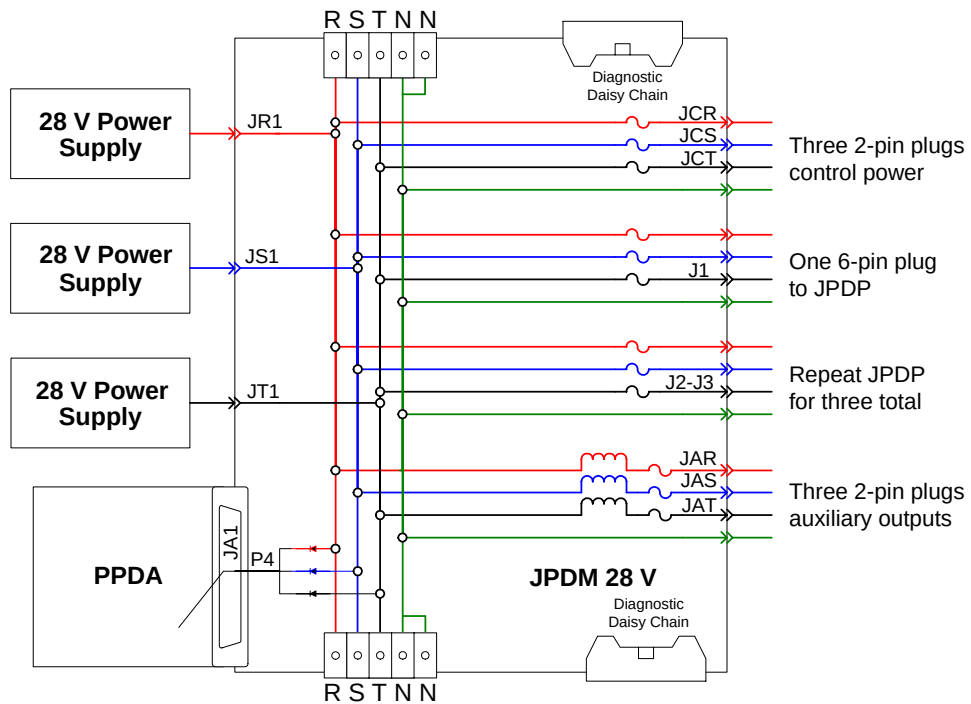
## Operation

The following I/O characteristics apply to the JPDM module:

- JDPM supplies three power supply inputs on JR, JS, and JT. Each connector uses pins 8 and 9 for positive 28 V dc and pins 1-3 for 28 V dc return providing 24 A steady state capacity. These connectors include low-level signals capable of monitoring status switches on each supply and sending feedback signals to PPDA. Pin 4 provides +10 V dc wetting to the status switch and return is on pin 5.
- Terminal boards TB1 and TB2 at the bottom and top of the board provide access to the three power buses. Jumpers can be used to parallel the bus between TB1 and TB2 when more than one JPDM board is used. Jumpers can also be used between terminals PR, PS, and PT to tie the positive bus terminals together when a single power bus is fed by redundant power supplies.
- Three fused two-pin Mate-N-Lok<sup>®</sup> connectors, JCR, JCS, JCT power controllers, and other loads. Pin 1 is +28 V dc and pin 2 is the return. A 10 A fuse protects the circuit.
- Three fused Mate-N-Lok connectors, J1, J2, and J3 have six pins each are provided to supply R, S, and T power to remote JPDP boards. They can also supply JPDL boards when using the proper wire harness. Pins 1 – 3 are 28 V dc return, pin 4 is +28R, pin 5 is +28S, and pin 6 is +28T. Each positive output is fused for 15 A to protect the circuits.
- A DC-62 connector, JA1, is for connecting to a PPDA I/O pack. The pack contains status feedback signals for up to six core power distribution boards.
- P4 supplies power to the PPDA I/O pack. It uses R, S, and T power using a diode-or arrangement in addition to a self-resetting fuse. This ensures the pack receives power if any of the three power buses are active.
- Two 50-pin diagnostic ribbon cable connectors, P1 and P2, are supplied on the top and bottom of the board. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2, when connected, receives feedback from another power distribution board and passes the signals out of P1 towards the PPDA.



JPDM Mechanical Board Layout



JPDM Simplified Circuit Diagram

## Specifications

| Item            | Description                                                          |                                                        |
|-----------------|----------------------------------------------------------------------|--------------------------------------------------------|
| Inputs          | Three 9-pin connections for 28 V dc Power Supply inputs              | 25 A max each                                          |
|                 | 5-screw terminal block for daisy chaining power distribution boards  | 35 A max per screw                                     |
| Outputs         | J1-J3 connections for either JPDP or JPDL boards                     | 10 A 250 V fuse per circuit, Bussmann® MDA-10 typical. |
|                 | JCR, JCS, JCT connections for controller power                       | 10 A 250 V fuse per circuit, Bussmann MDA-10 typical.  |
|                 | JAR, JAS, JAT connections, filtered and fused, for auxiliary devices | 3.75 A self-resetting fuse per circuit                 |
|                 | P4 connection for PPDA I/O pack power                                | 0.25 A max                                             |
|                 | JA1 connection for PPDA power diagnostic pack                        | ±5 V max                                               |
| Temperature     | -30 to +65°C (-22 to +149 °F)                                        |                                                        |
| Agency Approval | Class 1 Division 2 explosive atmosphere                              |                                                        |
| Board Size      | 16.51 cm High x 17.8 cm Wide (6.5 in x 7.0 in)                       |                                                        |
| Mounting        | DIN-rail mounting                                                    |                                                        |
|                 | Base mounted steel bracket                                           |                                                        |

## Diagnostics

The feedback wiring on JPDS and JPDM is different from the other PDM core boards. One JPDS or JPDM can host the PPDA I/O pack using the JA1 connector. The P1 connector is not used in this configuration because the output signals are going directly to PPDA. When a second JPDS or JPDM board is used, the P1 connector on the second board can be used for feedback into P2 of the board hosting PPDA. In both configurations, the P2 connector provides feedback signals from other core PDM boards. The following signals are created by JPDM:

- An electronic ID identifying the board type, revision, and serial number
- Three analog 28 V dc readings for the R, S, and T bus power supplies. Separate analog feedback signals are used. Accuracy is specified at ± 1% of full scale.
- Each power supply connector (JR1, JS1, JT1) has provisions for a dry contact indicating power supply status. JPDS conditions these signals and places them in the feedback signal set.
- Auxiliary Supply status feedback from downstream of the fuses provides three feedback signals to PPDA.
- Three control output fuse status signals plus nine J1 – J3 fuse output signals provide 12 feedback signals to PPDA

Due to a large signal count present on JPDM (15 fuses, 3 contacts and 3 bus voltages), a single set of board feedback signals is not adequate to transmit the signals to a PPDA I/O pack. Each JPDM consumes two sets of feedback signals out of the six available sets.

JPDS contains test rings for 28 V dc power from the three internal circuits, 28PR, 28PS, and 28PT. Each test ring has a series 10 k resistor to isolate the ring, and there is a single grounded ring 28N for the return path. These can be used to measure the 28 V dc power voltage using external test equipment.

## Configuration

There are no jumpers or hardware settings on the board.



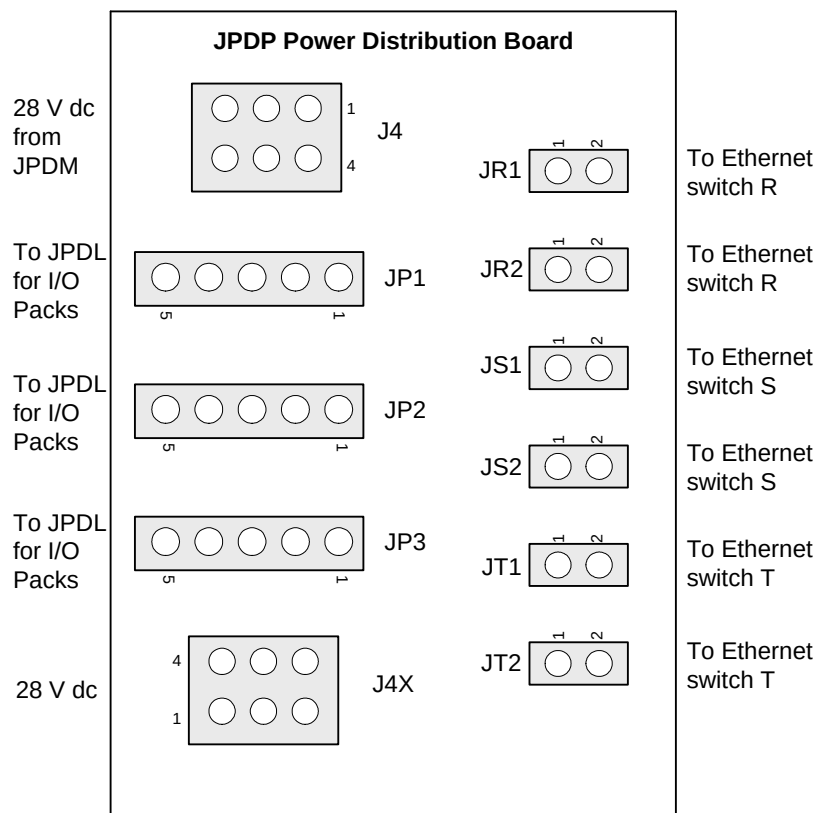
# JPDP Local Power Distribution

## Functional Description

The Local Power Distribution (JPDP) board provides intermediate 28 V dc power distribution from the JPDM board to multiple JPDL boards for further distribution to the I/O packs. JPDP also optionally provides power to Ethernet switches.

## Installation

JPDP mounts in a plastic holder, which fits on a vertical DIN-rail next to other power distribution boards. Power input and output cables have Mate-N-Lock connectors. For cable destinations, refer to the circuit diagram.

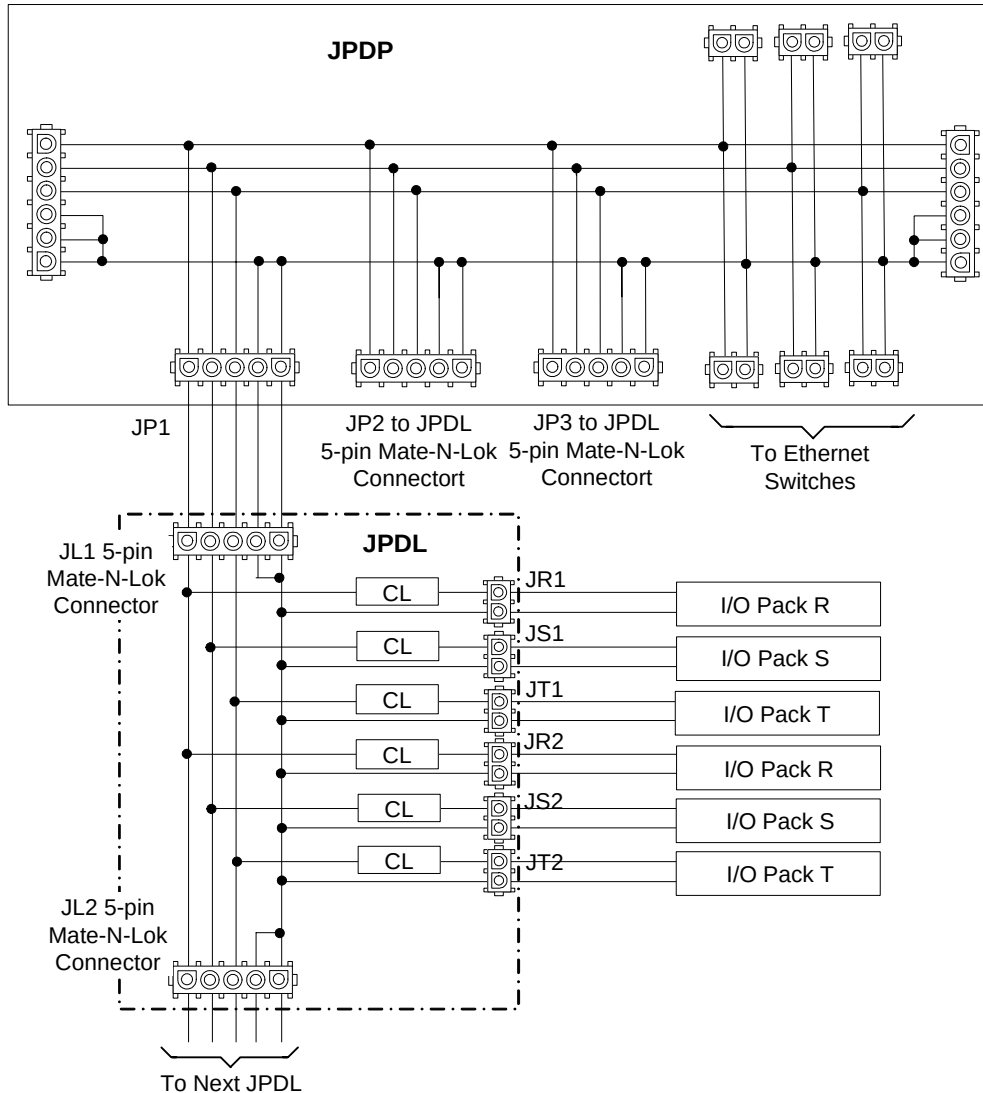


Plastic support tray for DIN-rail mounting

*JPDP Wiring and Cabling*

## Operation

The following figure shows how the 28 V dc power is distributed in JPDP, and how it reaches the I/O packs and the Ethernet switches.



*JPDP Simplified Circuit Diagram with JPDL*

## Inputs

Input power is typically 28 V dc, received from the JPDM (referred to as Pbus). The 6-pin Mate-N-Lock input connector receives three separate Pbus feeds from JPDS for triple redundancy. The feeds are designated Red, Blue, and Black.

## Outputs

Three identical output circuits provide power feeds to JPDL boards. Each JPDL output uses a 5-pin Mate-N-Lock connector. Three of the five pins are for Red, Blue, and Black. The other two pins are for Pbus return.

Six identical outputs are provided for Ethernet switches. Two connectors are dedicated to each of the three feeds (red, blue, and black).

## Specifications

| Item        | Description                                                 |                                       |
|-------------|-------------------------------------------------------------|---------------------------------------|
| Inputs      | One 6-pin connection with three separate 28 V dc Pbus feeds | Red, Blue, Black, and Return          |
| Outputs     | Six 2-pin connections for Ethernet Switches                 | 2 Red, 2 Blue, 2 Black                |
|             | Three 5-pin connections for JPDL boards, feeding I/O packs  | Each one Red, Blue, Black, and Return |
|             | One 6-pin connection with three separate 28 V dc Pbus feeds | Red, Blue, Black, and Return          |
| Temperature | -30 to +65 °C (-22 to +149 °F)                              |                                       |
| Board Size  | 15.875 cm high x 10.795 cm wide (6.25 in x 4.25 in)         | Without plastic mounting plate        |
| Mounting    | DIN-rail, card carrier mounting                             |                                       |
|             | Base mounted steel bracket, 4 holes                         |                                       |

## Diagnostics

No diagnostic features are provided on this module.

## Configuration

There are no jumpers or hardware settings on the board.

---

## JPDS 28 V Power Distribution

### Functional Description

The 28 V Power Distribution (JPDS) board receives 28 V dc input power from external ac/dc or dc/dc converters and distributes power to the control system. JPDS integrates into the PDM system feedback offered through the PPDA I/O pack.

### Compatibility

The IS200JPDS board is compatible with the feedback signal P1/P2 connectors on JPDB, JPDB, and JPDE leading to a PPDA I/O pack. The DC-62 connector on JPDS is compatible with the IS220PPDA I/O pack.

### Installation

JPDS mounts in a metal holder, which fits on a vertical DIN-rail next to other power distribution boards. Optionally, JPDS is also available with a metal holder designed for direct mounting. Refer to the wiring diagrams for power input and output routing. There is a 50-pin diagnostic connector mounted on the top and bottom of the board.

### Grounding

The IS200JPDS board is grounded through the sheet metal bracket to the underlying back base. In most cases, this can be the system FE.

## ***Physical Arrangement***

JPDS accepts power from cables and distributes it to the JR, JS, and JT connectors. JPDS, when hosting a PPDA I/O pack, is mounted so indicator lights on the pack are easily visible. Two JPDS boards, when used together, are mounted so that any terminal board connections are easily accessible. The location of JPDS is not critical in a panel. Connector P1 transmits feedback signals to a board hosting a PPDA I/O pack. Connector P2 receives feedback from other power distribution boards and passes the signals out of P1 to the PPDA. If a feedback cable connection from JPDS P2 to another power distribution board is planned, consideration should be given to the feedback cable routing.

## ***Application Notes***

The internal wiring permits either three independent 28 V dc power buses to be maintained, or all three combined into a single internal bus. Each bus is sized to handle 25 A. They share a common ground that is sized for 75 A. With three supplies, it is possible to operate R, S, and T controllers and their I/O from separate power supplies. Failure of a supply can take one controller and I/O but not affect the other two channels. There is a dedicated 28 V diode-OR power output for the PPDA I/O pack to avoid losing power system feedback in the event of a channel power failure.

A second method of operation has jumpers between the R, S, and T 28 V bus connection screws on TB1 and TB2. The board provides a single highly reliable source of 28 V. Up to three supplies could power this bus with parallel operation capability designed into the external supplies.

The screw terminals could also be used to parallel the power buses from two adjacent JPDS boards. Two boards offer the following features:

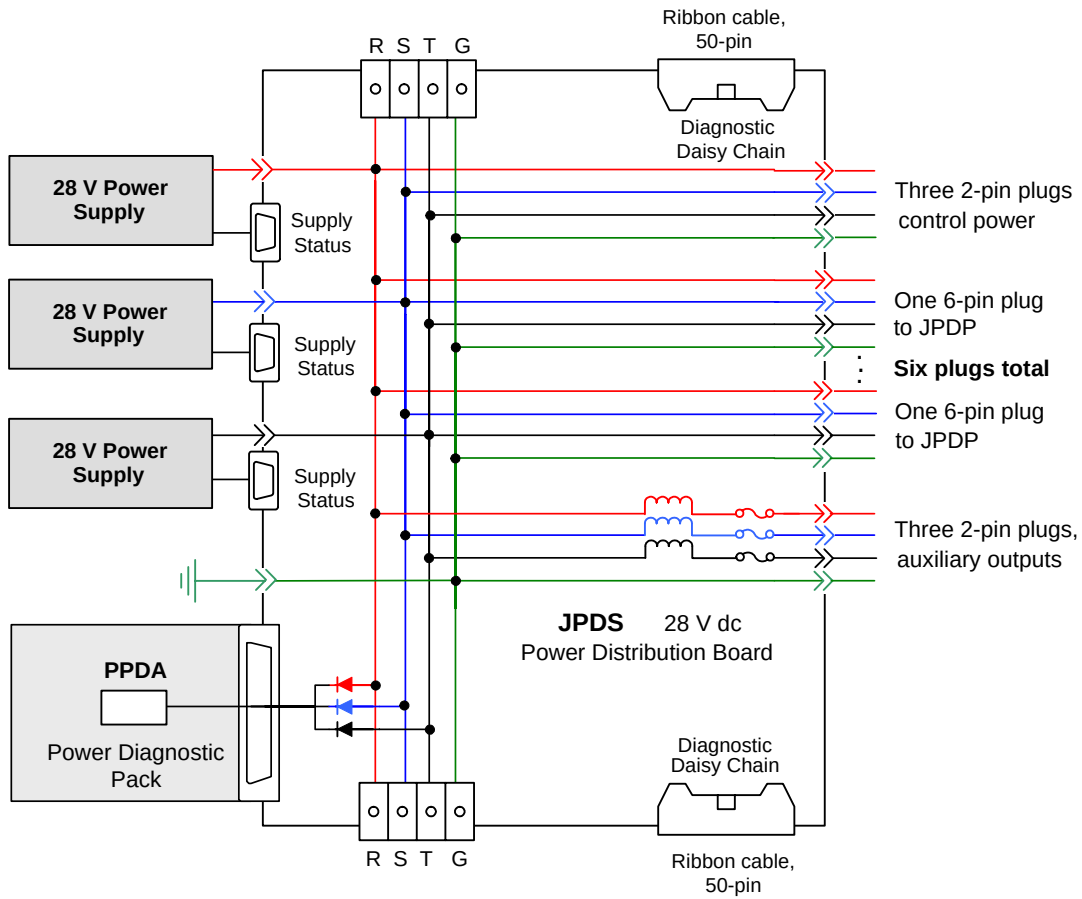
- Two sets of control rack output for Duplex or TMR applications using redundant supplies in the control racks, or systems where more than three supplies are to be paralleled
- Twelve JPDP outputs instead of six
- Separated R, S, and T power could now have two input power supplies providing supply redundancy on each bus.

In some applications, a battery bus can be applied as a power backup. A grounded battery system can also be used as input to this board using the screw terminals on the end of the board. This requires diodes not on JPDS to provide isolation between the battery and internal bus.

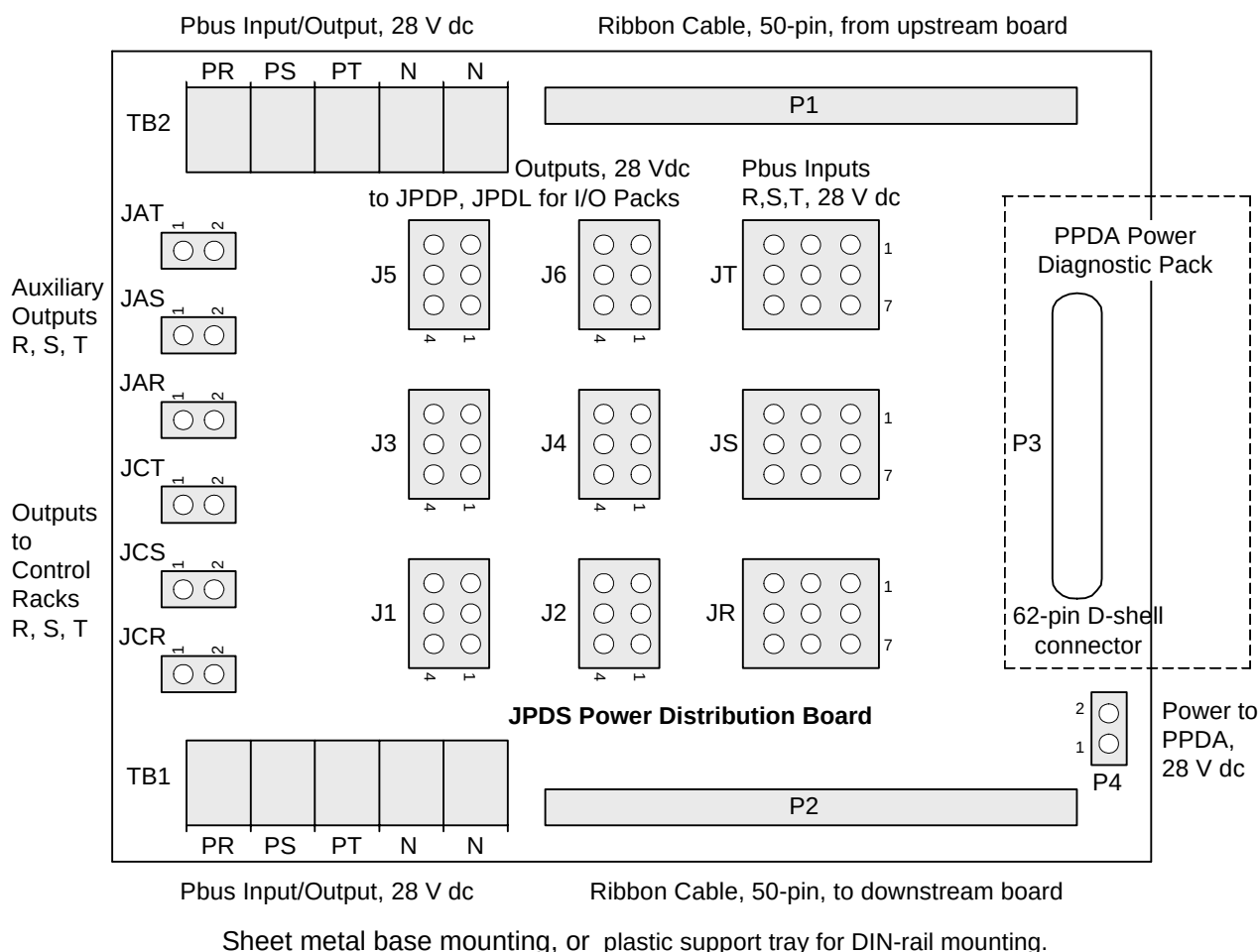
During installation or repair, any configuration performed through the barrier terminal strips must match system documentation.

## Operation

The JPDS is the power distribution board that receives 28 V dc power from the selected supplies and distributes it to the JPDP boards (for power to the I/O packs) and to the control racks. The normal 28 V power input to JPDS is through JR, JS, JT connectors.



*JPDS Simplified Circuit Diagram*



*JPDS Mechanical Board Layout*

The JPDS I/O characteristics are as follows:

- Three 28 V power input connectors, JR, JS, JT. The connectors on the power supplies have two connections for positive and three connections for negative power. In addition, there are three power supply health inputs each with two dry contact inputs per power source, which become diagnostic signals.
- Three DC outputs, JCR, JCS, and JCT, to control rack CPCI power supplies
- Six outputs to JPDP cards through six-pin connectors J1, J2, J3, J4, J5, J6 (3x2 Mate-N-Lok<sup>®</sup>). This is the same connector with the same pin assignments used on JPDP. It is possible to directly connect up to six JPDL boards to JPDS to supply the I/O packs.
- Three outputs JAR, JAS, JAT, to auxiliary power connectors, each with a positive temperature coefficient fuse for current limiting and containing a common-mode choke for noise suppression
- Access to the internal 28 V bus at the board top and bottom using individual screw terminals on TB1 and TB2. Screw terminals for R, S, and T are sized to handle a maximum of 35 A continuous current. These terminals can be used to jumper boards together. The screw terminal for ground is sized for 75 A.
- DC-62 connector for PPDA power diagnostic I/O pack. The PPDA monitors JPDS and up to five additional power distribution boards connected to JPDS with a 50-pin diagnostic ribbon cable.
- P28 power output, P4, diode ORed for the PPDA power diagnostic pack

## ***Specifications***

| <b>Item</b>     | <b>Description</b>                                                      |                                             |
|-----------------|-------------------------------------------------------------------------|---------------------------------------------|
| Inputs          | Three 9-pin connections for 28 V dc Power Supply inputs                 | 25 A max each                               |
|                 | One 50-pin ribbon cable with diagnostic data from upstream boards       | ±5 V max                                    |
|                 | One 5-screw terminal block for daisy chaining power distribution boards | 35 A max per screw                          |
| Outputs         | Six 6-pin connections for either JPDP or JPDL boards                    | 13 A max per pin                            |
|                 | Three 2-pin connections for CPCI control rack power                     | 12.5 A max per pin                          |
|                 | Three 2-pin connections, filtered and fused, for auxiliary devices      | 1.6 A positive temperature coefficient fuse |
|                 | One 50-pin ribbon cable with diagnostic data to downstream boards       | ±5 V max                                    |
|                 | One 5-screw terminal block for daisy chaining power distribution boards | 35 A max per screw                          |
|                 | One 2-pin connection for 28 V dc power to the PPDA pack                 | 0.25 A max                                  |
|                 | One 62-pin D-shell connection for PPDA power diagnostic pack            | ±5 V max                                    |
| Temperature     | -30 to +65°C (-22 to +149 °F)                                           |                                             |
| Agency approval | Class 1 Division 2 explosive atmosphere                                 |                                             |
| Board Size      | 16.51 cm high x 17.8 cm wide (6.5 in x 7.0 in)                          |                                             |
| Mounting        | DIN-rail mounting                                                       |                                             |
|                 | Base mounted steel bracket                                              |                                             |

## ***Diagnostics***

Diagnostic signals are obtained and routed into the PPDA pack as follows:

- An electronic ID identifying the board type, revision, and serial number
- Three analog P28 voltage readings for R, S, and T bus
- Each power supply connector (JR1, JS1, JT1) has provisions for a dry contact indicating power supply status. JPDS conditions these signals and places them in the feedback signal set.
- Auxiliary Supply status feedback from downstream of the fuses provides three feedback signals to PPDA.

JPDS contains test rings for 28 V dc power from the three internal circuits, 28PR, 28PS, and 28PT. Each test ring has a series 10k resistor isolating the ring and a single grounded ring, 28N, for the return path. These can be used to measure the 28 V dc power voltage using external test equipment.

## ***Configuration***

There are no jumpers or hardware settings on the board.

---

# **JGND Shield Ground**

## ***Functional Description***

The Shield Ground (JGND) terminal board mounts along side the terminal board and provides convenient ground connections for the customer's shield drain wires.

## ***Installation***

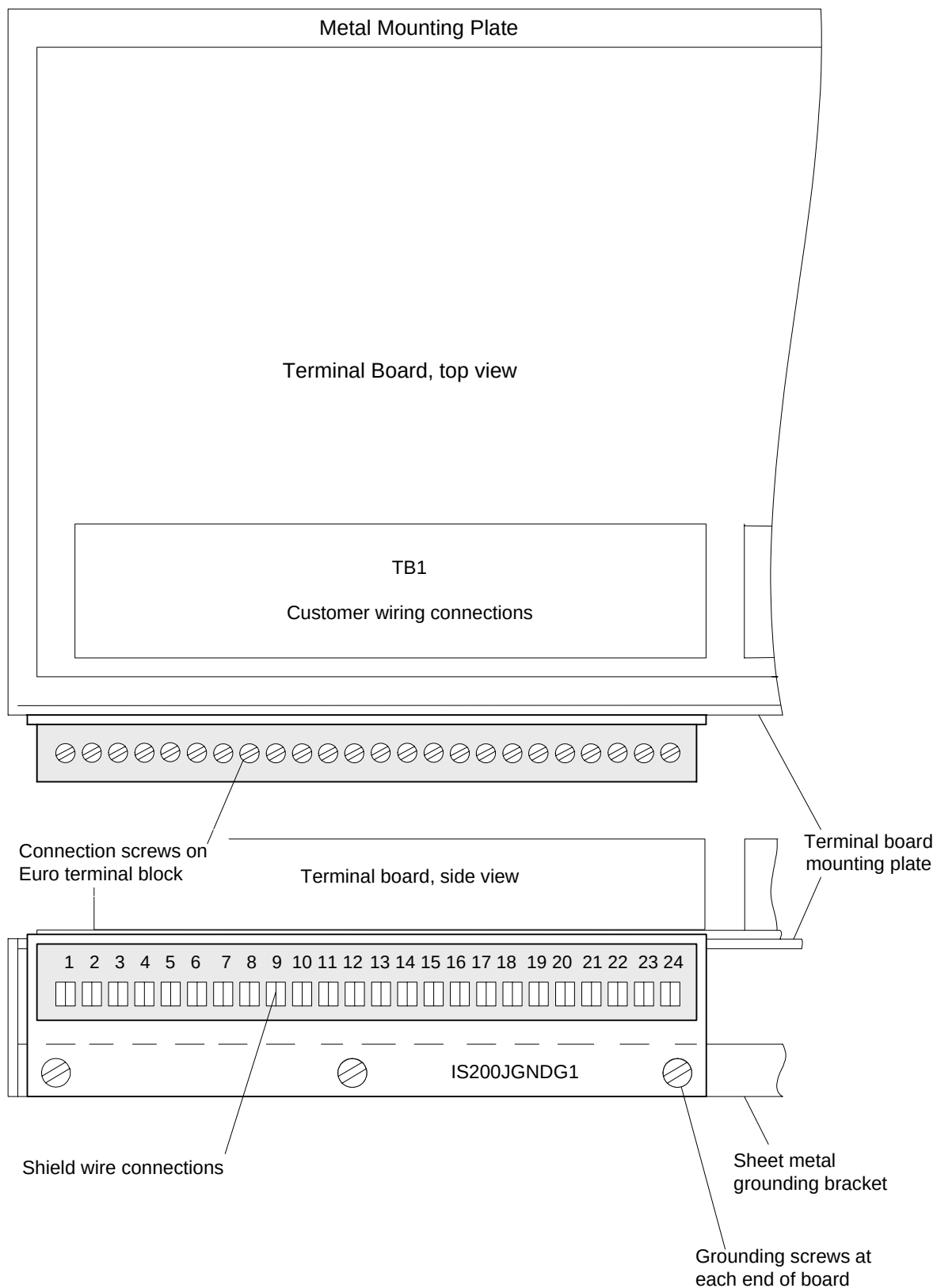
JGND mounts on a sheet metal bracket attached to the plate, which holds the terminal board. JGND is grounded to the bracket with the two screws at each end of the terminal board. The customer's shield wires connect to terminals in the Euro-type terminal block.

One or two JGND can be located on the side of the terminal board mounting bracket, for a maximum of 48 ground connections.

JGND provides a path to sheet metal ground at the board mounting screw locations. The default mechanical assembly of this board to its mount includes a nylon washer between the board and the sheet metal. This isolates JGND from the sheet metal and allows wiring of the board ground current into any desired grounding location. Removal of the washer permits conduction of the ground currents into local sheet metal and does not require any additional grounding leads.

At the time a JGND board is installed, a choice must be made to conduct ground currents through a wire to designated ground (washer present) or to conduct directly to sheet metal (washer absent). A direct connection to sheet metal is preferred. If a wire connection is used, it should be as short as possible, not exceeding 5 cm (2 in).





JGND Mounting

## ***Operation***

All 24 connectors on the Euro block are connected to ground through the two grounding screws at the ends of JGND. These make contact with the metal mounting bracket, which is connected to ground. If nylon washers are used to isolate the board, ground currents must be wired into an alternate system location.

## ***Specifications***

| Item        | Description                                                             |
|-------------|-------------------------------------------------------------------------|
| Terminals   | 24 terminals on Euro type terminal block                                |
| Temperature | -30 to +65°C (-22 to +149 °F)                                           |
| Board Size  | 3.175 cm high x 12.7 cm wide (1.25 in x 5.0 in)                         |
| Mounting    | Held with three screws to sheet metal bracket on side of terminal board |

## ***Diagnostics***

No diagnostic features are provided on this module.

## ***Configuration***

There are no jumpers or hardware settings on the board.

---

# ***Vendor Manufactured Control Power Supplies***

## ***Functional Description***

The Mark\* VIE Control uses several Vendor Manufactured Control Power Supplies (VMCPS). The features listed below are common to all the control power supplies:

- Convection cooling – no cooling fans used
- Ambient temperature range is -30°C to +65°C (-22 °F to +149 °F)
- 24, 28, and 48 V dc output has  $\pm 2\%$  voltage regulation
- Compatible with Mark VIE vibration and contamination requirements
- All power supplies have a normally open dry contact for status feedback
- Support for parallel operation without extra components. Diode equivalent is included on the output of each power supply
- Multiple supplies can load share when wired together
- Current limit and over-voltage protection of outputs
- Input filtering prevents sensitivity to input interference
- Supplies are CE marked

## Operation

### **Ac Input 150 W 28 V dc Power Supply – 342A4917P150W28**

### **Ac Input 150 W 48 V dc Power Supply – 342A4917P150W48**

The dc power supplies 342A4917P150W28 and 342A4917P150W48 provide bulk dc power to electronic loads in the Mark VIe control. Power is supplied through a 3-position terminal, Con1, mounted on the bottom of the supply. The inputs are, from left to right, ground, neutral, and line. A switch selects the input voltage range of 93 to 132 V ac or 187 to 264 V ac. The nominal selected voltage is displayed on the switch. The full load input current is rated 3 A at 115 V ac and 1.7 A at 230 V ac. The user must protect the wiring with a slow blow fuse or Type C circuit breaker. The power supply is internally protected by a 4 A, 250 V time delay fuse. In the event of ac line loss, the power supply holdup feature will maintain the output for 25 ms for 115 V ac and 30 ms for 230 V ac.

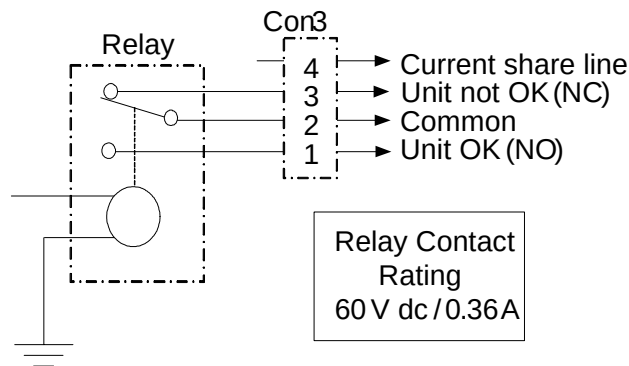


**Select the correct input voltage before applying power to prevent damage to the power supply.**

### **Caution**

Power output is through a seven-position terminal, Con3, located on the top of the supply. The terminal is clearly labeled on the side of the power supply showing all its connection points. Con2 is not used.

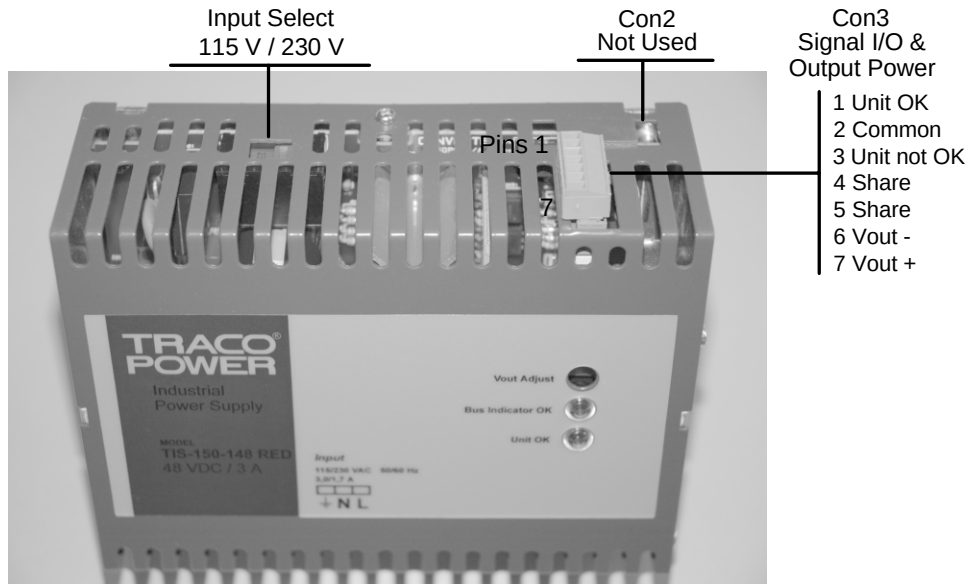
Power supply status is a dry form C relay contact rated at 0.36 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over-temperature. The relay contacts, wired to Con3, have normally open (NO) on pin 1, common on pin 2, and normally closed (NC) on pin 3. When the power supply status is OK, pin 1 to pin 2 is closed and pin 3 to pin 2 is open. Pins 1 and 2 are typically wired to a JPDS or JDPM power distribution board for feedback to the PPDM power diagnostic pack.



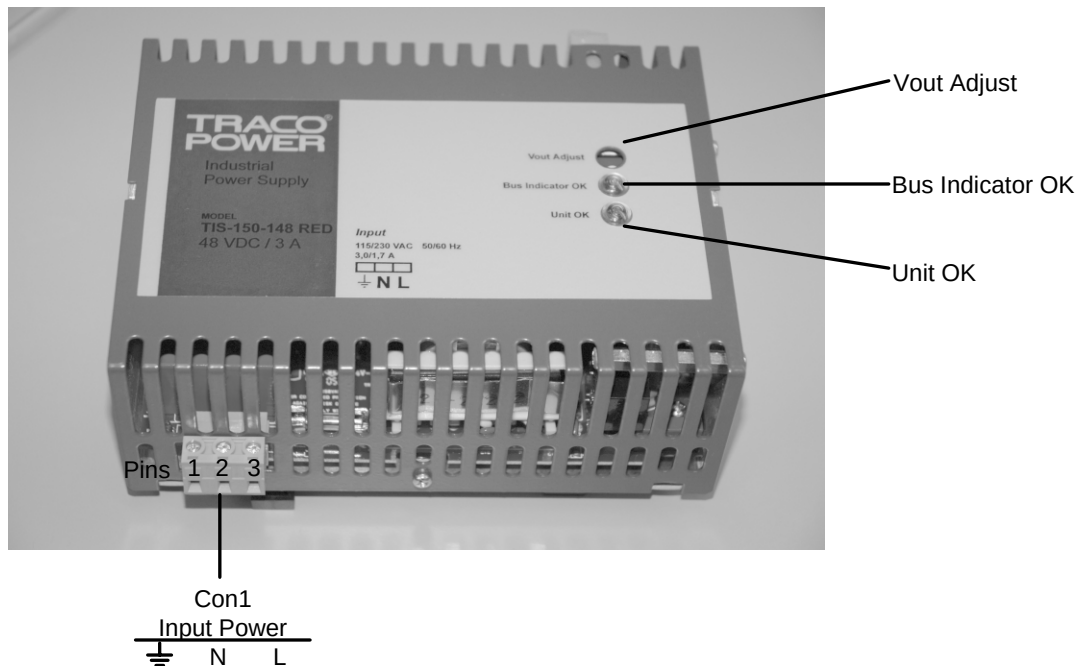
*Power Supply Relay Contacts on Con3*

Two or more power supplies of the same design can be paralleled, sharing the current equally to provide more output power. Pin 4 on Con3 provides an active load sharing signal and must be wired between power supplies to enable sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

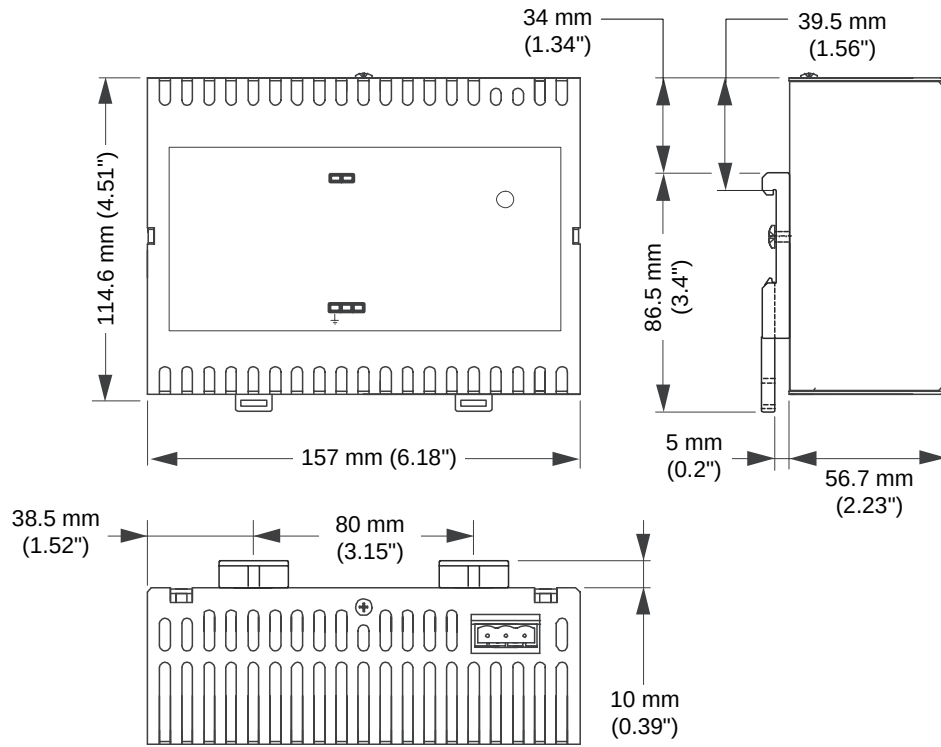
The Vout Adjust potentiometer provides adjustment of the output voltage from 24 to 32 V on the 28 V model and from 48 to 52 V dc on the 48 V model. The power supply has two indicator lamps, Bus Indicator OK and Unit OK. Bus Indicator OK lights when input power is applied. Unit OK lights when the supply is within regulation and has no over-current or over-temperature.



*Ac Input 150 W Power Supply Front View*



*Ac Input 150 W Power Supply Bottom View*



*Ac Input 150 W Power Supply Dimensions*

### ***Ac Input 300 W 24 V dc Power Supply – 342A4917P300W24***

### ***Ac Input 300 W 28 V dc Power Supply – 336A4940FEP01***

The dc power supplies 342A4917P300W24 and 336A4940FEP01 provide bulk dc power to electronic loads in the Mark VIe control. Power is supplied through the 3-position removable plug, Con1, mounted on the bottom of the supply. The inputs are, from left to right, ground, neutral, and line. A switch, mounted on the top of the supply, selects the input voltage range of 93 to 132 V ac or 187 to 264 V ac. The nominal selected voltage is displayed on the switch.



**Select the correct input voltage before applying power to prevent damage to the power supply.**

### ***Caution***

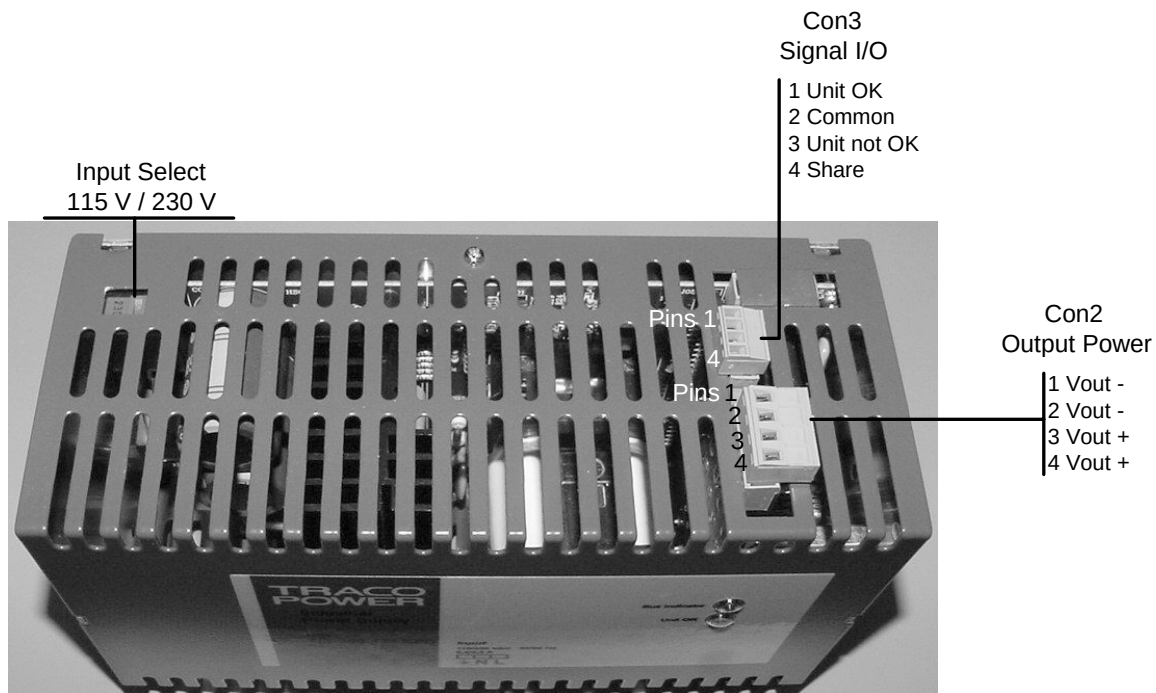
The full load input current is rated 5.4 A at 115 V ac and 3.3 A at 230 V ac. The user must protect the input wiring using a slow blow fuse or a Type C circuit breaker. The power supply is internally protected with a 6.3 A 250 V time delay fuse. In the event of ac line loss, the power supply hold up feature will maintain the output for 25 ms at 115 V ac and 30 ms at 230 V ac.

Power output is from Con2 and signal I/O is through the Con3 connector. Each connector is a removable plug. The connectors are shown in the following figure.

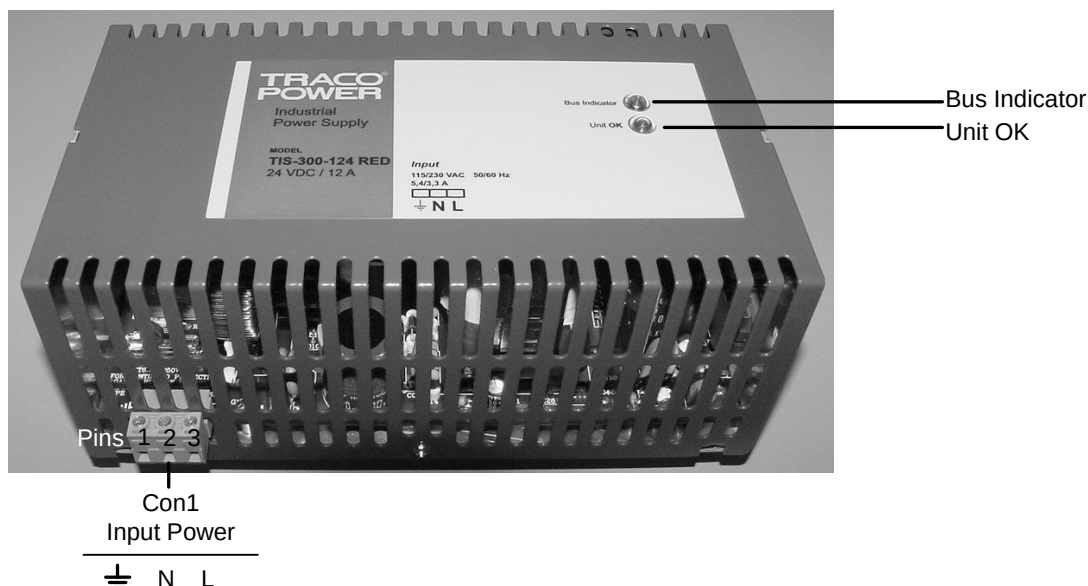
Power supply status is a dry form C relay contact rated at 3.6 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over temperature. The relay contacts, wired to Con3 have normally open (NO) on pin 1, common on pin 2, and normally closed (NC) on pin 3. When the power supply status is OK, pin 1 to pin 2 is closed and pin 3 to pin 2 is open. Con3 is a removable plug, smaller than Con1 and Con2. Con3 accepts 18G wire. Pins 1 and 2 are typically wired to a JPDS or JPDM power distribution boards for feedback to the PPDM power diagnostic pack.

Two or more power supplies of the same design can be paralleled, sharing the current equally to provide more output power. Pin 4 on Con3 provides a signal for active load sharing. Pin 4 must be wired between power supplies for load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

The Vout Adjust potentiometer provides adjustment of the output voltage from 24-32 V dc. The power supply has two indicator lamps, Bus Indicator and Unit OK. Bus Indicator lights when input power is applied. Unit OK lights when the supply is within regulation and has no over-current or over-temperature.



*Ac Input 300 W Power Supply Top View*



*Ac Input 300 W Power Supply Bottom View*

### **Ac Input 600 W 24 V dc Power Supply – 342A4917P600W24**

### **Ac Input 600 W 28 V dc Power Supply – 342A4917P600W28**

### **Ac Input 600 W 48 V dc Power Supply – 342A4917P600W48**

The dc power supplies 342A4917P600W24, 342A4917P600W28, and 342A4917P600W48 supply bulk dc power to electronic loads in the Mark VIe control. Power input is through a 3-position terminal, Con1, mounted on the top left side. The inputs are, from left to right, ground, neutral, and line. A switch selects the input voltage range of 93 to 132 V ac or 187 to 264 V ac. The nominal selected voltage is displayed on the switch. The full load input current is rated 10.5 A at 115 V ac and 6.4 A at 230 V ac. The user must protect the input wiring using a slow blow fuse or Type C circuit breaker. The power supply is internally protected by a 12 A, 250 V time delay fuse. In the event of ac line loss, the power supply holdup feature will maintain the output for 15 ms for 115 V ac, and 25 ms for 230 V ac.



**Select the correct input voltage before applying power to prevent damage to the power supply.**

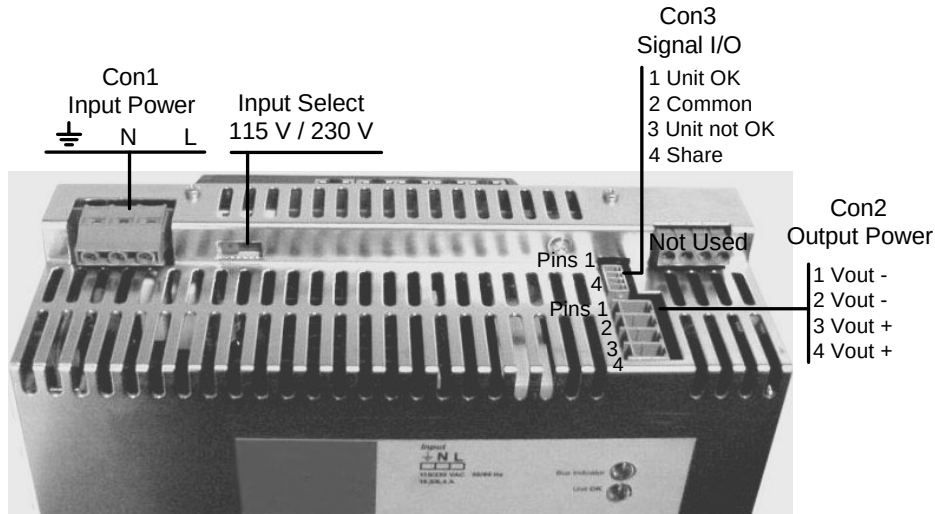
### **Caution**

Power output is through the Con2 connector. Positive dc output is on pins 3 and 4 and dc common is on pins 1 and 2.

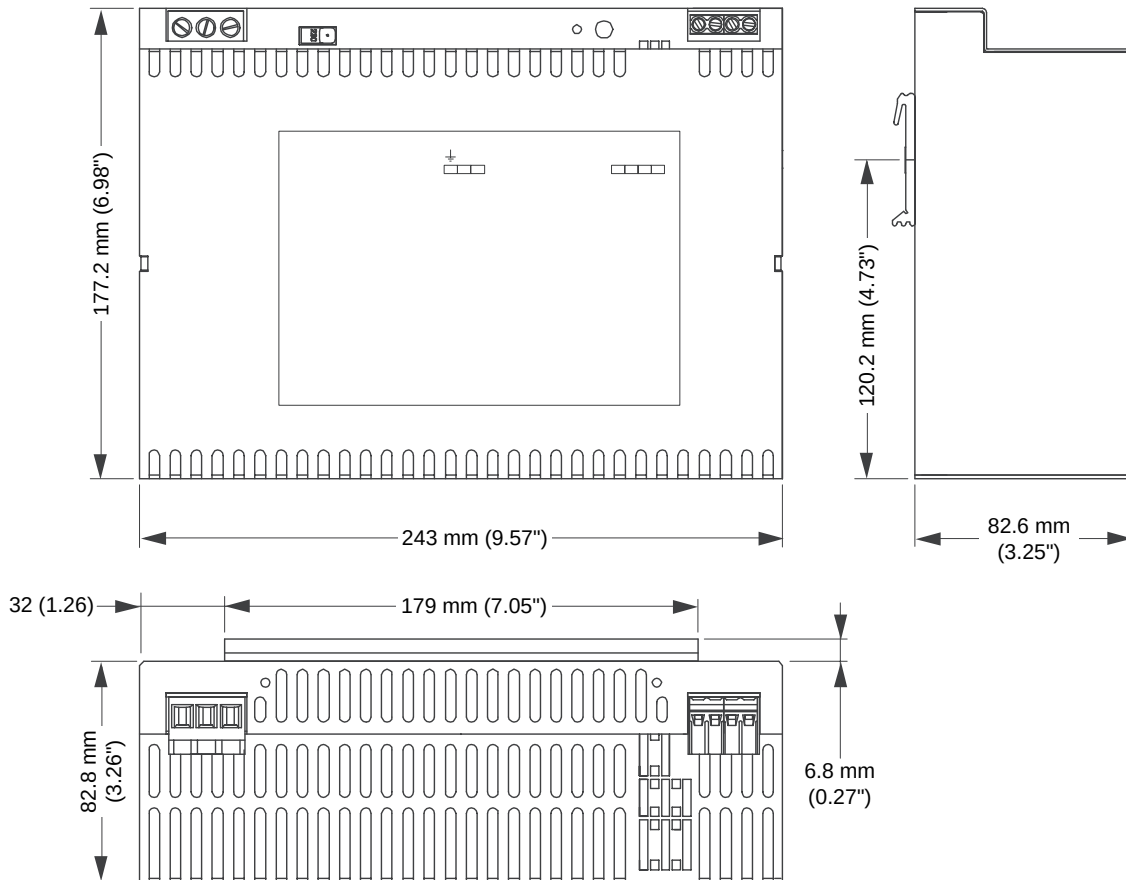
Power supply status is a dry form C relay contact rated at 3.6 A at 60 V dc. The relay indicates the output is within regulation, with no over-current, and no over-temperature. The relay contacts, wired to Con3, have normally open (NO) on pin 1, common on pin 2, and NC on pin 3. Con3 is a terminal that is smaller than Con1 and Con2. It accepts 18G wire. Pins 1 and 2 are typically wired to a JPDS or JDPM power distribution board for feedback to the PPDM power diagnostic pack.

Two or more power supplies can be paralleled, sharing the current equally to provide more output power. Pin 4 on Con3 provides a signal for active load sharing. Pin 4 must be wired between power supplies for load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

The power supply has two indicator lamps, Bus Indicator and Unit OK. Bus Indicator lights when input power is applied. Unit OK lights when the supply is within regulation and has no over-current or over-temperature.



*Ac Input 600 W Power Supply Top View*



*Ac Input 600 W Power Supply Dimensions*



## **24 V dc In/150 W 28 V dc Power Supply - 342A4922P28V150DL**

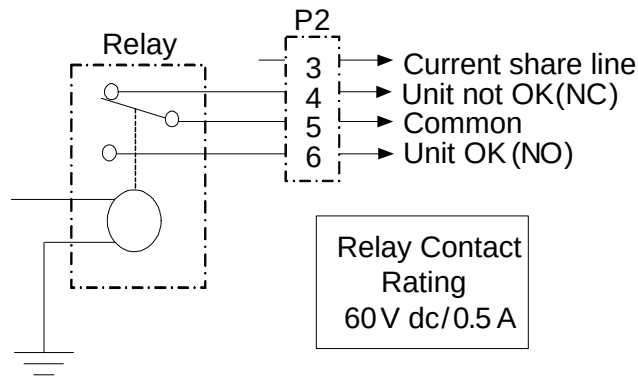
## **125 V dc In/150 W 28 V dc Power Supply – 342A4922P28V150DH**

The dc power supplies 342A4922P28V150DL and 342A4922P28V150DH, built specifically for the Mark VIe Control, provide bulk 28 V dc power to electronic loads.

Power input is through the P1 connector, a pluggable box terminal. Positive dc input is connected to pin 1, negative dc input to pin 2, and ground to pin 3. The input voltage range is 18 to 36 V dc on the 24 V dc In supply and 70 to 145 V dc on the 125 V dc In supply. The input current for the 24 V dc In power supply is 10 A at 18 V dc and 5 A at 36 V dc. This supply is internally protected with a 15 A, 125 V time delay fuse. The input current for the 125 V dc In power supply is 3 A at 70 V dc and 1.2 A at 145 V dc. This supply is internally protected with a 4 A, 250 V time delay fuse. The user must protect the input wiring using a time delay fuse or circuit breaker.

Power output is through the P2 connector, a pluggable box terminal. Positive dc output is connected to pin 1 and dc common to pin 2. The supply meets the 150 W current rating over the convection cooled temperature range of -30°C to +65°C (-22 °F to +149 °F).

Power supply status is a dry form C relay contact rated at 0.5 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over-temperature. The relay contacts, wired to P2, have normally open (NO) on pin 6, common on pin 5, and normally closed (NC) on pin 4. Pin 5 and pin 6 are typically wired to a JPDS or JDPM power distribution board for feedback to the PPDM power diagnostic pack.



*Power Supply Relay Contacts on P2*

Multiple power supplies can be paralleled, sharing current equally to provide more output power. Pin 3 on P2 provides active load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

152.2 mm (5.99")

110 mm (4.33")

90 mm (3.54")

6 Unit OK  
5 Common  
4 Unit not OK  
3 Share  
2 Vout -  
1 Vout +  
3 Ground  
2 Vin -  
1 Vin +

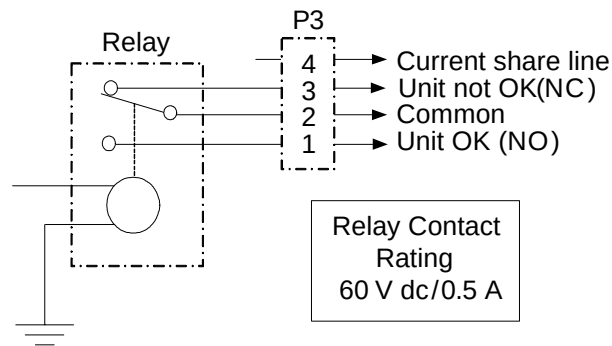


**125 V dc In/500 W 28 V dc Power Supply –  
342A4922P28V500DH**

Power is supplied through the P1 connector, a pluggable box terminal. Positive dc input is connected to pins 3 and 4, negative dc input to pins 1 and 2, and ground to pin 5. A ferrite filter is included in the input wiring to meet CE requirements. The input voltage range is 18 to 36 V dc on the 24 V dc In supply and 70 to 145 V dc on the 125 V dc In supply. The input current for the 24 V dc In power supply is 33 A at 18 V dc and 17 A at 36 V dc. This supply is internally protected with a 50 A, 300 V time delay fuse. The input current for the 125 V dc In power supply is 8 A at 70 V dc and 4 A at 145 V dc. This supply is internally protected with a 15 A, 250 V time delay fuse. The user must protect the input wiring using a time delay fuse or circuit breaker.

Power output is through the P2 connector, a pluggable box terminal. Positive dc input is connected to pins 3 and 4 and dc common to pins 1 and 2. A ferrite filter is included in the input wiring to meet CE requirements. The supply meets the 500 W current rating over the convection cooled temperature range of -30°C to +65°C (-22 °F to +149 °F).

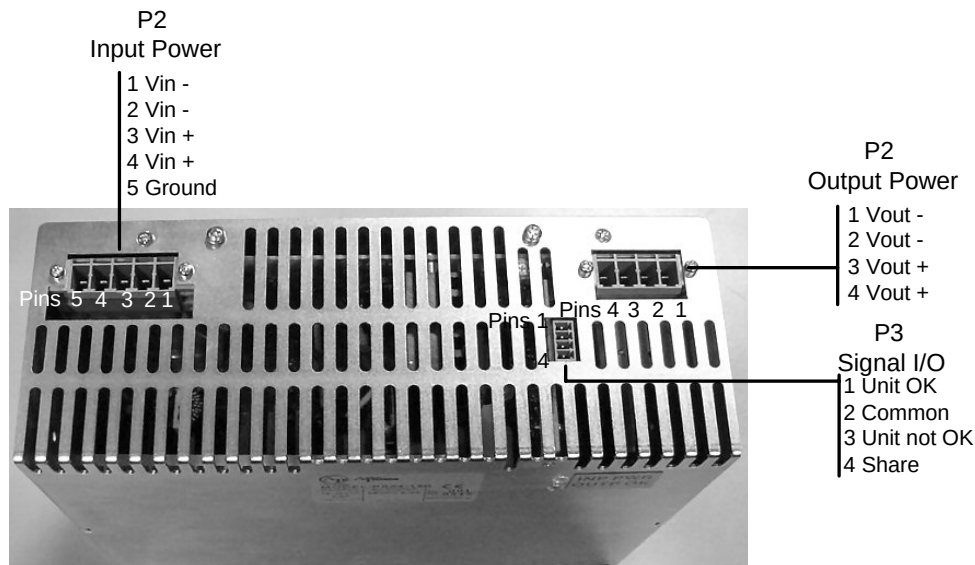
Power supply status is a dry form C relay contact rated at 0.5 A at 60 V dc. The relay indicates the output is within regulation, with no over-current and no over-temperature. The relay contacts, wired to P3, have normally open (NO) on pin 1 and common on pin 2. P3, a removable plug smaller than P1 and P2, accepts 18G wire. Pins 1 and 2 are typically wired to a JPDS or JDPM power distribution board for feedback to the PPDM power diagnostic pack.



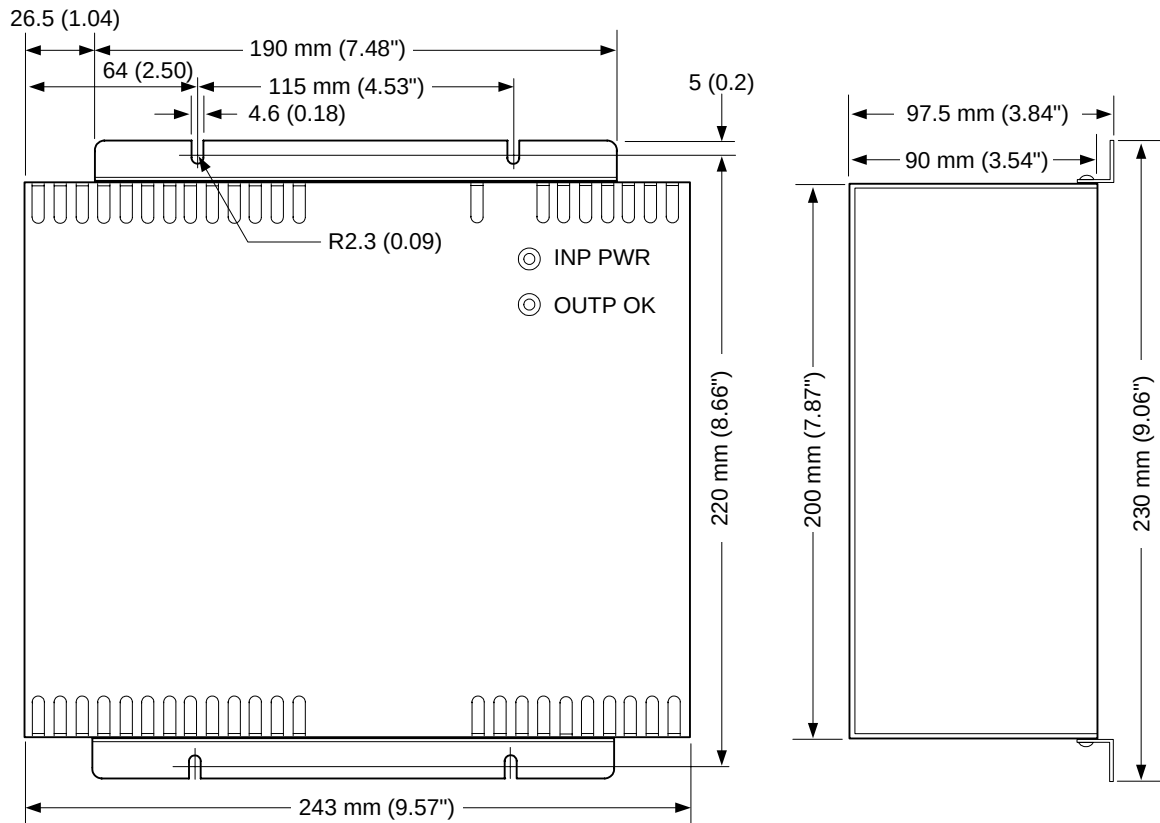
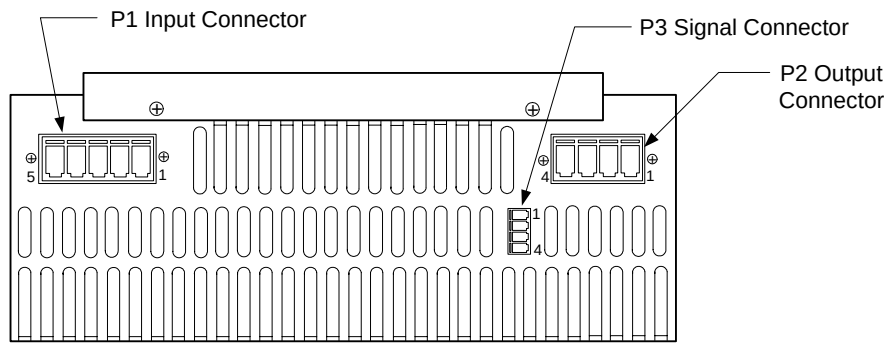
*Power Supply Relay Contacts on P3*

Multiple power supplies can be paralleled, sharing the current equally to provide more output power. Pin 4 on P3 provides a signal for active load sharing. Pin 4 must be wired between power supplies for load sharing. For accurate load sharing (within 10%), the negative outputs from all supplies must be tied together within a few feet of the supplies.

The power supply has two indicator lamps, INP PWR and OUTP OK. INP PWR lights when input power is applied. OUTP OK lights when the unit is within regulation and has no over-current or over-temperature. The status output relay shows the same status.



*Dc Input 500 W Power Supply Top View*



*Dc Input 500 W 28 V Power Supply Dimensions*

# Replacement/Warranty

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## Pack/Board Replacement

### Handling Precautions



#### Caution

To prevent component damage caused by static electricity, treat all boards with static sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation.



#### Warning

This equipment contains a potential hazard of electric shock, burn, or death. Ensure that all Lockout/Tag Out procedures are followed prior to replacing terminal boards. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

Printed wiring boards may contain static-sensitive components. Therefore, GE ships all replacement boards in anti-static bags.

Use the following guidelines when handling boards:

- Store boards in anti-static bags or boxes.
- Use a grounding strap when handling boards or board components (per previous Caution criteria).

### Replacement Procedures

System troubleshooting should be at the circuit board level. The failed pack/board should be removed and replaced with a spare.

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**Note** The failed pack/board should be returned to GE for repair. Do not attempt to repair it on site.

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#### Warning

To prevent electric shock, turn off power to the turbine control, then test to verify that no power exists in the board before touching it or any connected circuits.



#### Caution

To prevent equipment damage, do not remove, insert, or adjust board connections while power is applied to the equipment.

## ***Replacing a Pack***

### **➤ To replace the pack**

- 1** Lockout and/or tagout the field equipment and isolate the power source.
- 2** Remove the power plug located in the connector on the side of the pack.
- 3** Unplug the Ethernet cables and mark the positions of the cables to remove.
- 4** Loosen the two mounting nuts on the pack threaded shafts.
- 5** Unplug the pack and install the new pack.

## ***Replacing T-type Boards***

### **➤ To replace the board**

- 1** Lockout and/or tagout the field equipment and isolate the power source.
- 2** Check the voltage on each terminal and ensure no voltage is present.
- 3** Unplug the I/O cable (J-Plugs).
- 4** If applicable, unplug JF1, JF2 and JG1.
- 5** If applicable, remove TB3 power cables.
- 6** Loosen the two screws on the wiring terminal blocks and remove the blocks, leaving the field wiring attached.
- 7** Remove the terminal board and replace it with a spare board, check that all jumpers are set correctly (the same as in the old board).
- 8** Screw the terminal blocks back in place and plug in the J-plugs and connect cable to TB3 as before

## ***Replacing D-type Boards***

### **➤ To replace the board**

- 1** Lockout and/or tag out the field equipment and isolate the power source.
- 2** Unplug the I/O cable (J-plugs).
- 3** Disconnect all field wire and thermocouples along with shield wire.
- 4** Remove the terminal board and install the new board.
- 5** Reconnect all field wire and thermocouples as before.
- 6** Plug the I/O cable (J-plug) back.

## ***Replacing J-type Boards***

### **➤ To replace the board**

- 1** Lockout and/or tag out the field equipment and isolate the power source.
- 2** Check the voltage on each terminal to ensure no voltage is present.
- 3** Verify the label and unplug all connectors.
- 4** Loosen the two screws on each of the terminal blocks and remove the top portion leaving all field wiring in place. If necessary, tie the block to the side out of the way.
- 5** Remove the mounting screws and the terminal board.
- 6** Install a new terminal board. Check that all jumpers, if applicable, are in the same position as the ones on the old board.
- 7** Tighten it securely to the cabinet.
- 8** Replace the top portion of the terminal blocks and secure it with the screws on each end. Ensure all field wiring is secure.
- 9** Plug in all wiring connectors.

## ***Replacing S-type Boards***

### **➤ To replace the board**

- 1** Lockout and/or tagout the field equipment and isolate the power source.
- 2** Check the voltage on each terminal to ensure there is no voltage present.
- 3** Unplug the I/O cable (J-plugs)
- 4** If applicable, unplug JF1, JF2, and JG1.
- 5** If applicable, remove the TB3 power cables.
- 6** A S-type terminal board uses a Euro-style box terminal block. Gently pry the segment of the terminal block, containing the field wiring, away from the part attached to the terminal board, leaving the wiring in place. If necessary, tie the block to the side out of the way.
- 7** Remove the mounting screws and terminal board.
- 8** Install a new terminal board. Check to ensure all jumpers, if applicable, are in the same position as the ones on the old board.
- 9** Tighten it securely to the cabinet.
- 10** Slide the segments containing field wiring into the terminal block. Ensure the numbers on the segment with the field wires match the numbers on the terminal block. Press together firmly. Ensure all field wiring is secure.

## ***Replacing a BAPA Module***

### **➤ To replace the BAPA**

- 1** Lockout and/or tagout the field equipment and isolate the power source.
- 2** Unplug the HSSL Ethernet cable from the module to be removed. Cut loose any cord ties fastening the cable to the module.
- 3** Unscrew the retaining hardware on the BAPA module and remove the module.
- 4** Place the new module in the location of the old module and securely tighten retaining hardware.
- 5** Plug the HSSL Ethernet cable into the module and secure the cable.

## ***Replacing the SAMB Board***

### **➤ To replace the board**

- 1** Lockout and/or tagout the field equipment and isolate the power source.
- 2** Check the voltage on each terminal to ensure there is no voltage present.
- 3** Disconnect the power cables from P28-1 and P28-2.
- 4** Remove the BAPA module(s).
- 5** Gently pry the segments of the terminal blocks, containing the field wiring, away from the part attached to the terminal board, leaving the wiring in place. If necessary, tie the blocks to the side out of the way.
- 6** Remove the screws securing the shield ground bus, leaving the shield grounds in place. If necessary, tie the shield bus to the side out of the way.
- 7** Loosen the four mounting screws and remove the SAMB module.
- 8** Install a new IS210SAMB module. Check to ensure all jumpers are in the same position as the ones on the old board. If the new module has an attached shield ground bus, then remove the bus from the new module and discard. Securely tighten the module to the panel.
- 9** Attach the shield ground bus to the SAMB module.
- 10** Slide the segments containing field wiring into the terminal block. Ensure the numbers on the segment with the field wires match the numbers on the terminal block. Press together firmly. Ensure all field wiring is secure.
- 11** Replace the BAPA modules and reconnect the power cables to P28-1 and P28-2.



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# Renewal/Warranty

## How to Order a Board

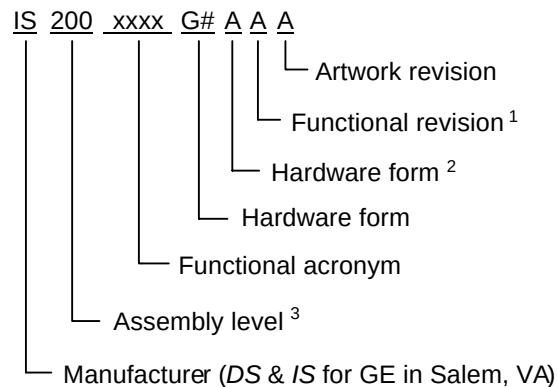
When ordering a replacement board for a GE product, you need to know:

- How to accurately identify the part
- If the part is under warranty
- How to place the order

## Board Identification

A printed wiring board is identified by an alphanumeric **part (catalog) number** located near its edge. The following figure explains the structure of the part number.

The board's functional acronym, shown below, is normally based on the **board description**, or name.



<sup>1</sup>Backward compatible

<sup>2</sup>Not backward compatible

<sup>3</sup>200 = a base-level board

215 = a higher level assembly or added components

220 = pack specific assembly

230 = a higher level module

### Board Part Number Conventions

## Placing the Order

Renewals/spares (or those not under warranty) should be ordered by contacting the nearest GE Sales or Service Office, or an authorized GE Sales Representative. Be sure to include:

- Complete part number and description
- Serial number
- Material List (ML) number

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**Note** All digits are important when ordering or replacing any board. The factory may substitute later versions of replacement boards based on availability and design enhancements. However, GE Energy ensures backward compatibility of replacement boards.

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## ***Notes***

# UCSA Stand-alone Modules

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## Mark\* Vle Controller

The Mark\* Vle UCSx controllers are a family of stand-alone computers that run the application code. The controller mounts in a panel, and communicates with the I/O packs through on-board I/O network interfaces. The controller operating system (OS) is QNX<sup>®</sup> Neutrino<sup>®</sup>, a real time, multitasking OS designed for high-speed, high-reliability industrial applications. Five communication ports provide links to I/O, operator, and engineering interfaces are as follows:

- Ethernet connection for the Unit Data Highway (UDH) for communication with HMIs, and other control equipment
- Ethernet connection for the R, S, and T I/O network
- RS-232C connection for setup using the COM1 port

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**Note** The I/O networks are private special-purpose Ethernet that support only the I/O packs and the controllers.

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The stand-alone controllers offer the following advantages over the Compact PCI and Mark Vle controllers.

- Single module
- Built-in power supply
- No jumper settings required
- No battery
- No fan
- Smaller panel footprint
- Easy access to CompactFlash<sup>™</sup>

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## Operation

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**Note** Application software can be modified online without requiring a restart.

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The controller is loaded with software specific to its application, which includes but is not limited to, steam, gas, wind, hydro, and land-marine aeroderivative (LM), or balance of plant (BoP) products. It can run rungs or blocks. The IEEE<sup>®</sup> 1588 protocol is used through the R, S, and T IONets to synchronize the clock of the I/O packs and controllers to within  $\pm 100$  microseconds.

External data is transferred to and from the control system database in the controller over the R, S, and T IONets.

In a simplex system, this includes process inputs/outputs to the I/O packs.

In a dual system:

- Process inputs/outputs to the I/O packs
- Internal state values and initialization information from the designated controller
- Status and synchronization information from both controllers

In a triple modular redundant (TMR) system:

- Process inputs/outputs to the I/O packs
- Internal state values for voting and status, and synchronization information from all three controllers
- Initialization information from the designated controller

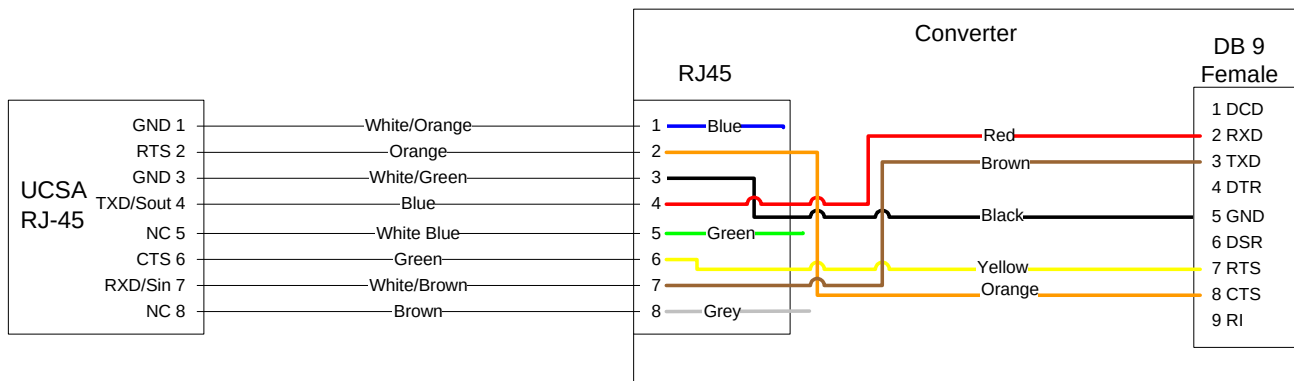
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## Configuration

The controller must be configured with a TCP/IP address prior to connecting to the UDH Ethernet. This can be achieved using one of the following methods.

- Through the ToolboxST™ application and the COM1 serial port. See *GEH-6700, ToolboxST Guide for Mark VIe Control* for details. A RJ45 to DB9 adapter is required along with an Ethernet cable. The adapter part number is 342A4944P1.
- Through the ToolboxST\* application and a CompactFlash® programmer. See *GEH-6700, ToolboxST Guide for Mark VIe Control* for details. The CompactFlash programmer can be a PCMCIA adapter or a USB device.

The following drawing shows the pin definition of the UCSx RJ45 to the COM port adapter.

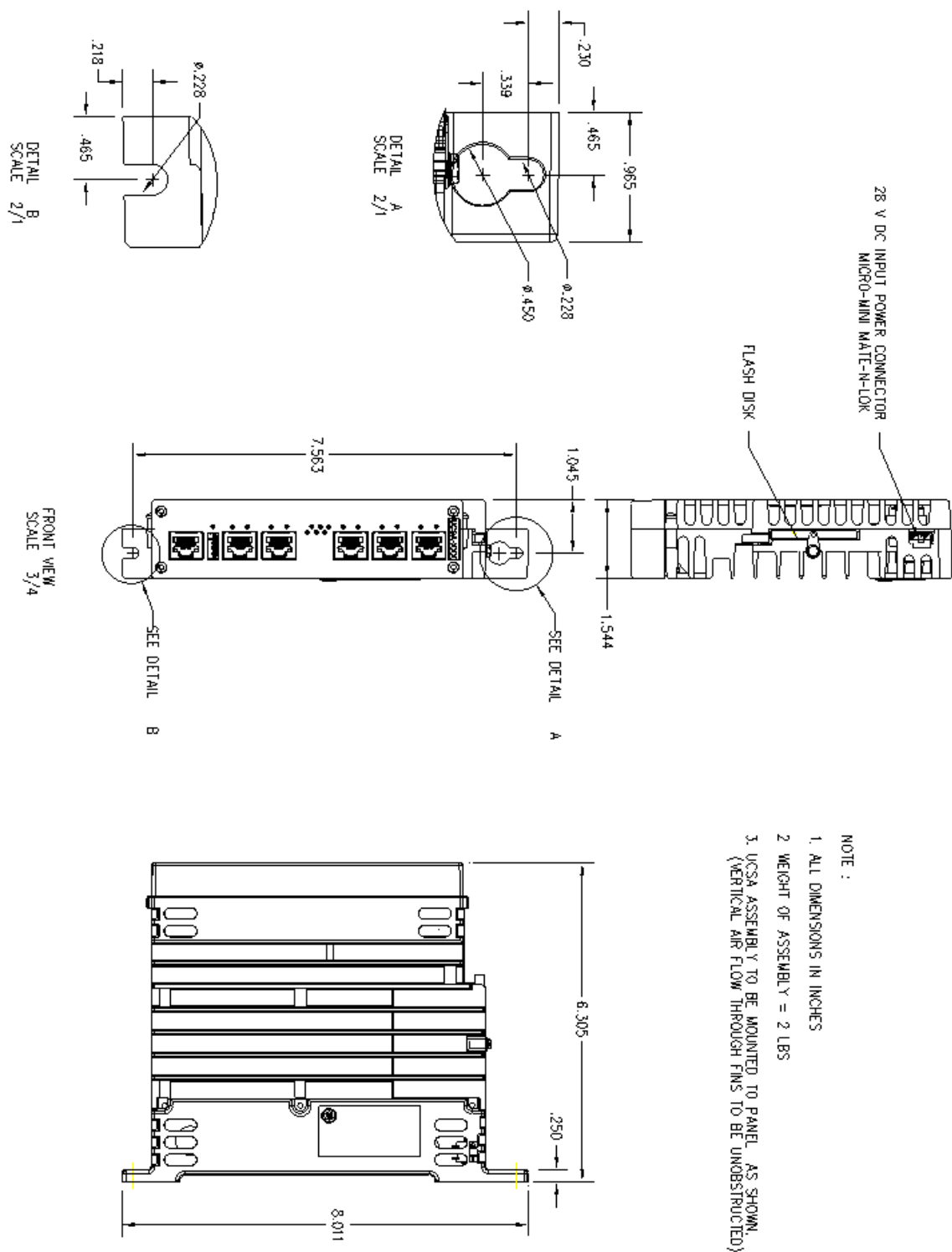


Once the IP address has been assigned, all ToolboxST configuration is through the Ethernet. See *GEH-6700, ToolboxST Guide for Mark VIe Control* for further details.

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## Installation

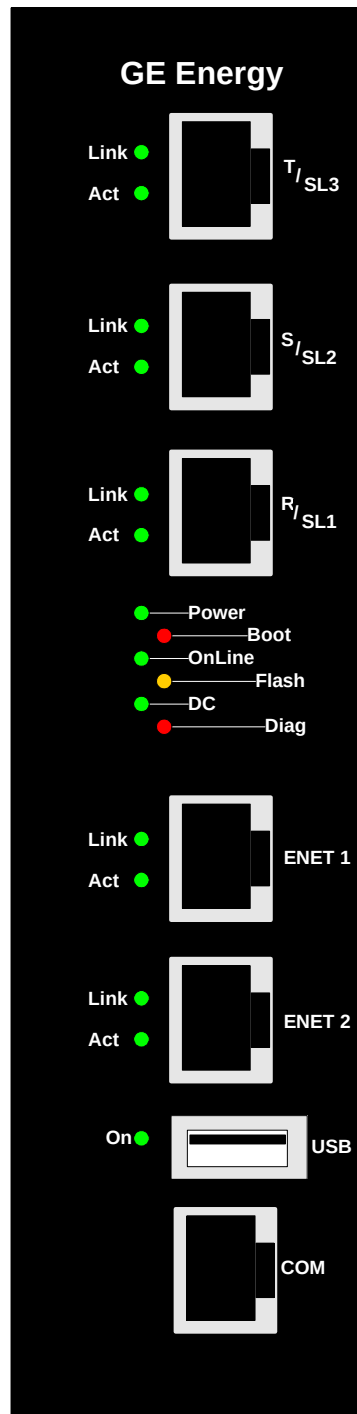
The controller is contained in a single module that mounts directly to the panel sheet metal. The following diagram shows the module envelope and mounting dimensions.



Module Envelope and Mounting Dimensions

## UCSA Module

The IS220UCSAH1+ Module contains a 667 MHz Power QUICC II Pro Freescale processor. Two 10/100BaseTX Ethernet ports provide connectivity to the UDH, and three additional 10/100Base TX Ethernet ports provide connectivity to the IONets.



UCSA Front View

## LEDs

The UCSA module has the following LEDs:

- **Link** displays solid green if the Ethernet PHY on the UCSA has established a link with an Ethernet switch port.
- **Act** indicates packet traffic on an Ethernet interface. This LED may blink if the traffic is low, but is solid green in most systems.
- **Power** displays solid Green when the internal 5 V supply is up and regulating. The UCSA converts the incoming 28 V dc to 5 V dc. All other internal power planes are derived from the 5 V.
- **Boot** displays solid red or blinking red during the boot process. The boot blink codes are described below.
  - **Online** displays solid green when the controller is online and running application code.
  - **Flash** blinks amber when any flash device is being accessed.
  - **Dc** displays solid green when the controller is the designated controller.
  - **Diag** displays solid red when the controller has a diagnostic available. The diagnostic can be viewed and cleared using the ToolboxST application.
  - **On** displays solid green when the USB is active.

## Boot LED Blink Codes

The boot LED is lit continuously during the boot process unless an error is detected. If an error is detected, the LED blinks at a 1 Hz frequency. The LED, when blinking, is on for 500 ms and off for 500 ms. The number of blinks indicates the failed state. After the blink section, the LED turns off for three seconds.

The blink codes are:

- 1: Failed Serial Presence Detect (SPD) EEPROM.
- 2: Failed to initialize DRAM or DRAM tests failed.
- 3: Failed NOR flash file system check.
- 4: Failed to load FPGA or PCI failed.
- 5: CompactFlash device not found.
- 6: Failed to start IDE driver
- 7: CompactFlash image not valid.

If the CompactFlash image is valid but the runtime firmware has not been loaded, the *boot* LED blinks continuously at a 1 Hz rate. Once the firmware is loaded, the boot LED turns off.

If the controller does not go *online*, use the ToolboxST application to determine why the controller is blocked. Once the IP address has been assigned, all the ToolboxST configuration is through the Ethernet. See *GEH-6700, ToolboxST Guide for Mark VIe Control* for further details.

## **UCSA Specifications**

| <b>Item</b>                        | <b>Specification</b>                                                                                                                                                                                                                                                                                                                                                                                             |
|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Microprocessor                     | Freescap Power pc (Power QUICC II PRO 667 MHz)                                                                                                                                                                                                                                                                                                                                                                   |
| Memory                             | 256 MB DDR SDRAM<br>Flash-backed SRAM - 8K allocated as NVRAM for controller functions<br>CompactFlash size is dependent on the application.                                                                                                                                                                                                                                                                     |
| Operating System                   | QNX Neutrino                                                                                                                                                                                                                                                                                                                                                                                                     |
| Programming                        | Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include:<br><br>Boolean<br>16-bit signed integer<br>16-bit unsigned integer<br>32-bit signed integer<br>32-bit unsigned integer<br>32-bit floating point<br>64-bit long floating point                                                                                    |
| Primary Ethernet Interface (2)     | Twisted pair 10BaseT/100BaseTX, RJ-45 connectors:<br><br>TCP/IP protocol used for communication between controller and toolbox<br>TCP/IP protocol used for alarm communication to HMIs<br>EGD protocol for application variable communication with CIMPLICITY <sup>®</sup> HMI and Series 90-70 PLCs<br>Ethernet Modbus <sup>®</sup> protocol supported for communication between controller and third-party DCS |
| IONet Ethernet Interface (3 ports) | Twisted pair 10BaseT/100BaseTX, RJ-45 connectors:<br>TCP/IP protocols used to communicate between controllers and I/O packs                                                                                                                                                                                                                                                                                      |
| COM ports                          | One accessible through RJ-45 connector on front panel<br><br>For cabling use a standard 4-pair UTP cable (for example, Ethernet cable) joined with a computer null modem connector (GE part #342A4944P1)                                                                                                                                                                                                         |
| Power Requirements                 | +32 V dc to 18 V dc ( 12.5 W (typical preliminary), TBD (maximum))                                                                                                                                                                                                                                                                                                                                               |
| Environmental Specifications       | Operating: 0 to +65°C (32 to +149 °F)<br>Storage: -40 to +85°C (-40 to +185 °F)<br>Relative humidity: 5% to 95%, no-condensing                                                                                                                                                                                                                                                                                   |
| Weight                             | 2 lbs                                                                                                                                                                                                                                                                                                                                                                                                            |



# Diagnostic Alarms

The controller detects certain system errors during startup, download, and normal operation. These diagnostic alarms can be displayed and reset from the ToolboxST application, and are recorded in historical manner on WorkstationST<sup>TM</sup>.

| Alarm | Description                                                              | Possible Cause                                                                                                                                                                       | Solution                                                                                                                                                                                                                                                                                                                                   |
|-------|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 259   | [ ] frame overruns have occurred                                         | Runtime sequencer malfunction. One or more frame overruns, which occur when frame idle time is 0, detected.                                                                          | Replace processor module.                                                                                                                                                                                                                                                                                                                  |
| 260   | [ ] frame number skips have occurred                                     | Runtime malfunction. Frame number skips have been detected. (Other than during frame synchronization during startup, the frame number should monotonically increase until rollover.) | Same as above                                                                                                                                                                                                                                                                                                                              |
| 279   | Sys - Could not determine platform type from hardware                    | Incorrect firmware version or hardware malfunction The firmware could not recognize the host hardware type.                                                                          | Ensure all connectors are aligned properly and fully seated. Check firmware version for compatibility with platform; if OK, replace processor module.                                                                                                                                                                                      |
| 280   | Sys - Platform hardware does not match runtime application               | The platform type identified in the application configuration does not match the actual hardware.                                                                                    | Fix platform type in the ToolboxST application, rebuild and download application.                                                                                                                                                                                                                                                          |
| 281   | Sys - FPGA not programmed due to platform errors                         |                                                                                                                                                                                      | Replace processor module                                                                                                                                                                                                                                                                                                                   |
| 282   | Sys - Unable to initialize application independent processes             | Runtime malfunction. An application-independent firmware process could not be started successfully.                                                                                  | Reload firmware and application and reboot. For controller, if failure persists remove CompactFlash module and reprogram boot loader using the ToolboxST application. Download Flash Bootloader pick. After reinstalling the flash module and rebooting, reload firmware and application. If this does not work, replace processor module. |
| 283   | Sys - Process disconnected illegally.                                    | Runtime or hardware malfunction. A runtime process has crashed.                                                                                                                      | Same as above                                                                                                                                                                                                                                                                                                                              |
| 284   | Process fault detected.                                                  | Same as above                                                                                                                                                                        | Same as above                                                                                                                                                                                                                                                                                                                              |
| 292   | A seq client did not respond to an overrun event prior to the next frame | Excessive application loading.                                                                                                                                                       | Check application loading and reduce the amount of application code or frequency of execution.                                                                                                                                                                                                                                             |
| 294   | Controller CPU over temperature, Temp [ ] °C, Threshold [ ] °C           | Fan loss, excessive ambient temperature, hardware malfunction.                                                                                                                       | Check fan, ambient temperature, dust buildup on processor module; if OK, replace processor module.                                                                                                                                                                                                                                         |
| 300   | Application code load failure                                            | Invalid application configuration, firmware or hardware malfunction.                                                                                                                 | Rebuild and download application to all processors; reload firmware and application; replace processor module.                                                                                                                                                                                                                             |
| 320   | Alarm - scan buffers full. Alarm process can miss alarm transitions      | Too many alarm variables are changing state too quickly to transmit all transitions. Excessive alarms in queue.                                                                      | If possible, reduce the number of alarms that can change state at the same time, for example, filter alarm variables in the application code.                                                                                                                                                                                              |

| Alarm | Description                                                                 | Possible Cause                                                                                                                                                                                                                                                      | Solution                                                                                                                                                                                                           |
|-------|-----------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 321   | Alarm - not scanning. Application stopped sending Data                      | Runtime malfunction. Alarms not being scanned. Processor will likely reboot on a S/W watchdog timeout due to a processor overload.                                                                                                                                  | If processor does not reboot, condition was transient. Clear alarm and monitor for repeat occurrences, which may indicate spurious processor overloads. Check idle time and reduce application load, if necessary. |
| 322   | EGD configuration >1400 bytes, may not be supportable by fault tolerant EGD | Number of relevant, consumed UDH EGD variables exceeds fault tolerant EGD limitation. Normal UDH EGD operation is not affected; however, in the event of a UDH EGD failure, some consumed variables may not be transmitted to redundant controllers over the IONet. | Reduce amount of relevant, consumed UDH EGD data.                                                                                                                                                                  |
| 323   | Received request to send fault tolerant EGD data to redundant controllers   | Redundant processor unable to receive UDH EGD inputs and has requested that EGD data be transferred over the IONet. An EGD exchange timeout has occurred on the requesting processor.                                                                               | Check UDH network and verify that all redundant processors are receiving all of the expected EGD exchanges. Ensure that all relevant devices are powered up and producing data on the network.                     |
| 324   | Requested fault tolerant EGD data from redundant controllers                | Unable to receive UDH EGD inputs and the exchange data is being requested over the IONet.                                                                                                                                                                           | Same as above                                                                                                                                                                                                      |
| 326   | Communication lost from R processor                                         | IONet or hardware malfunction. The S or T processor in a redundant system has lost communication with the R processor.                                                                                                                                              | Verify that the processor is in the Controlling state. Check for disconnected IONet cables or malfunctioning switches. Rebuild and download application.                                                           |
| 327   | Communication lost from S processor                                         | IONet or hardware malfunction. The R or T processor in a redundant system has lost communication with the S processor.                                                                                                                                              | Same as above                                                                                                                                                                                                      |
| 328   | Communication lost from T processor                                         | IONet or hardware malfunction. The R or S processor in a redundant system has lost communication with the T processor.                                                                                                                                              | Same as above                                                                                                                                                                                                      |
| 329   | Data initialization timeout R processor                                     | IONet malfunction, controllers have different application revisions, one or more controllers are powered down, or controller is overloaded by external command messages. Controller unable to complete startup data initialization.                                 | Check IONets; rebuild and download application, ensure all controllers are powered up, disable jabbering command senders (for example, Modbus masters) until controller is online.                                 |
| 330   | Data initialization timeout S processor                                     | Same as above                                                                                                                                                                                                                                                       | Same as above                                                                                                                                                                                                      |
| 331   | Data initialization timeout T processor                                     | Same as above                                                                                                                                                                                                                                                       | Same as above                                                                                                                                                                                                      |
| 334   | Application frame number skip                                               | Hardware or IONet malfunction. Frame number skips detected. Frame number should monotonically increase until rollover; alarm occurs following a single frame number skips in successive frames.                                                                     | Check IONet (switches, cables); replace processor module.                                                                                                                                                          |
| 335   | Process code segment CRC mismatch                                           | Hardware memory failure. A modification has occurred in the code segment for one of the processes.                                                                                                                                                                  | Replace processor module.                                                                                                                                                                                          |
| 336   | Controller is unlocked                                                      | Mark VleS: Leaving Data Init control state and not locked or the controller is unlocked through the ToolboxST application.                                                                                                                                          | Lock the controllers from the ToolboxST application before executing safety functions.                                                                                                                             |

| Alarm | Description                                                | Possible Cause                                                                                                                                                                                                                                                                                                                                             | Solution                                                                                                                                                                                                                                             |
|-------|------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 337   | EGD output exchange disagreement detected                  | IONet malfunction or hardware problem. For at least one output, a difference was detected between the three controllers in a SIS. This alarm remains active until the controllers agree on all outputs. A difference for non-Boolean data generally indicates a deviation of more than 10% from the median value or no IONet EGD configuration is present. | Check IONet (switches, cables); rebuild and download application to all processors; if this does not help, replace processor module.                                                                                                                 |
| 347   | Running application does not match the branded application | Mark VIeS: Application not branded or different from branded version                                                                                                                                                                                                                                                                                       | Reload branded application to controller and I/O packs or use the ToolboxST application to brand currently running application.<br><b>Note:</b> The purpose of branding is to label a verified safety application, and to ensure that it is running. |
| 348   | Packet loss on IONet 1 exceeded [ ]%                       | Power cycled on I/O producer (controller or I/O pack), IONet malfunction, I/O message corruption. Communication errors have occurred on more than 5% of the data transmissions on IO Net.                                                                                                                                                                  | Check IONet (switches, cables); make sure alarm did not occur due to pack reboot, and so on.                                                                                                                                                         |
| 349   | Packet loss on IONet 2 exceeded [ ]%                       | Same as above                                                                                                                                                                                                                                                                                                                                              | Same as above                                                                                                                                                                                                                                        |
| 350   | Packet loss on IONet 3 exceeded [ ]%                       | Same as above                                                                                                                                                                                                                                                                                                                                              | Same as above                                                                                                                                                                                                                                        |
| 352   | Blockware app static data CRC mismatch                     | Hardware memory failure. App process data that should not change after the controller goes online was modified. This may indicate a hardware memory problem.                                                                                                                                                                                               | Replace processor module.                                                                                                                                                                                                                            |
| 353   | Sys Config Shmem CRC mismatch                              | Hardware memory failure. System process data that should not change after the controller goes online was modified.                                                                                                                                                                                                                                         | Same as above                                                                                                                                                                                                                                        |
| 354   | EGD static data CRC mismatch                               | Hardware memory failure. IONet-EGD process data that should not change after the controller goes online was modified.                                                                                                                                                                                                                                      | Same as above                                                                                                                                                                                                                                        |
| 355   | State Exchange Voter disagreement detected                 | IONet malfunction or hardware problem. State Exchange disagreement found.                                                                                                                                                                                                                                                                                  | Check IONet (switches, cables); if this does not help, replace processor module.                                                                                                                                                                     |
| 356   | NANs in CALC Block detected                                | NAN received from I/O interface or hardware problem.                                                                                                                                                                                                                                                                                                       | Check external devices that may be sending NANs to the controller; if conditions persists, replace processor module.                                                                                                                                 |
| 357   | Sequencer client out-of-order execution detected           | Hardware malfunction. Sequencer critical clients scheduled out of order. Alarm occurs following three successive frames of sequencer critical client out-of-order execution detections; after five, controller put in FAILURE control state.                                                                                                               | Replace processor module.                                                                                                                                                                                                                            |
| 358   | Sequencer client execution underrun detected               | Hardware malfunction. Sequencer critical client underrun detected. Alarm occurs after a sequencer critical client has been run slower than its nominal rate three times in a row; after five, controller put in FAILURE control state.                                                                                                                     | Same as above                                                                                                                                                                                                                                        |
| 359   | Sequencer client execution overrun detected                | Hardware malfunction. Sequencer critical client overrun detected. Alarm occurs after a sequencer critical client has been run faster than its nominal rate three times in a row; after five, controller put in FAILURE control state.                                                                                                                      | Same as above                                                                                                                                                                                                                                        |

| Alarm | Description                                                        | Possible Cause                                                                                                                                                                                                                              | Solution                                                                         |
|-------|--------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| 360   | Sequencer frame period out-of-bounds ( $\pm 5\%$ ) detected        | Hardware malfunction. Frame period greater than $\pm 5\%$ of nominal. Alarm occurs following frame period out-of-bounds condition occurring three frames in a row; after five, controller put in FAILURE control state.                     | Same as above                                                                    |
| 361   | Sequencer frame state timeout out-of-bounds ( $\pm 5\%$ ) detected | Hardware malfunction. Sequencer frame state timeout greater than $\pm 5\%$ of nominal. Alarm occurs following a sequencer frame state timeout being out-of-bounds three frames in row; after five, controller put in FAILURE control state. | Same as above                                                                    |
| 362   | Sequencer frame number skip detected                               | Hardware or IONet malfunction. Frame number skips detected. Frame number should monotonically increase until rollover; alarm occurs following three skips in a row, after five, controller put in FAILURE control state.                    | Check IONet (switches, cables); replace processor module.                        |
| 363   | Seq static data CRC mismatch                                       | Hardware memory failure. Sequencer process data that should not change after the controller goes online was modified.                                                                                                                       | Replace processor module.                                                        |
| 364   | Too many SEV disagreements in a single packet                      | IONet malfunction or hardware problem. SEV disagreement overflow. Firmware cannot handle more than 128 disagreements at once.                                                                                                               | Check IONet (switches, cables); if this does not help, replace processor module. |

**Note** So that input validation alarms can be generated for each I/O pack in a configuration, the following IONet EGD input validation alarms are numbered starting from a base of 1000, and are uniquely created based on I/O pack topology. Four error messages are associated with each alarm number, and are used based on particular validation types.

Alarm ID convention: R I/O pack in TMR module or Simplex, single-net I/O pack:  $1000 + \text{ModuleID}$ ; S I/O pack in TMR module:  $1256 + \text{ModuleID}$ ; T I/O pack in TMR module or dual-net or dual I/O pack on IONet 1:  $1512 + \text{ModuleID}$ ; dual-net or dual I/O pack on IONet 2:  $1768 + \text{ModuleID}$ .

| Alarm     | Description                                                    | Possible Cause                                                                                                   | Solution                                                      |
|-----------|----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| 1000-2024 | I/O module [ ], R pack: exch [ ] timed out, IONet [ ]          | I/O pack comm. malfunction or IONet malfunction. (R, S, or T) I/O pack input packet not received timeout.        | Check I/O pack health, diagnostics, IONet (cables, switches). |
| 1000-2024 | I/O module [ ], S pack: exch [ ] timed out, IONet [ ]          | Same as above                                                                                                    | Same as above                                                 |
| 1000-2024 | I/O module [ ], S pack: exch [ ] timed out, IONet [ ]          | Same as above                                                                                                    | Same as above                                                 |
| 1000-2024 | I/O module [ ]: exch [ ] timed out                             | I/O pack comm. malfunction or IONet malfunction. SMX I/O pack input packet not received timeout.                 | Same as above                                                 |
| 1000-2024 | I/O module [ ]: exch [ ] timed out, IONet [ ]                  | I/O pack comm. malfunction or IONet malfunction. SMX I/O pack, dual network input packet not received timeout.   | Same as above                                                 |
| 1000-2024 | I/O module [ ], R pack: exch [ ] major sig mismatch, IONet [ ] | Controller, I/O pack application mismatch. (R, S, or T) I/O pack input packet major signature mismatch detected. | Rebuild application and download.                             |
| 1000-2024 | I/O module [ ], S pack: exch [ ] major sig mismatch, IONet [ ] | Same as above                                                                                                    | Same as above                                                 |

| Alarm     | Description                                                         | Possible Cause                                                                                                           | Solution      |
|-----------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|---------------|
| 1000-2024 | I/O module [ ] , T pack: exch [ ] major sig mismatch, IONet [ ]     | Same as above                                                                                                            | Same as above |
| 1000-2024 | I/O module [ ] : exch y major sig mismatch                          | Controller, I/O pack application mismatch. SMX I/O pack input packet major signature mismatch detected.                  | Same as above |
| 1000-2024 | I/O module [ ] , R pack: exch [ ] cfg timestamp mismatch, IONet [ ] | Controller, I/O pack application mismatch. (R, S, or T) I/O pack input packet configuration timestamp mismatch detected. | Same as above |
| 1000-2024 | I/O module [ ] , S pack: exch [ ] cfg timestamp mismatch, IONet [ ] | Same as above                                                                                                            | Same as above |
| 1000-2024 | I/O module [ ] , T pack: exch [ ] cfg timestamp mismatch, IONet [ ] | Same as above                                                                                                            | Same as above |
| 1000-2024 | I/O module [ ] : exch [ ] cfg timestamp mismatch                    | Controller, I/O pack application mismatch. SMX I/O pack input packet configuration timestamp mismatch detected.          | Same as above |
| 1000-2024 | I/O module [ ] , R pack: exch [ ] received too short, IONet [ ]     | Controller, I/O pack application mismatch. (R, S, or T) I/O pack input packet received shorter than expected.            | Same as above |
| 1000-2024 | I/O module [ ] , S pack: exch [ ] received too short, IONet [ ]     | Same as above                                                                                                            | Same as above |
| 1000-2024 | I/O module [ ] , T pack: exch [ ] received too short, IONet [ ]     | Same as above                                                                                                            | Same as above |
| 1000-2024 | I/O module [ ] : exch [ ] received too short                        | Controller, I/O pack application mismatch. SMX I/O pack input packet received shorter than expected.                     | Same as above |

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## ***Notes***

# ***Glossary of Terms***

## **Glossary of Terms**

### ***application code***

Software that controls the machines or processes, specific to the application.

### ***ARCNET***

Attached Resource Computer Network. A LAN communications protocol developed by Datapoint Corporation. The physical (coax and chip) and datalink (token ring and board interface) layer of a 2.5 MHz communication network which serves as the basis for DLAN+. See DLAN+.

### ***attributes***

Information, such as location, visibility, and type of data that sets something apart from others. In signals, an attribute can be a field within a record.

### ***Balance of Plant (BOP)***

Plant equipment other than the turbine that needs to be controlled.

### ***baud***

A unit of data transmission. Baud rate is the number of bits per second transmitted.

### ***Bently Nevada***

A manufacturer of shaft vibration monitoring equipment.

### ***BIOS***

Basic input/output system. Performs the controller boot-up, which includes hardware self-tests and the file system loader. The BIOS is stored in EEPROM and is not loaded from the toolbox.

### ***bit***

Binary Digit. The smallest unit of memory used to store only one piece of information with two states, such as One/Zero or On/Off. Data requiring more than two states, such as numerical values 000 to 999, requires multiple bits (see Word).

## ***block***

Instruction blocks contain basic control functions, which are connected together during configuration to form the required machine or process control. Blocks can perform math computations, sequencing, or continuous control. The ToolboxST application receives a description of the blocks from the block libraries.

## ***board***

Printed wiring board.

## ***Boolean***

Digital statement that expresses a condition that is either True or False. In the toolbox, it is a data type for logical signals.

## ***Bus***

An electrical path for transmitting and receiving data.

## ***byte***

A group of binary digits (bits); a measure of data flow when bytes per second.

## ***CIMPLICITY***

Operator interface software configurable for a wide variety of control applications.

## ***COI***

Computer Operator Interface that consists of a set of product and application specific operator displays running on a small panel computer hosting Embedded Windows NT.

## ***COM port***

Serial controller communication ports (two). COM1 is reserved for diagnostic information and the Serial Loader. COM2 is used for I/O communication

## ***configure***

To select specific options, either by setting the location of hardware jumpers or loading software parameters into memory.

## ***CRC***

Cyclic Redundancy Check, used to detect errors in Ethernet and other transmissions.



## ***CT***

Current Transformer, used to measure current in an ac power cable.

## ***data server***

A PC which gathers control data from input networks and makes the data available to PCs on output networks.

## ***DCS (Distributed Control System)***

Control system, usually applied to control of boilers and other process equipment.

## ***DDPT***

IS200DDPT Dynamic Pressure Transducer Terminal Board that is used in conjunction with the IS200VAMA VME Acoustic Monitoring Board that is used to monitor acoustic or pressure waves in the turbine combustion chamber.

## ***dead band***

A range of values in which the incoming signal can be altered without changing the output response.

## ***device***

A configurable component of a process control system.

## ***DIN-rail***

European standard mounting rail for electronic modules.

## ***DLAN+***

GE Energy LAN protocol, using an ARCNET controller chip with modified ARCNET drivers. A communications link between exciters, drives, and controllers, featuring a maximum of 255 drops with transmissions at 2.5 MBPS.

## ***DRAM***

Dynamic Random Access Memory, used in microprocessor-based equipment.

## ***EGD***

Ethernet Global Data is a control network and protocol for the controller. Devices share data through EGD exchanges (pages).

## ***EMI***

Electro-magnetic interference; this can affect an electronic control system

## ***Ethernet***

LAN with a 10/100 M baud collision avoidance/collision detection system used to link one or more computers together. Basis for TCP/IP and I/O services layers that conform to the IEEE 802.3 standard, developed by Xerox, Digital, and Intel.

## ***EVA***

Early valve actuation, to protect against loss of synchronization.

## ***event***

A property of Status\_S signals that causes a task to execute when the value of the signal changes.

## ***EX2000 (Exciter)***

GE generator exciter control; regulates the generator field current to control the generator output voltage.

## ***EX2100 (Exciter)***

Latest version of GE generator exciter control; regulates the generator field current to control the generator output voltage.

## ***fanned input***

An input to the terminal board which is connected to all three TMR I/O boards.

## ***fault code***

A message from the controller to the HMI indicating a controller warning or failure.

## ***firmware***

The set of executable software that is stored in memory chips that hold their content without electrical power, such as EEPROM.

## ***flash***

A non-volatile programmable memory device.

## ***forcing***

Setting a live signal to a particular value, regardless of the value blockware or I/O is writing to that signal.

## ***frame rate***

Basic scheduling period of the controller encompassing one complete input-compute-output cycle for the controller. It is the system dependent scan rate.

## ***function***

The highest level of the blockware hierarchy, and the entity that corresponds to a single .tre file.

## ***gateway***

A device that connects two dissimilar LAN or connects a LAN to a wide-area network (WAN), pc, or a mainframe. A gateway can perform protocol and bandwidth conversion.

## ***Graphic Window***

A subsystem of the ToolboxST application for viewing and setting the value of live signals.

## ***health***

A term that defines whether a signal is functioning as expected.

## ***heartbeat***

A signal emitted at regular intervals by software to demonstrate that it is still active.

## ***hexadecimal (hex)***

Base 16 numbering system using the digits 0-9 and letters A-F to represent the decimal numbers 0-15. Two hex digits represent 1 byte.

## ***HMI***

Human Machine Interface, usually a PC running CIMPLICITY software.

## ***HRSG***

Heat Recovery Steam Generator using exhaust from a gas turbine.

## ***ICS***

Integrated Control System. ICS combines various power plant controls into a single system.

## ***IEEE***

Institute of Electrical and Electronic Engineers. A United States-based society that develops standards.

## ***initialize***

To set values (addresses, counters, registers, and such) to a beginning value prior to the rest of processing.

## ***I/O Device***

Input/output hardware device that allow the flow of data into and out

## ***I/O***

Input/output interfaces that allow the flow of data into and out of a device

## ***I/O drivers***

Interface the controller with input/output devices, such as sensors, solenoid valves, and drives, using a choice of communication networks.

## ***I/O mapping***

Method for moving I/O points from one network type to another without needing an interposing application task.

## ***IONet***

The Mark VI I/O Ethernet communication network (controlled by the VCMIs)

## ***insert***

Adding an item either below or next to another item in a configuration, as it is viewed in the hierarchy of the Outline View of the ToolboxST application.

## ***instance***

Update an item with a new definition.

## ***item***

A line of the hierarchy of the Outline view of the ToolboxST application, which can be inserted, configured, and edited (such as Function or System Data)

## ***IP Address***

The address assigned to a device on an Ethernet communication network.

## ***LCI Static Starter***

This runs the generator as a motor to bring a gas turbine up to starting speed.

## ***logical***

A statement of a true sense, such as a Boolean

## ***macro***

A group of instruction blocks (and other macros) used to perform part of an application program. Macros can be saved and reused.

## ***Mark VIe Turbine controller***

A controller hosted in one or more VME racks that perform turbine-specific speed control, logic, and sequencing.

## ***median***

The middle value of three values; the median selector picks the value most likely to be closest to correct.

## ***Modbus***

A serial communication protocol developed by Modicon for use between PLCs and other computers.

## ***module***

A collection of tasks that have a defined scheduling period in the controller.

## ***MTBFO***

Mean Time Between Forced Outage, a measure of overall system reliability.

## ***NEMA***

National Electrical Manufacturers Association; a U.S. standards organization.

## ***non-volatile***

The memory specially designed to store information even when the power is off.

## ***online***

Online mode provides full CPU communications, allowing data to be both read and written. It is the state of the ToolboxST application when it is communicating with the system for which it holds the configuration. Also, a download mode where the device is not stopped and then restarted.

## ***pcode***

A binary set of records created by the ToolboxST application, which contain the controller application configuration code for a device. Pcode is stored in RAM and flash memory.

## ***period***

The time between execution scans for a module or task - also a property of a module that is the base period of all of the tasks in the module

## ***pin***

Block, macro, or module parameter that creates a signal used to make interconnections.

## ***Plant Data Highway (PDH)***

Ethernet communication network between the HMI Servers and the HMI Viewers and workstations

## ***PLC***

Programmable Logic Controller. Designed for discrete (logic) control of machinery. It also computes math (analog) function and performs regulatory control.

## ***PLU***

Power load unbalance, detects a load rejection condition which can cause overspeed.

## ***Power Distribution Module (PDM )***

The PDM distributes 125 V dc and 115 V ac to the VME racks and I/O terminal boards.

## ***PROFIBUS***

An open fieldbus communication standard defined in international standard EN 50 170 and is supported in simplex Mark VIe systems.

## ***Proximitator***

Bently Nevada's proximity probes used for sensing shaft vibration.

## ***PT***

Potential Transformer, used for measuring voltage in a power cable.

## ***QNX***

A real time operating system used in the controller.

## ***real time***

Immediate response, referring to process control and embedded control systems that must respond instantly to changing conditions.

## ***reboot***

To restart the controller or the ToolboxST application.

## ***RFI***

Radio Frequency Interference is high frequency electromagnetic energy which can affect the system.

## ***register page***

A form of shared memory that is updated over a network - register pages can be created and instanced in the controller and posted to the SDB

## ***resources***

Also known as groups. Resources are systems (devices, machines, or work stations where work is performed) or areas where several tasks are carried out. Resource configuration plays an important role in the CIMPLICITY system by routing alarms to specific users and filtering the data users receive.

## ***RPSM***

IS2020RPSM Redundant Power Supply Module for VME racks that mounts on the side of the control rack instead of the power supply. The two power supplies that feed the RPSM are mounted remotely.

## ***RTD***

Resistance Temperature Device used for measuring temperature.

## ***runtime***

See product code.

## ***runtime errors***

Controller problems indicated on the front panel by coded flashing LEDS, and also in the Log View of the ToolboxST application.

## ***sampling rate***

The rate at which process signal samples are obtained, measured in samples/second.

## ***Serial Loader***

Connects the controller to the toolbox PC using the RS-232C COM ports. The Serial Loader initializes the controller flash file system and sets its TCP/IP address to allow it to communicate with the ToolboxST application over Ethernet.

## ***Server***

A pc which gathers data over Ethernet from plant devices, and makes the data available to PC-based operator interfaces known as viewers.

## ***SIFT***

Software Implemented Fault Tolerance, a technique for voting the three incoming I/O data sets to find and inhibit errors. Note that Mark VIe also uses output hardware voting.

## ***signal***

The basic unit for variable information in the controller.

## ***Simplex***

Operation that requires only one set of control and I/O, and generally uses only one channel. The entire Mark VIe control system can operate in simplex mode, or individual VME boards in an otherwise TMR system can operate in implex mode.

## ***stall detection***

Detection of stall condition in a gas turbine compressor.

## ***SOE***

Sequence of Events, a high-speed record of contact closures taken during a plant upset to allow detailed analysis of the event.

## ***Static Starter***

See LCI.

## ***symbols***

Created by the ToolboxST application and stored in the controller, the symbol table contains signal names and descriptions for diagnostic messages.



## ***task***

A group of blocks and macros scheduled for execution by the user.

## ***TBAI***

Analog input terminal board, interfaces with VAIC.

## ***TBAO***

Analog output terminal board, interfaces with VAOC.

## ***TBCC***

Thermocouple input terminal board, interfaces with VTCC.

## ***TBCI***

Contact input terminal board, interfaces with VCCC or VCRC.

## ***TCP/IP***

Communications protocols developed to inter-network dissimilar systems. It is a de facto UNIX standard, but is supported on almost all systems. TCP controls data transfer and IP provides the routing for functions, such as file transfer and e-mail.

## ***TGEN***

Generator terminal board, interfaces with VGEN.

## ***TMR***

Triple Modular Redundancy. An operation that uses three identical sets of control and I/O (channels R, S, and T) and votes the results.

## ***ToolboxST***

A Windows-based software package used to configure the Mark VIe controllers, also exciters and drives.

## ***TPRO***

Turbine protection terminal board, interfaces with VPRO.

## ***TPYR***

Pyrometer terminal board for blade temperature measurement, interfaces with VPYR.

## ***TREG***

Turbine emergency trip terminal board, interfaces with VPRO.

## ***trend***

A time-based plot to show the history of values, similar to a recorder, available in the Historian and the ToolboxST application.

## ***TRL Y***

Relay output terminal board, interfaces with VCCC or VCRC.

## ***TRPG***

Primary trip terminal board, interfaces with VTUR.

## ***TRTD***

RTD input terminal board, interfaces with VRTD.

## ***TSVO***

Servo terminal board, interfaces with VSVO.

## ***TTUR***

Turbine terminal board, interfaces with VTUR.

## ***TVIB***

Vibration terminal board, interfaces with VVIB.

## ***UCVB***

A version of the Mark VIe controller.

## ***Unit Data Highway (UDH)***

Connects the Mark VIe controllers, LCI, EX2000, PLCs, and other GE provided equipment to the HMI Servers.

## ***validate***

Makes certain that the ToolboxST application items or devices do not contain errors, and verifies that the configuration is ready to be built into pcode.

## ***VAMA***

IS200VAMA VME Acoustic Monitoring Board that is used in conjunction with the IS200DDPT Dynamic Pressure Transducer Terminal Board to monitor acoustic or pressure waves in the turbine combustion chamber.

## ***VCMI***

The Mark VIe VME communication board which links the I/O with the controllers.

## ***VME board***

All the Mark VIe boards are hosted in Versa Module Eurocard (VME) racks.

## ***VPRO***

Mark VIe Turbine Protection Module, arranged in a self contained TMR subsystem.

## ***Windows NT***

Advanced 32-bit operating system from Microsoft for 386-based PCs and above.

## ***word***

A unit of information composed of characters, bits, or bytes, that is treated as an entity and can be stored in one location. Also, a measurement of memory length, usually 4, 8, or 16-bits long.



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